

ORIGINAL RESEARCH

An interleaved non-isolated high gain soft switching DC–DC converter with small input current ripple

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Abstract

This article suggests a non-isolated high step-up interleaved DC–DC topology for renewable energy applications. Two three-winding coupled-inductors along with two voltage multiplier cells are used to enhance the voltage gain significantly. One interesting aspect of this new topology is that high duty cycles are not required to achieve high voltage gains; this is done by adjusting the turn ratio of the coupled inductors. Moreover, the presented interleaved converter enjoys not only having less current stress due to the interleaving structure, but also showing 16% increase in voltage gain compared to the best similar boost topologies. Additional elements are designed for the purpose of soft switching and gain increase, which have little effect on the cost, weight and size of the proposed converter. Interestingly, the voltage stresses both on the switching devices and passive elements are much less than the output voltage. Furthermore, the coupled inductor's leakage inductance energy is recovered by employing a passive clamp circuit to minimize stresses across the semi-conductors; therefore, efficiency is improved. The suggested converter is analyzed in the steady state, and a 400 W experimental setup was implemented; the outcomes verify the practicality of the proposed boost converter in accordance with the analysis.

1 | INTRODUCTION

Sustainable DC resources, such as fuel cells and solar panels, typically provide low and variable output voltages; connection of these resources to the grid-tied inverters needs intermediate DC adjustment. Hence, DC–DC topologies with higher voltage gains are needed [1, 2]. The utilization of low duty cycles to retain highly efficient converters is one of the attractive characteristics of such converters, which is not practically feasible with conventional converters. High efficiency, low complexity, reduced cost, and low input ripple current are the most essential characteristics needed for high gain DC–DC topologies used in PV systems [3]. Excessive quadratic voltage gain could be achieved by cascading boost topologies, which eliminate applying extreme duty cycle values. Nevertheless, the active switch and diode in the second cell could suffer an excessive voltage stress. Furthermore, the first-stage switch could be switched at a high frequency, whereas the second-stage switch must be driven at a lower frequency to avoid significant switching losses. This

sort of multi-stage power conversion could reduce efficiency significantly [4].

The proposed converter in [5] can enhance the output voltage gain without utilizing any magnetic equipment including a transformer; however, its design is complex due to the large number of MOSFETs used to improve the voltage level. In practice, high duty cycles for DC–DC topologies are inefficient when converting a large voltage gain. In fact, high duty cycles make long conduction times for the converter's switching devices; hence, switching component conduction losses will grow, resulting in significant power losses in practical systems.

Numerous high step-up coupled-inductor (CI) based topologies have been suggested with features of low voltage stress, high voltage gain, and low total losses [6–14]. Lately, CI method with the performance of recycling energy of leakage inductance has been widened to enhance voltage conversion coefficient. Owing to their secondary leakage inductance, these kinds of topologies exhibit minimal reverse recovery ringing and provide soft switching of the output diode. However, employing a larger

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turn ratio and a very high duty cycle to obtain a better voltage gain results in increased EMI noise and power losses. In [6–14], several three-winding CI topologies are discussed, allowing for more adjustable voltage stress and voltage gain control. Nevertheless, owing to one active power switch, the nominal output power of these converters is restricted, and the voltage gain is still insufficient to be connected directly to the grid-tied inverter.

Switched inductor and switched capacitor DC–DC topologies are also among choices for increasing voltage gain [15–17]. Nevertheless, getting exceptionally high voltage gain requires additional elements, leading to higher costs and more complicated circuits. In addition, voltage stresses on transistors or other components are high in switched-inductor circuits, while the current stress on devices is high in switched-capacitor circuits, resulting in significant conduction losses. In practice, certain passive or active clamp circuit is needed to absorb switching spikes which are caused by leakage inductances and recover the linked inductor's leakage energy to the circuit, leading to a rise in total efficiency [18].

This paper proposes an interleaved high step-up DC–DC converter with two switches and two three-winding CIs. To reach a greater voltage gain, the suggested converter combines voltage multiplier cells with two CIs, where the CIs contribute static gain, and the voltage multiplier cell can add further voltage gain. Also, using a CI with three windings in the described topology results in more adjustable voltage gain and voltage stress control on every semiconductor device. In this topology, a passive voltage clamp module is used to recover the CI's remaining energy. The suggested boost topology is analyzed in six modes of operation per cycle, where a 400 W laboratory prototype provides experimental outcomes that verify operation of converter according to the discussed operating principles and performed analysis. This article is arranged in the following manner. The suggested converter's topology and principle of operation are illustrated in Section 2. The main parameters of the proposed topology like voltage gain and voltage stress on semiconductors are calculated in Section 3. The design steps of components and efficiency analyzes are mentioned in Section 4. The control of this converter is briefly checked in Section 5. The sixth section includes a comparison of this converter with similar topologies. Section 6 discusses the experimental outcomes as well as the analysis performed in six steps per cycle. Eventually, Section 7 brings this paper to a conclusion.

2 | PROPOSED CONVERTER: OPERATION MODES AND ANALYSIS

Figure 1 depicts the power circuit of the suggested high step-up DC–DC converter with two switches and two three-winding CIs. The converter is made up of two active power switches (S_1, S_2), six capacitors ($C_1, C_2, C_3, C_4, C_5, C_6$), two resonance capacitors (C_{r1}, C_{r2}), six diodes ($D_1, D_2, D_3, D_4, D_5, D_6$), two input inductors (L_{in1}, L_{in2}) and two three-winding CIs. The three-winding CI is represented by an ideal transformer with turn ratios ($N_p:N_s:N_T$), a leakage inductance, L_{Lkg} and a magnetizing inductance L_m . Thus, turn ratios of the first CI

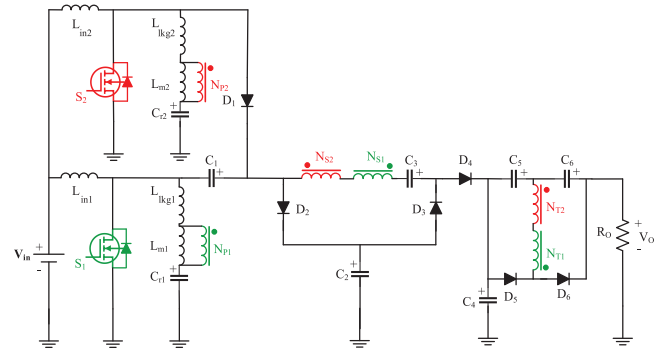


FIGURE 1 Suggested interleaved boost converter topology

(in red) are defined as $n_{21} = \frac{N_{S1}}{N_{P1}}$, $n_{31} = \frac{N_{T1}}{N_{P1}}$, and $n_{22} = \frac{N_{S2}}{N_{P2}}$, $n_{32} = \frac{N_{T2}}{N_{P2}}$ for the second CI (in green).

Operation principles of the proposed three-winding CI DC–DC topology in CCM can be divided into six-time intervals. Figure 2 illustrates the conducting circuits of the suggested design in six different operation modes. Also, Figure 3 shows typical waveforms of six CCM operation modes in accordance with conducting circuits of Figure 2. The following subsections explain analysis of the converter (see Figure 1) in order to describe high gain build-up achievement.

2.1 | Mode 1

The switch S_1 is turned on; L_{in1} is charged through the source, capacitor C_1 is charged through L_{in2} and diode D_1 , capacitor C_3 is charged through capacitor C_2 and diode D_3 , and capacitor C_5 is charged through N_{T1} and diode D_5 . The CIs contribute to the charging process of mentioned capacitors. Due to the presence of input inductor L_{in1} , the current through S_1 increases slowly, turning on in the ZCS situation. In this mode, diode D_5 turns on with a low current slope due to the presence of the CI. This mode ends when diode D_1 turns off. The voltage over CIs and input inductor can be given as shown in as below (see Figure 2a):

$$V_{L_{in1}}^D = V_{in} \quad (1)$$

$$V_{L_{m1}}^D = \left[\frac{L_{m1}}{L_{m1} + L_{lkg1}} \right] V_{Cr1} = k V_{Cr1} \quad (2)$$

$$V_{L_{kg1}}^D = \left[\frac{L_{lkg1}}{L_{m1} + L_{lkg1}} \right] V_{Cr1} = (1 - k) V_{Cr1} \quad (3)$$

$$V_{L_{in2}}^{D'} = V_{in} - V_{C1} \quad (4)$$

$$V_{L_{m2}}^{D'} = \left[\frac{L_{m2}}{L_{m2} + L_{lkg2}} \right] (V_{Cr2} - V_{C1}) = k' (V_{Cr2} - V_{C1}) \quad (5)$$

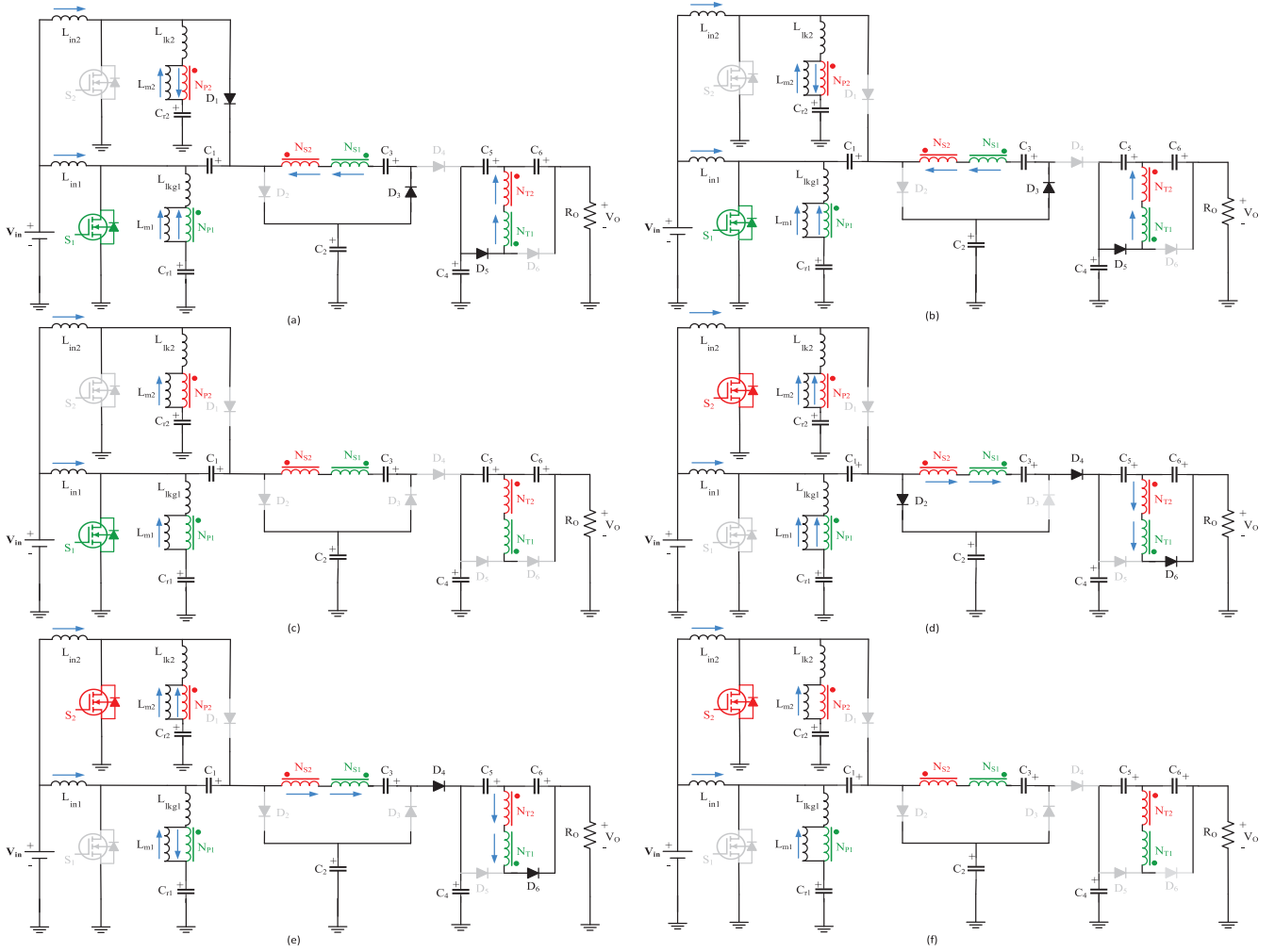


FIGURE 2 The CCM operation of the proposed boost converter during a full switching period in six steps; equivalent circuits of the suggested topology. (a) Mode 1, (b) mode 2, (c) mode 3, (d) mode 4, (e) mode 5, and (f) mode 6

2.2 | Mode 2

While statuses of active switches remain unchanged, diode D_1 turning off under a ZCS condition (current through D_2 approached zero during the C_2 charge-up, almost no minority carriers for reverse recovery process). This second interval continues until the resonance between the capacitor C_{r1} and the leakage inductance L_{Lkg1} ends ($T_{r1} = 2\pi\sqrt{L_{Lkg1}C_{r1}}$); the current of the S_1 decreases slightly from its maximum state and the diodes D_3 and D_5 turn off under a ZCS situation. The voltage over secondary and tertiary of CI and capacitors are obtained as below (see Figure 2b):

$$V_{NS1}^D = n_{21} V_{Lm1}^D \quad (6)$$

$$V_{NS2}^{D'} = n_{22} V_{Lm2}^{D'} \quad (7)$$

$$V_{NT1}^D = n_{31} V_{Lm1}^D \quad (8)$$

$$V_{NT2}^{D'} = n_{32} V_{Lm2}^{D'} \quad (9)$$

$$V_{C3} = V_{C2} - V_{NS2}^{D'} + V_{NS1}^D - V_{C1} \quad (10)$$

$$V_{C5} = V_{NT1}^D - V_{NT2}^{D'} \quad (11)$$

2.3 | Mode 3

During this short time, all the diodes are off and this mode continues until switch S_1 is turned off (hard switching) when the total time DT_S is completed.

2.4 | Mode 4

This interval starts when S_1 is turned off (hard switching) and the second switch S_2 is turned on under a ZCS condition while

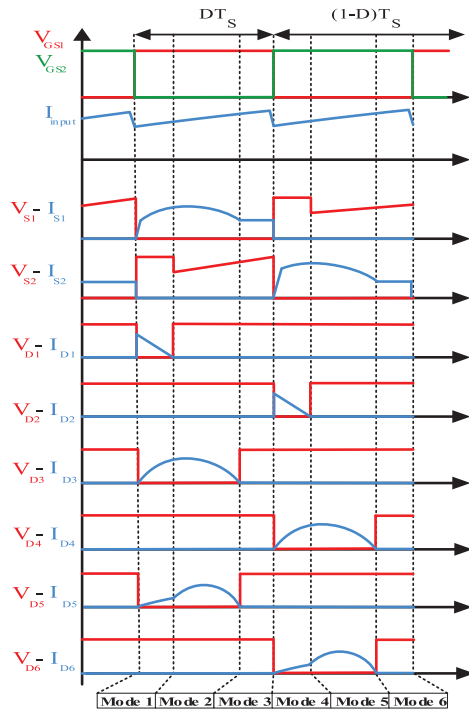


FIGURE 3 Voltage and current waveforms of two active switches (S_1, S_2) and six diodes ($D_1, D_2, D_3, D_4, D_5, D_6$) for a switching period divided in six modes

current through the inductance L_{in2} is charged from zero. In this case, diode D_2 turns on to act as a clamping diode to suppress voltage spike on switch S_1 by redirecting the stored energy of the leakage inductance L_{lk2} towards the capacitor C_2 . Also, D_6 is on and its current is like that of diode D_5 in the first mode. The voltage over L_{m2} and input inductor are derived as below (see Figure 2d):

$$V_{Lin2}^D = V_{in} \quad (12)$$

$$V_{Lm2}^D = \left[\frac{L_{m2}}{L_{m2} + L_{lk2}} \right] V_{Cr2} = k' V_{Cr2} \quad (13)$$

$$V_{Lk2}^D = \left[\frac{L_{lk2}}{L_{m2} + L_{lk2}} \right] V_{Cr2} = (1 - k') V_{Cr2} \quad (14)$$

$$V_{Lin1}^{D'} = V_{in} + V_{C1} - V_{C2} \quad (15)$$

$$V_{Lm1}^{D'} = k(V_{Cr1} + V_{C1} - V_{C2}) \quad (16)$$

2.5 | Mode 5

While S_2 is on (and S_1 is off), diode D_2 turning off under a ZCS condition (current through D_2 approached zero during the C_2 charge-up, almost no minority carriers for reverse recovery process). This interval continues until the resonance between

the capacitor C_{r2} and the leakage inductor L_{lk2} ends ($T_{r2} = 2\pi\sqrt{L_{lk2}C_{r2}}$); the current through S_2 slightly decreases from its maximum state, both diodes D_4 and D_6 are turned off under a ZCS situation. The voltage over secondary and tertiary of CI and capacitors can be given as below (see Figure 2e):

$$V_{NS1}^{D'} = n_{21} V_{Lm1}^{D'} \quad (17)$$

$$V_{NS2}^D = n_{22} V_{Lm2}^D \quad (18)$$

$$V_{NT1}^{D'} = n_{31} V_{Lm1}^{D'} \quad (19)$$

$$V_{NT2}^D = n_{32} V_{Lm2}^D \quad (20)$$

$$V_{C4} = V_{C3} + V_{NS2}^D - V_{NS1}^{D'} + V_{C1} - V_{Lin1}^{D'} + V_{in} \quad (21)$$

$$V_{C6} = V_{NT2}^D - V_{NT1}^{D'} \quad (22)$$

2.6 | Mode 6

During this time interval all diodes are off, similar to those of Mode 3, where the switch S_2 is turned off (hard switching) at the end of the full period T_s .

It is important to note that diodes D_1 and D_4 are in the power transmission path; but the current through D_4 is very low because it is located at the output stage of the suggested converter. This can be clearly seen from experimental outcomes in Figure 10 that the current of this diode is much lower than the current of the input stage components. Thus, the power losses of D_4 is considerably low in practice. Regarding D_1 , this diode is in on-state only for a short time (during the mode I) and it is off for the other five modes, imposing low power losses to the converter.

3 | STEADY-STATE ANALYSIS OF THE PROPOSED TOPOLOGY

3.1 | Voltage gain calculations

By applying the volt-second equilibrium rule to both inductors L_{in1} and L_{in2} (see (4), (12), (1) and (15)) ($D' = 1 - D$):

$$D(V_{Cr1}) + D'(V_{in} + V_{C1} - V_{C2}) = 0 \quad (23)$$

$$\begin{cases} V_{C1} = \frac{V_{in}}{D'} \\ V_{C2} = \frac{2V_{in}}{D'} \end{cases} \quad (24)$$

Substituting (24) in the volt-second rule both for L_{m1} (see (2) and (16)) and L_{m2} (see (5) and (13)) results in:

$$\begin{cases} V_{Cr2} = D' V_{C1} = V_{in} \\ V_{Cr1} = D' (V_{C2} - V_{C1}) = V_{in} \end{cases} \quad (25)$$

Also, considering (25), (2), (6) and (8) gives:

$$\begin{cases} V_{NS1}^D = kn_{21} V_{in} \\ V_{NT1}^D = kn_{31} V_{in} \end{cases} \quad (26)$$

Similarly, combination of (25), (13), (18) and (20) gives:

$$\begin{cases} V_{NS2}^D = kn_{22} V_{in} \\ V_{NT2}^D = kn_{32} V_{in} \end{cases} \quad (27)$$

By substituting (24) and (25) in (16), also (28) in (17) and (18):

$$\begin{cases} V_{Lm1}^{D'} = -k \frac{D}{D'} V_{in} \\ V_{NS1}^{D'} = -kn_{21} \frac{D}{D'} V_{in} \\ V_{NT1}^{D'} = -kn_{31} \frac{D}{D'} V_{in} \end{cases} \quad (28)$$

Similarly, by substituting (24) and (25) in (5), also (35) into (7) and (9):

$$\begin{cases} V_{Lm2}^{D'} = -k' \frac{D}{D'} V_{in} \\ V_{NS2}^{D'} = -k' n_{22} \frac{D}{D'} V_{in} \\ V_{NT2}^{D'} = -k' n_{32} \frac{D}{D'} V_{in} \end{cases} \quad (29)$$

Substituting (24), (26) and (29) in (10) results in:

$$V_{C3} = \left(1 + k' \left(n_{21} + n_{22} \frac{D}{D'} \right) \right) V_{in} \quad (30)$$

By substituting (24) in (15):

$$V_{Lin1}^{D'} = -\frac{D}{D'} V_{in} \quad (31)$$

By substituting (24), (27), (28), (30) and (31) in (21), also (26) and (29) in (11) together with (27) and (28) in (22), we get (both

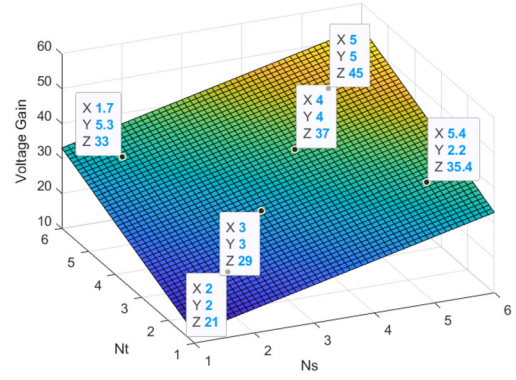


FIGURE 4 Voltage gain changes versus secondary and tertiary turn ratio

CI specifications are the same, i.e. $k = k'$):

$$\begin{cases} V_{C4} = k(n_{21} + n_{22}) \frac{V_{in}}{D'} + \frac{2 + D'}{D'} V_{in} \\ V_{C5} = k \left(n_{31} + n_{32} \frac{D}{D'} \right) V_{in} \\ V_{C6} = k \left(n_{31} \frac{D}{D'} + n_{32} \right) V_{in} \end{cases} \quad (32)$$

Finally, the nominal gain of the suggested boost topology can be derived by substitution of (32) in (23) as below:

$$\frac{V_O}{V_{in}} = 1 + \frac{k(n_{21} + n_{22} + n_{31} + n_{32}) + 2}{D'} \quad (33)$$

Hence, for a given D , maximum gain of the converter is achieved, if under ideal condition the coupling coefficient k is equal to 1. Figure 4 shows the voltage gain versus secondary and tertiary turn ratios. Also, it is assumed that the secondary and tertiary turn ratios are identical for both CIs ($n_{31} = n_{32}$ and $n_{21} = n_{22}$).

3.2 | Voltage stresses on semiconductor devices

Considering Figure 2a–f as well as the performed analysis in Section 3.1, the voltage stresses across the power MOSFET and diodes could be worked out as follows:

$$\begin{cases} V_{S1} = V_{S2} = V_{D2} = \frac{V_{in}}{D'} \\ V_{D1} = \frac{2V_{in}}{D'} \\ V_{D3} = V_{D4} = (n_{21} + n_{22}) \frac{V_{in}}{D'} + V_{in} \\ V_{D5} = V_{D6} = (n_{31} + n_{32}) \frac{V_{in}}{D'} \end{cases} \quad (34)$$

4 | DESIGN PROCEDURE AND EFFICIENCY

The following subsections describes how to design different parameters of the suggested topology as well as obtaining efficiency of the converter.

4.1 | Input inductances

Inductances of the input inductors are obtained as below:

$$L_{in1} = L_{in2} > \frac{V_{in} D}{\Delta I_{in} f_s} \quad (35)$$

4.2 | Capacitors

Assume average current, voltage and power of each capacitor is equal to I_O , V_O and P_O ; then, the minimum capacitance can be worked out as follows (the ESR of the capacitors are ignored due to their small sizes):

$$C > \frac{P_O}{V_O \Delta V_C f_s} \quad (36)$$

4.3 | Magnetizing inductance of the CIs

The magnetic inductances are obtained from the following relationship, where their equivalent series resistors are ignored due to their small sizes:

$$L_{m1} = L_{m2} = L_{Lm} = \frac{V_{in} D}{\Delta I_{Lm} f_s} \quad (37)$$

4.4 | Resonant circuits

As mentioned earlier, the diode D_4 turns off in the ZCS condition due to the resonance tank. To calculate the resonant capacitor C_{r1} and the leakage inductance of the CI (L_{lkg1}), these elements are designed according to [20] to operate in boundary-resonance mode to reduce output diode switching losses and improve the reverse recovery problems. Also, the amount of L_{lkg1} depends on how the CI winding is wound and thus the following equation is obtained:

$$\pi \sqrt{L_{lkg1} C_{r1}} \leq DT_s \rightarrow C_{r1} \leq \frac{D^2}{\pi^2 L_{lkg1} f_s^2} \quad (38)$$

Assuming $L_{lkg2} = L_{lkg1}$, then $C_{r2} = C_{r1}$.

4.5 | Power losses and efficiency

In order to accurately evaluate the performance of the converter, it would be better to analyze the converter losses by dividing into five groups as follows.

4.5.1 | Switching and conduction losses (S_1 and S_2)

Losses of one switch is divided into two categories; switching losses and conduction losses. Due to the soft turn on of the two active switches, the switching losses only include turning off losses. Hence, switching and conduction losses can be computed as below:

$$\left\{ \begin{array}{l} P_{loss-turn\ OFF} = \left(\frac{1}{2} V_{DS} I_{DS} t_{turn-OFF} \right) f_s \\ P_{oss} = \frac{1}{2} * f_s * C_{oss} * V_{ds}^2 \\ P_{loss-conduction} = R_{DS(on)} \times I_{DS(RMS)}^2 \\ P_{loss-S1} = P_{loss-S2} = P_{loss-turn\ OFF} + P_{loss-conduction} \end{array} \right. \quad (39)$$

where R_{DS} of the MOSFET is typically about 6.3 m Ω .

4.5.2 | Diodes

The suggested topology operation shows that both the conductive losses and the reverse recovery losses (due to very low minority carriers) of the diodes are ignorable; the main losses of the diodes are related to their forward voltage drops times the average current through diodes as below:

$$P_{loss-diode} = V_{Forward-diode} \times I_{D-average} \quad (40)$$

It should be noted that diodes D_{1-4} have a ZCS operation in turning off and do not have reverse recovery losses. Also, the reverse recovery losses of the diodes $D_{5,6}$ can be ignored.

4.5.3 | ESR loss of C_4

All capacitors are of non-electrolyte MKT (nearly ideal) except electrolyte capacitors C_4 that its non-ideal internal resistive loss is worked out as below (ESR = 100 m Ω):

$$P_{loss(c4)} = ESR \times I_{COUT(RMS)}^2 \quad (41)$$

4.5.4 | Conductive and magnetic losses of inductors

Core loss of the two inductors is obtained from their core datasheet (T131-52 iron powder), which is 125 mW/cm³. Hence, adding the conduction loss to core loss will result in total losses of inductors as below:

$$P_{loss(Lin1)} = P_{loss(Lin2)} = P_{loss(core)} + P_{loss(conduction)} \quad (42)$$

TABLE 1 Designed boundary parameters of the suggested converter according to (35)–(38) for a 400 prototype

Designed parameters	ΔV_C	Boundary capacitance	Designed parameters	ΔI_L	Boundary inductance
C_1	5%	9.52 μ F	L_{in1}	15%	130 μ H
C_2	4%	6.09 μ F	L_{in2}	15%	130 μ H
C_3	2%	9.75 μ F	L_{m1}	15%	68.96 μ H
C_4	1%	75.05 μ F	L_{m2}	15%	68.96 μ H
C_5	3%	8.13 μ F	L_{lk1}	-	$\sim 1 \mu$ H
C_6	3%	8.13 μ F	L_{lk2}	-	$\sim 1 \mu$ H
C_{r1}, C_{r2}	-	10.14 μ F			

TABLE 2 Calculated losses and efficiency of the suggested converter according to (39)–(42) for a 400 prototype

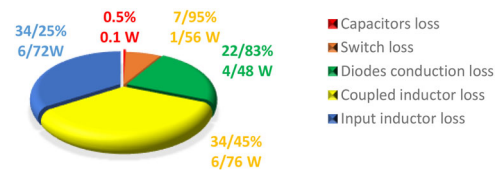
Dissipative element	Power losses (W)	
Active switches (S_1, S_2) $R_{DS} = 6.3 \text{ m}\Omega$	Turn-off	Conduction
	2×0.15	2×0.63
Diodes ($D_1, D_2, D_3, D_4, D_5, D_6$): worst case	$5 \times (1 \times 0.78) + 1 \times 0.58$	
ESR of electrolyte capacitor C_4		0.1
Inductors (L_{in1}, L_{in2}) Core datasheet T131-52 iron powder	Core	Conduction
	2×1.71	2×1.65
CIs Core datasheet ETD49/25/16	Core	Conduction
	2×3.38	-
Total losses		19.62
Efficiency ($P_o / (P_o + \text{Total losses})$)		95.32%

4.5.5 | Losses of CIs

Core loss of the two CIs is obtained from their core datasheet (ETD49/25/16), which is 139 mW/cm^3 . The conductive loss is negligible due to the large number of primary shunted wires.

4.5.6 | Power losses and Efficiency of the suggested converter

Assume the suggested topology is going to be designed for a 400 W prototype. Applying (35)–(38) will result in parameters listed in Table 1, if duty cycle is limited to 0.5, input voltage is 20 V with a gain of 20.5 at $D = 0.5$ and input current ripple is 15%. Furthermore, power losses of all elements are calculated according to (39)–(42), where Table 2 details the power losses as well as efficiency of the designed converter. Also, Figure 5 illustrates distribution of power losses in a pie-chart diagram under the stated operating conditions, showing in total power losses of 19.62 (W) and efficiency of 95.32%.

**FIGURE 5** Power losses of the 400 (W) suggested boost topology in pie-chart under the operating point 20 (V)/ 410 (V) and $D = 0.5$.

5 | COMPARISONS AND DISCUSSIONS

A detailed literature survey has been performed on similar high-gain three-winding CI-based DC to DC topologies recently appeared under the same condition as the suggested topology. Here it is compared several critical specifications of available converters presented in [6–14, 21–25] with those of the suggested converter. Table 3 describes these comparisons on the key properties, introducing number of involved switches, diodes, capacitors, inductors and CIs as well as conversion ratios, voltage stresses on switches and diodes. Figure 6

TABLE 3 A comparison of the proposed DC to DC converter with some other comparable converters

Converters	Number of S/D/C/CI+L	Continuous input current	Common ground	Voltage gain	Voltage stress on switches	Voltage stress on output diode
2018 [6]	1/3/3/1 ^{3w} +0	-	✓	$\frac{n_2+n_3+D(n_3-1)}{(1-D)(n_3-1)}$	$\frac{n_3-1}{n_2+n_3+D(n_3-1)} V_{\hat{O}}$	$\frac{(n_3-1)(1-D)-1+\frac{n_2+n_3+D(n_3-1)}{(1-D)}}{n_2+n_3+D(n_3-1)} V_{\hat{O}}$
2015 [7]	1/4/4/1 ^{3w} +0	✓	✓	$n_3 + \frac{2-D+n_2}{1-D}$	$\frac{n_3}{2-D+n_2(1-D)+n_3} V_{\hat{O}}$	$\frac{1}{2-D+n_2(1-D)+n_3} V_{\hat{O}}$
2019 [8]	1/4/4/1 ^{3w} +0	✓	✓	$\frac{n_3+2n_2-1}{(1-D)(n_2-1)}$	$\frac{(n_2-1)V_{\hat{O}}}{n_3+2n_2-1}$	$\frac{(n_3)V_{\hat{O}}}{(1-D)(n_2-1)}$
2016 [9]	2/4/4/1 ^{3w} +0	-	-	$\frac{1+n_3+D}{1-D}$	$\frac{1}{1+n_3+D} V_{\hat{O}}$	$\frac{n_3}{n_3+1+D} V_{\hat{O}}$
2018 [10]	1/3/3/1 ^{3w} +0	-	✓	$\frac{2n_2+n_3-1}{(1-D)(n_2-1)}$	$\frac{n_2-1}{2n_2+n_3-1} V_{\hat{O}}$	$\frac{n_2+n_3}{2n_2+n_3-1} V_{\hat{O}}$
2018 [11]	1/3/3/1 ^{3w} +0	-	-	$\frac{2+n_3D+n_2}{1-D}$	$\frac{1}{2+n_3D+n_2} V_{\hat{O}}$	$\frac{1+n_2+n_3}{2+n_3D+n_2} V_{\hat{O}}$
2017 [12]	1/3/3/1 ^{3w} +0	-	✓	$\frac{1+\frac{n_1+n_2}{n_1}}{1-D} + \frac{n_3}{n_1}$	$\frac{n_1}{2n_1+n_2+n_3(1-D)} V_{\hat{O}}$	$\frac{n_1 V_{\hat{O}}}{(n_1+n_2)(\frac{n_1}{D-1} + 1 - \frac{n_3}{n_1})(D-1)}$
2020 [13]	1/3/3/1 ^{3w} +1	✓	✓	$\frac{2+n_2-n_3(1+D)}{(1-D)(1-n_3)}$	$\frac{-3n_3+n_2+3}{(2+n_2)(2+n_2-n_3(1+D))} V_{\hat{O}}$	$\frac{1+n_2}{2+n_2-n_3(1+D)} V_{\hat{O}}$
2020 [14]	1/5/5/1 ^{3w} +0	-	✓	$\frac{3+2n_2+n_3}{1-D}$	$\frac{1}{3+2n_2+n_3} V_{\hat{O}}$	$\frac{1+2n_2+n_3}{3+2n_2+n_3} V_{\hat{O}}$
2019 [21]	2/4/4/2 ^{2w} +0	✓	✓	$\frac{2+2n_2}{1-D}$	$\frac{1}{2+2n_2} V_{\hat{O}}$	Not stated in [21]
2019 [22]	3/3/3/0+3	✓	-	$\frac{2+D}{1-D}$	$\frac{1}{2+D} V_{\hat{O}}$	$\frac{2}{2+D} V_{\hat{O}}$
2019 [23]	2/4/4/0+2	✓	-	$\frac{4}{1-D}$	$\frac{1}{4} V_{\hat{O}}$	$\frac{1}{2} V_{\hat{O}}$
2019 [24]	2/10/6/2 ^{3w} +1 ^{2w}	✓	✓	$\frac{1+3n}{1-D}$	$\frac{1}{1+3n} V_{\hat{O}}$	$\frac{1+4n}{1+3n} V_{\hat{O}}$
2018 [25]	2/6/5/1 ^{3w} +2 ^{2w}	✓	✓	$\frac{2(n_3+1)+n_2}{1-D}$	$\frac{1}{2(n_3+1)+n_2} V_{\hat{O}}$	$\frac{2n_3+1+n_2}{2(n_3+1)+n_2} V_{\hat{O}}$
Proposed Converter	2/6/8/2 ^{3w} +2	✓	✓	$1 + \frac{k(n_{21}+n_{22}+n_{31}+n_{32})+2}{1-D}$	$\frac{V_{\hat{O}}}{n_{21}+n_{22}+n_{31}+n_{32}+3-D}$	$\frac{(n_{31}+n_{32})V_{\hat{O}}}{n_{21}+n_{22}+n_{31}+n_{32}+3-D}$

illustrates conversion ratio (voltage gain) of different CI-based high step up topologies with that of the suggested topology according to the relationships given in the fourth column of Table 3, assuming $n_{21} = n_{31} = n_{22} = n_{32} = 2$ for converters of [6–12, 14, 25]. However, the parameter n_3 cannot be equal to 2 for the suggested converter in [13], designed to be 0.175 according to [13]. It can be seen that the proposed converter produces the highest voltage gains at all duty cycles (blue colour) compared to [6–14, 21–25]. Interestingly, the high gains bigger than 20 can be achieved in duty cycles smaller than 0.5.

Moreover, another advantage of the suggested boost topology can be found in Figure 7 in which the normalized voltage stresses on active switches are compared; the suggested topology imposes the lowest voltage stresses on the active switches at all duty cycles (blue colour). It is noticeable that the normalized voltage stress of the active switches does not change much with duty cycle variations. This is significantly beneficial when using MOSFETs both with smaller on-resistances and breaking voltages, enhancing efficiency as well as lowering cost of the active power switches. Further, normalized maximum voltage stresses of output diodes for all available designs

are compared with that of the proposed converter (D_4) as illustrated by Figure 8. While the proposed converter shows nearly fixed normalized voltage stress on output diode for all duty cycles, posing considerably low stress that is smaller than those of [6, 8–11, 13–14, 22–25]; it is bigger than those of [7] and [12] though.

It is noticeable to mention two additional features: Continuous input current and non-isolated common ground connection (see Table 3). Continuous input current makes it ideal for clean energy applications. Nevertheless, the input currents in the recommended designs in [9–12, 14] are discontinuous. Common ground connection is a critical feature for a front-end boost DC–DC topology that is connecting to a grid-connected transformer less inverter.

Meanwhile, the suggested topology includes two switches along with two CIs (in conjunction with resonant capacitors) that is due to the interleaved configuration that reduces the input current ripples considerably. The number of capacitors and diodes are increased in the suggested topology in order to get higher gains, lower voltage and current stresses on switches and diodes as well as high efficiency.

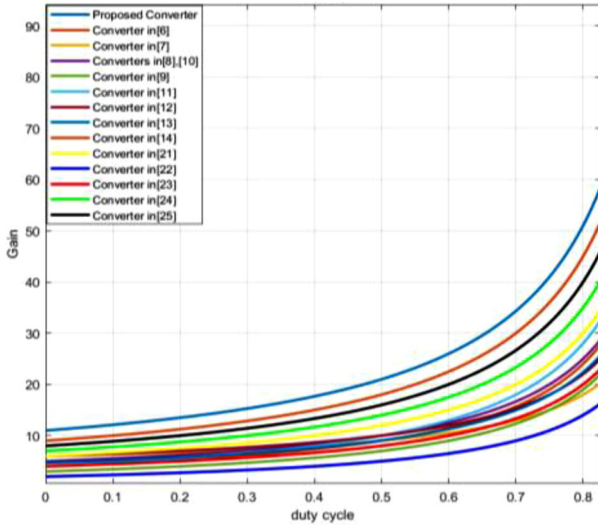


FIGURE 6 Voltage gains of CI-based boost topologies listed in Table 3

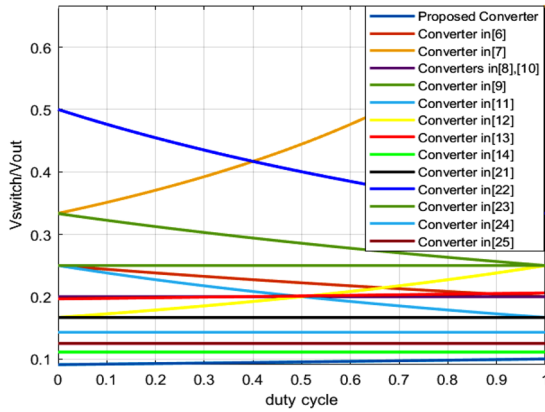


FIGURE 7 Normalized voltage stresses of active power switches of CI-based boost topologies listed in Table 3

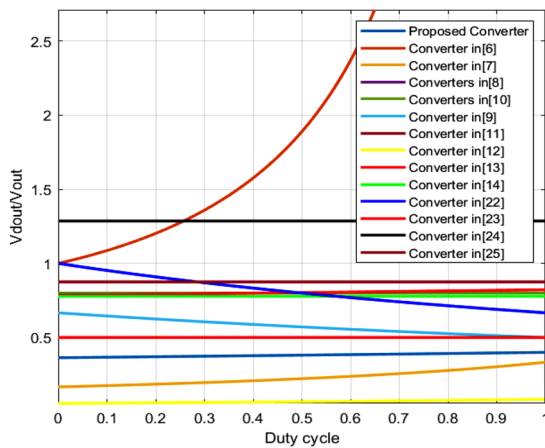


FIGURE 8 Normalized voltage stresses of output diodes of CI-based boost topologies listed in Table 3

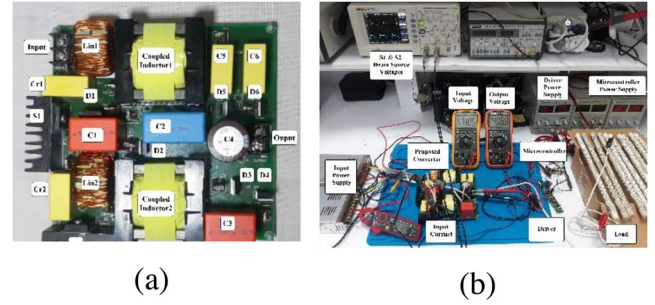


FIGURE 9 (a) Implemented power circuit, and (b) the presented high-step-up converter's experimental platform

In terms of cost comparison, it is important to note that usually in high-efficiency topologies, output diodes and switches can make up a large portion of the converter price. Also, these components are more sensitive to failure due to voltage spikes and the life of the converter is highly dependent on these components. Therefore, by carefully examining Figures 7 and 8, it is obvious that we can use a lower cost power switch(s) and output diode for the proposed converter.

6 | LABORATORY PROTOTYPE AND EXPERIMENTS

The suggested interleaved boost topology (see Figure 1) was implemented by developing a 400 W laboratory prototype to verify the performance and theoretical analysis of the circuit. Figure 9a–b illustrates pictures of the experimental setup, where Table 4 shows the specifications of elements. The source voltage is 20 V, the load voltage is 410 V (voltage gain of 20.50), and the switching frequency of the device is set at 50 kHz to lower the size of the passive elements. Figure 10a–e illustrates experimental waveforms of the implemented topology in CCM (time scale is 5 μ s per division), showing both breaking voltages and conducting currents across the diodes. The measured breaking voltages on diodes ranges from 84 V to about 200 V. Since the capacitor C_1 is charged through diode D_1 , Figure 10a illustrates how the stored energy of inductances L_{in2} and leakage L_{lk2} of the CI is transferred to capacitor C_1 via diode D_1 (I_{D1}).

Also, Figure 10f provides voltage and current of I_{in1} and Figure 10g describes primary of the first CI; voltages and currents of the primary, secondary and tertiary windings of the second CI are shown by Figures 10h, 10i and Figure 10j, contributing to the boosting process by exchanging energy between their magnetic field and capacitors electrical fields. Current and voltage of the active power switches (S_1 and S_2) are shown in Figure 10k,l. It can be seen that the highest voltage stress on the power switch is 54 V, much smaller than the output voltage (about 13 percent). Hence, a low on-resistance MOSFET can be used. Since part of the leakage inductance energy is absorbed by the clamping capacitor and the remaining energy appears as a small spike on the switch, designing proper snubbers lowers

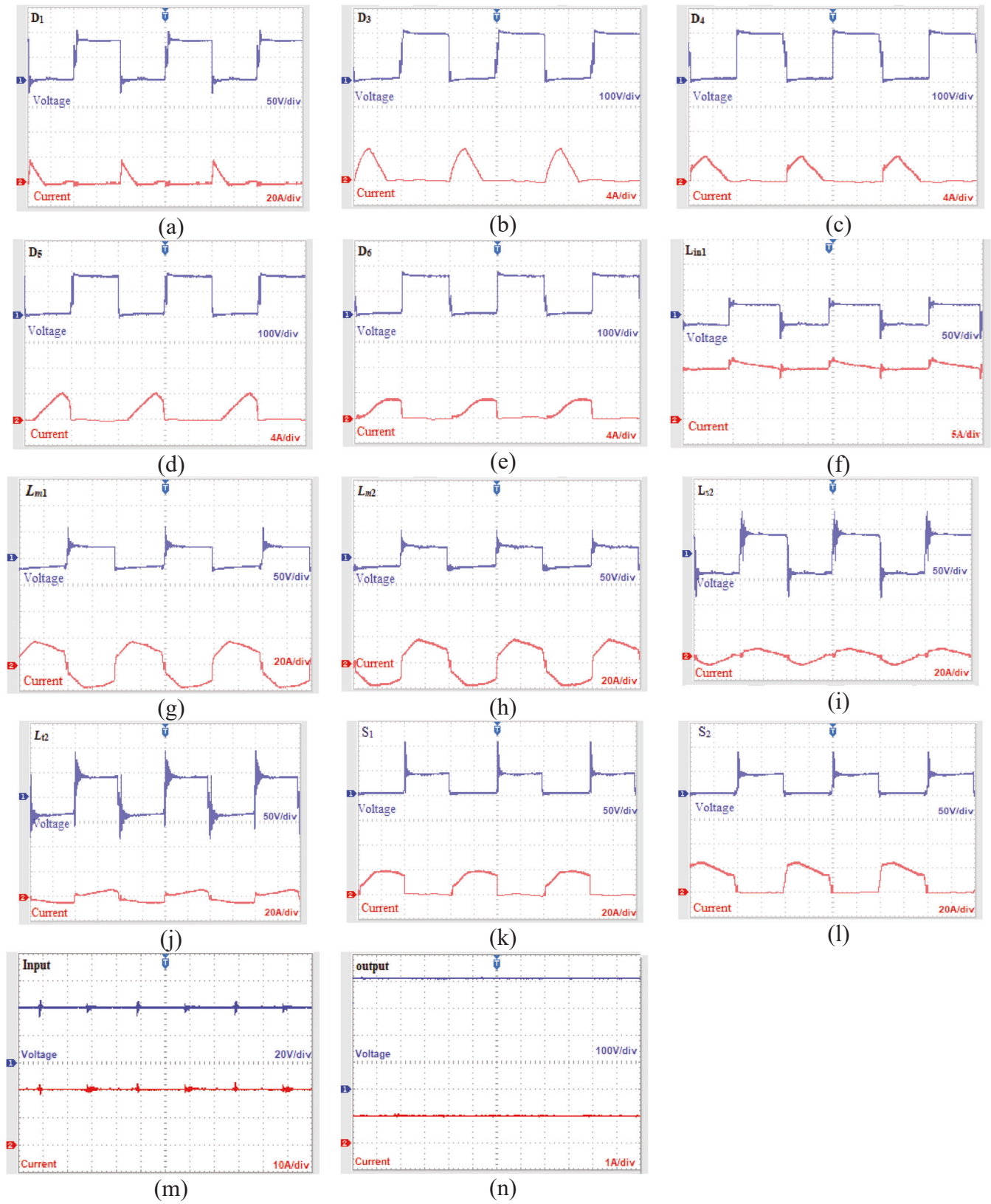
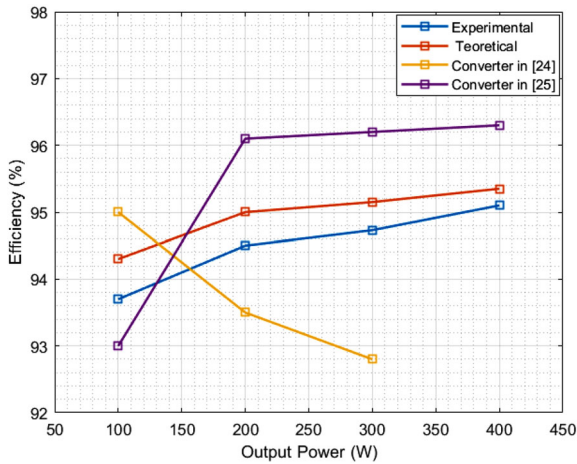


FIGURE 10 Experimental results of the proposed topology; voltages and currents across diodes ((a) D_1 , (b) D_3 , (c) D_4 , (d) D_5 , and (e) D_6), (f) voltage and current of inductance L_{m1} , (g) primary voltage and current of the first CI, voltage and current of the second CI ((h) primary, (i) secondary, and (j) tertiary), voltage and current of active switches ((k) S_1 , and (l) S_2), (m) input voltage and current, and (n) output voltage and current

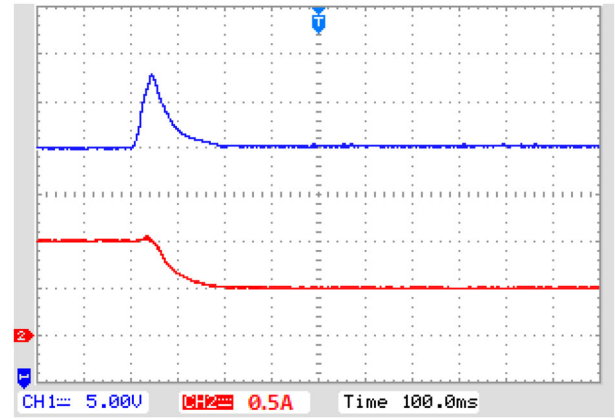
TABLE 4 Developed prototype circuit parameters

Parameters	Description/value
Switches:	HY3912 MOSFET,
S_1, S_2	6.3 m Ω on-resistance
Diodes: D_1	STPS40H100CW Schottky diode, $V_F = 0.58$ V
D_2, D_3, D_4, D_5, D_6	MBR20200CT Schottky diode, $V_F = 0.78$ V
Magnetic coupled Inductor 1 & 2	Turns ratio: 2 ($N_1:N_2 = 20:40$) 2 ($N_1:N_3 = 20:40$) Core: ETD 49/25/16 Ferrite core Magnetizing inductance: 130 μ H With PSTPST winding Leakage inductance :1 μ H
Inductors:	100 μ H, 22 turns wrapped on double T131-52 iron powder core
L_{in1}, L_{in2}	
Capacitors:	
C_1, C_3	10 μ F, 250 V (MKT)
C_2	6.8 μ F, 250 V (MKT)
C_4	470 μ F, 400 V
C_{r1}, C_{r2}, C_5, C_6	10 μ F (MKT)
Switching frequency	50 KHz
Output power	400 W
Input voltage	20 V
Nominal gain	20.5

**FIGURE 11** The suggested converter's efficiency curve for various load circumstances

the spikes further on the switches or diodes. Input voltage and current are shown in Figure 10m in comparison with those of measured output voltage and current in Figure 10n. Experimental outcomes confirm the analytical waveforms depicted in Figure 3 according to the different modes of operation.

The suggested converter's efficiency is evaluated at various power levels, as illustrated in Figure 11. At half load, the maximum converter efficiency is around 94.51%, and at full load,

**FIGURE 12** Output voltage and current in step load change

it is approximately 95.1%. Finally, based on the data presented above, it is clear that the suggested converter is capable of obtaining a high voltage gain without the requirement to work at high duty values. Although the efficiency of the converter suggested in [25] is slightly higher than the efficiency of the proposed converter, its voltage gain is lower and the normalized voltage stress is higher on its components.

Figure 12 shows the output voltage and current when the output load changes from 100% to 50% of its nominal value (i.e. from 400 to 200 W, as a step change). It can be seen from Figure 12 that the output voltage is 410 V with an 8 V overshoot (totally about 418 V), where the output current changes from about 1 to 0.5 A.

7 | CONCLUSION

This paper suggests a high step-up DC–DC converter with a significantly high voltage conversion ratio. By using low size and small resonance capacitors, we have an excellent soft switching operation for the active power switches. Two three-windings CI with voltage multiplier cells are used to achieve an ultra-high voltage gain. The DC–DC topology is based on a two-phase interleaved architecture that includes one CI per phase, a voltage boost capacitor C_1 , and two voltage multiplier networks linked throughout the secondary and tertiary windings. A laboratory 400 W prototype has been implemented to verify analytical descriptions of the suggested design with those of experimental outcomes, confirming the proposed converter operates with an efficiency of 95.32% under full load condition. Significantly, this DC–DC converter is capable of producing a voltage gain of 20.5 at a duty cycle of $D = 0.5$ and turn ratios $n_{21} = n_{31} = n_{22} = n_{32} = 2$ for both CIs. The current ripples amplitude at the input side decreases considerably since the suggested topology employs an interleaved structure with the ability of phase-shift between the interleaved legs. Moreover, the MOSFETs were only exposed to voltage stress of about 13% of the output voltage, introducing low on-resistance low conduction losses for the two switches.

AUTHOR CONTRIBUTIONS

S.A.: Conceptualization; Data curation; Investigation; Software; Supervision. M.F.: Data curation; Formal analysis; Investigation; Software; Validation. M.T.B.: Conceptualization; Formal analysis; Methodology; Supervision; Writing—review and editing. A.A.: Conceptualization; Methodology; Writing—review and editing. A.S.: Conceptualization; Data curation; Investigation; Methodology; Supervision; Writing—original draft; Writing—review and editing

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CONFLICT OF INTEREST

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

Data gathered from simulations that taken place by authors, and no conflict of interest.

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