

Matrix Coupled All-in-One Magnetics for PWM Power Conversion

Ping Wang, *Student Member, IEEE*, Daniel Zhou, *Student Member, IEEE*, Youssef Elasser, *Student Member, IEEE*, Jaeil Baek, *Member, IEEE*, and Minjie Chen, *Senior Member, IEEE*

Abstract—This paper investigates the matrix coupled “all-in-one” magnetic structure that combines both series coupling and parallel coupling for pulse-width-modulated (PWM) power conversion. A systematic analysis of the current ripple reduction mechanism is performed. Current ripple steering among asymmetric series coupled windings is discussed. The transient performance of the matrix coupled inductor is demystified, providing insights for analyzing converter dynamics and large- or small-signal modeling. To quantify the benefits of matrix coupling, a figure of merit is defined by comparing the current ripple of a matrix coupled inductor to that of a discrete inductor given the same transient speed. The comparison results indicate that a higher number of phases and a stronger matrix coupling coefficient amplify the benefits of matrix coupling. A 1 V-to-5 V input, 1 V-to-5 V output, four-phase matrix coupled synchronous SEPIC converter with planar PCB integrated magnetics is built and tested. The matrix coupled SEPIC prototype can support load current up to 185 A at 5 V-to-1 V voltage conversion with a maximum power density over 470 W/in³. Compared to commercial discrete inductors, the matrix coupled inductor has a 5.6 times smaller size and 8.5 times faster transient speed with similar current ripple and current rating. The experimental results validate the matrix coupling concept and the theoretical analysis, opening the possibilities toward wide adoption of “All-in-One-Magnetics” in PWM topologies.

Index Terms—Coupled inductor, inductance dual model, multiphase interleaving, integrated magnetics, current ripple reduction, PWM converter, SEPIC converter.

I. INTRODUCTION

MAGNETIC components, including inductors and transformers, play critical roles in power electronics converters. They can provide various functions such as filtering, galvanic isolation, voltage conversion, etc. Traditionally, magnetic components of different functions are implemented individually as discrete components, taking up a large portion of the converter volume. Coupling multiple inductors and transformers with a shared magnetic core offers reduced magnetic size and loss, increased level of integration, higher converter efficiency, and higher power density [2]–[7].

There are two fundamental ways of coupling magnetic components: series coupling and parallel coupling [8], each

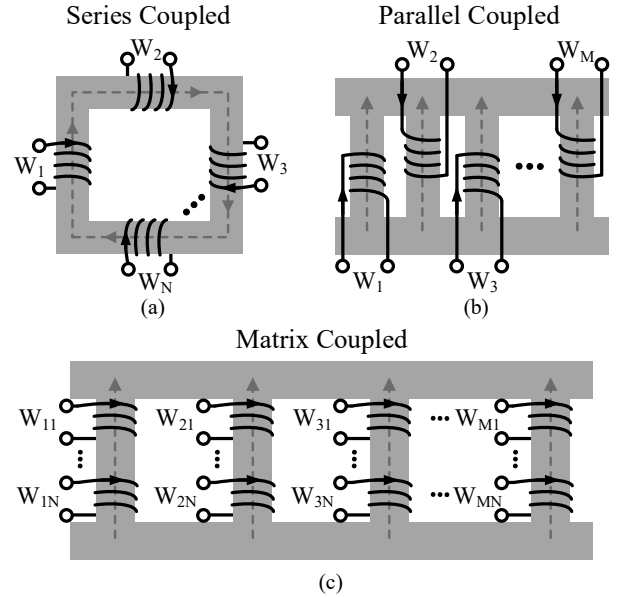


Fig. 1. Coupled magnetic structures: (a) series coupled; (b) parallel coupled; (c) matrix coupled.

offering distinct advantages in reducing current ripple and magnetic size for power converters. In the series coupled magnetic structure, windings with in-phase voltages are coupled by a serial flux linkage, as shown in Fig. 1a. Examples are multi-winding transformers and series coupled inductors. For the multi-winding transformer, cross-sectional area of the magnetic core doesn't scale up with the winding count, but depends on the maximum volt-second-per-turn of all the windings [9]–[14]. The total VA power rating scales faster than the transformer volume [2]. Thus, integrating many transformers into a single multi-winding transformer with the same total power rating can reduce the overall transformer size. For the series coupled inductor, winding current ripple can be reduced given the same self inductance. It has been successfully implemented in lots of topologies such as Ćuk, SEPIC, and tapped-inductor buck or boost converters, and has been proven to offer improved efficiency, reduced converter size, and more benign control characteristics [15]–[19]. Moreover, by adjusting the leakage inductance and turns ratio, current ripples can be steered among the series coupled windings [15], [16]. With appropriate configuration, current ripples on specific windings can be significantly decreased, even to zero, which is beneficial to ripple-sensitive applications like microprocessor power supplies [20].

Figure 1b plots the parallel coupled magnetic structure,

This paper is an extension of a prior conference paper, “Matrix Coupled All-in-One Magnetics for PWM Power Conversion” in *Proc. IEEE COMPEL* 2021 [1]. (Corresponding Author: Minjie Chen.)

P. Wang, D. Zhou, Y. Elasser, J. Baek, and M. Chen are with the Department of Electrical and Computer Engineering and Andlinger Center for Energy and the Environment at Princeton University, Princeton, NJ 08540, USA (e-mail: ping.wang, minjie@princeton.edu).

This work was jointly supported by pSemi Corporation, the NSF CAREER award (#1847365), and the DOE ARPA-E CIRCUITS Program (DE-AR0000906).

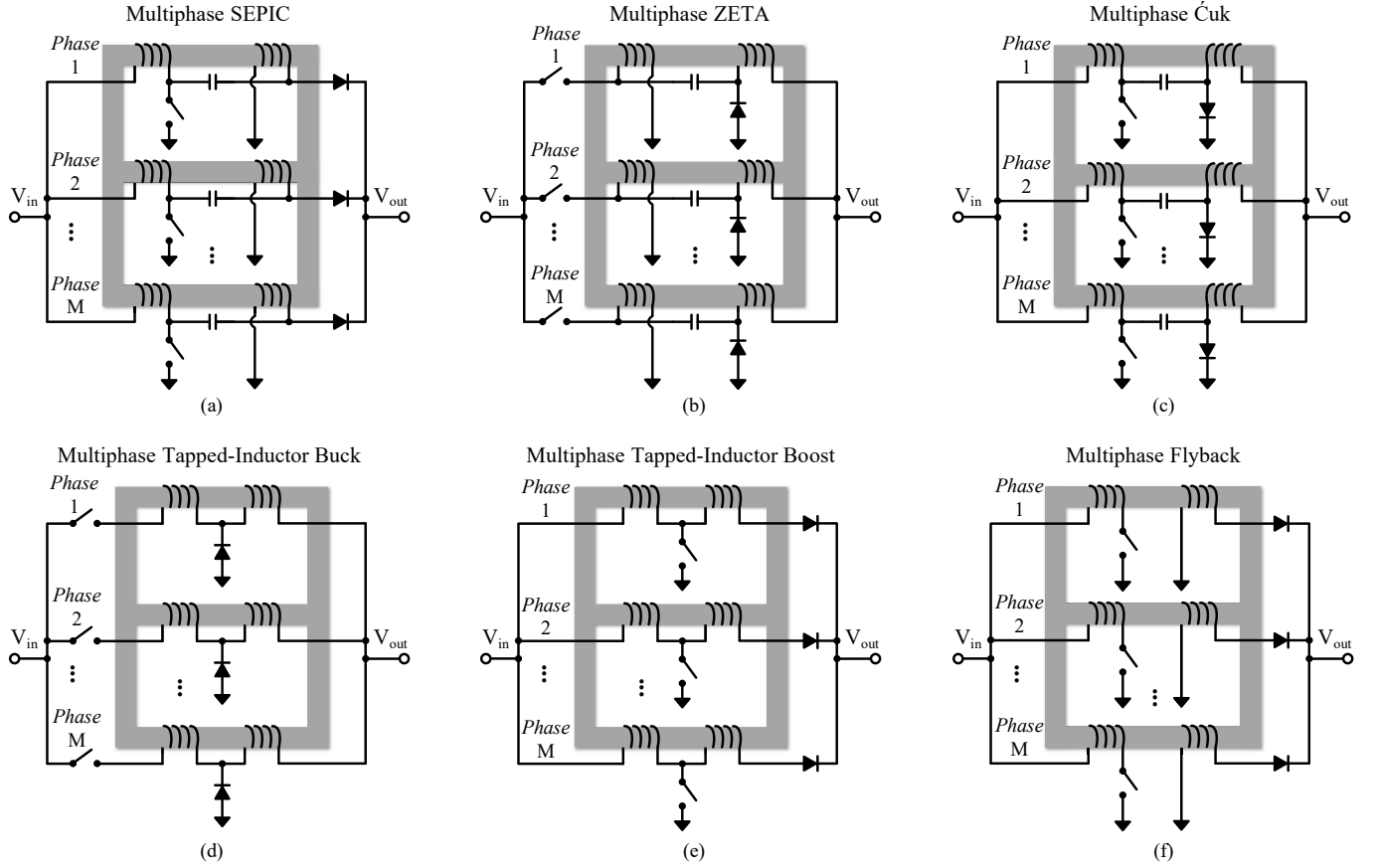


Fig. 2. Example PWM topologies that may apply matrix coupled magnetics: (a) multiphase SEPIC; (b) multiphase ZETA; (c) multiphase Ćuk; (d) multiphase tapped-inductor buck; (e) multiphase tapped-inductor boost; (f) multiphase flyback.

where windings on multiple core legs are coupled by parallel flux linkages. Parallel coupled inductors are widely used in interleaved multiphase topologies [21]–[30]. In these converters, interleaved winding voltages lead to ripple cancellation between winding currents. The resulting reduced current ripples in all circuit components (switches, inductors, capacitors, etc.) and PCB traces decrease power losses and extend the operation range of continuous-conduction mode (CCM). In parallel coupling with equally-shared phase currents, magnetomotive forces (MMF) from parallel coupled windings cancel each other. Almost entire dc inductive energy is stored in leakage fluxes. Due to current ripple reduction, small leakage inductance is allowed, which can reduce total energy storage and boost transient performance [24]–[31]. Since the majority of dc fluxes are leakage fluxes that flow through high reluctance paths, current saturation ratings are greatly improved.

This paper presents a matrix coupled magnetic structure that combines both series coupling and parallel coupling, as shown in Fig. 1c. Motivations for merging multiple discrete magnetics into one origin from their voltage relationships – magnetics with in-phase voltages can be coupled in series on the same core leg, while magnetics with interleaved voltages can be coupled on parallel core legs. Benefiting from both series and parallel couplings as well as interleaving, matrix coupled magnetics can achieve miniaturized magnetic size and inductive energy storage, reduced current ripple and power loss, and improved transient response. Similar coupled

magnetics applied in current doubler rectifier [32], [33], dual flyback [34], multiphase LLC [35], and cross commutated buck converters [36] are a subset of the generalized matrix coupled magnetic structure presented in this paper. A systematic analysis of the current ripple reduction mechanism is performed, revealing the fundamental benefits of matrix coupling. The transient performance of matrix coupled inductors is demystified, providing guidance on large- and small-signal modeling. A figure of merit (FOM) based on current ripple and transient performance is defined to quantify the benefits obtained from matrix coupling.

To validate the matrix coupled magnetic structure and theoretical analysis, a four-phase matrix coupled synchronous SEPIC converter with planar PCB integrated magnetics is designed and tested. The prototype measures 0.392 in^3 in volume and is capable of flexibly delivering power from 1~5 V input to 1~5 V output. At 5 V-to-1 V voltage conversion, the prototype can support load current up to 185 A with power density over 470 W/in^3 . Compared to discrete commercial inductors of similar current ratings and ripples, the matrix coupled inductor reduces the magnetic component size by over 5.6 times and increases the transient speed by over 8.5 times.

In the remainder of this paper, Section II demonstrates several example PWM topologies that may apply matrix coupled magnetics. Section III performs a systematic analysis of current ripple reduction for matrix coupled magnetics. Section IV reveals the transient performance, quantifies the

matrix coupling benefits, and provides insights for large- and small-signal modeling. Section V details the design of a four-phase matrix coupled synchronous SEPIC prototype. Experimental verifications are summarized in Section VI. Finally, Section VII concludes this paper.

II. EXAMPLE PWM TOPOLOGIES WITH MATRIX COUPLED MAGNETICS

Matrix coupled magnetics are generally applicable to power converters that have both in-phase and interleaved voltage relationships between magnetic components. In-phase voltages motivate series coupling to reduce cross-sectional core area, and interleaved voltage excitations motivate parallel coupling to reduce ac current ripples. Typical examples are multiphase, multi-order PWM converters [37], as shown in Fig. 2.

Figures 2a-2c plot a series of multiphase buck-boost topologies (SEPIC, ZETA, and Ćuk) with matrix coupled inductors. Each topology contains two inductors and one capacitor per phase. Given that the capacitor maintains stable dc voltage, two inductors of each phase have identical square wave voltages and thus are coupled in series on the same core leg. Many phases on different core legs are coupled in parallel and are operated in interleaving. Figures 2d-2e plot some multiphase tapped-inductor topologies, where two windings of each tapped inductor are originally series coupled. The turns ratio can be adjusted to enlarge voltage conversion ratio, but in-phase square wave voltages are always applied to the series coupled windings. Through parallel coupling and multiphase interleaving, ac current ripples on the tapped inductors are decreased, enabling the use of a smaller magnetic core with faster transient speed. Figure 2f shows an isolated matrix coupled converter based on flyback topology. In the flyback converter, transformer windings are coupled in series. While providing the functions of galvanic isolation and voltage conversion, the transformer also needs to store energy due to dc magnetizing current. Applying matrix coupling and interleaving operation to the multiphase flyback converter can help reduce the required energy storage in the transformer.

Matrix coupled converters in Fig. 2 are constructed based on identical switching converter cells connected in parallel. One can also combine multiple switching cells of different types into a composite converter [38] or sigma converter [39] to leverage the resulting mutual advantages.

III. CURRENT RIPPLE REDUCTION MECHANISM OF MATRIX COUPLED MAGNETICS

This section systematically analyzes the current ripple reduction mechanism of the matrix coupled magnetics when operated under PWM voltage excitations. Fundamental ripple reduction benefits from both parallel and series couplings are revealed. The analysis is first performed based on symmetric matrix coupling structures where series coupled windings of each phase have the same voltages, winding turns, and leakage reluctance and winding configurations across parallel coupled phases are identical. Matrix coupling structures are then generalized as asymmetric series coupling plus symmetric parallel coupling, in which the above-mentioned quantities

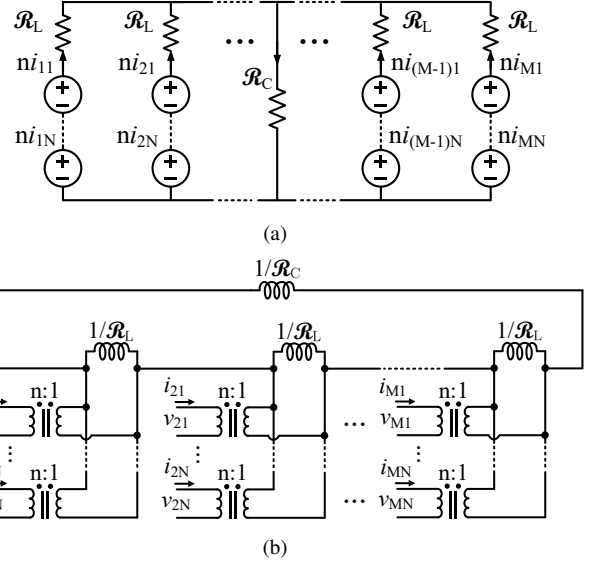


Fig. 3. Equivalent magnetic models for the matrix coupled magnetics: (a) magnetic circuit model; (b) inductance dual model.

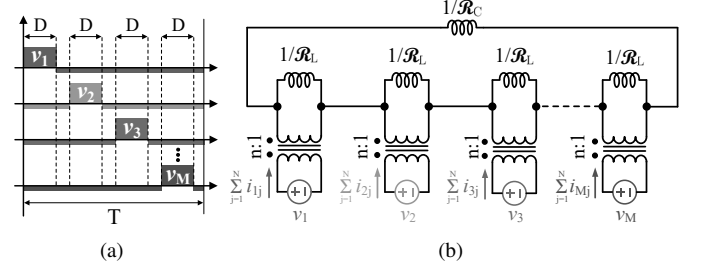


Fig. 4. (a) Interleaved winding voltages for parallel phases. (b) Modified inductance dual model where windings of each phase are combined as one port delivering the summed currents into the inductance network.

may vary across series coupled windings, but parallel phases are still identical. In this case, current ripples can be steered among the series coupled windings. Although asymmetric parallel coupling is not elaborated in this paper, it shares the same ripple reduction principles and benefits as the symmetric cases. The discussed conditions herein already cover most of the matrix coupling applications, especially the multiphase topologies. Following current ripple analysis is based on CCM operation, but related analysis in discontinuous-conduction mode (DCM) can emulate the procedures presented below.

A. Phase Current Ripple Reduction by Parallel Coupling and Multiphase Interleaving

Assume the matrix coupled magnetic component in Fig. 1c contains M parallel core legs, and on each leg are wound N series coupled windings. Figure 3a plots its equivalent magnetic circuit model [40]. Each core leg is modeled as a circuit branch with a leg reluctance \mathcal{R}_L and N MMF sources. Given that parallel coupled phases are symmetric, the leakage fluxes between phases can be modeled as a central branch with an equivalent reluctance \mathcal{R}_C . Applying topological duality to the magnetic circuit model leads to the inductance dual model [41]–[44], as shown in Fig. 3b. In the inductance dual

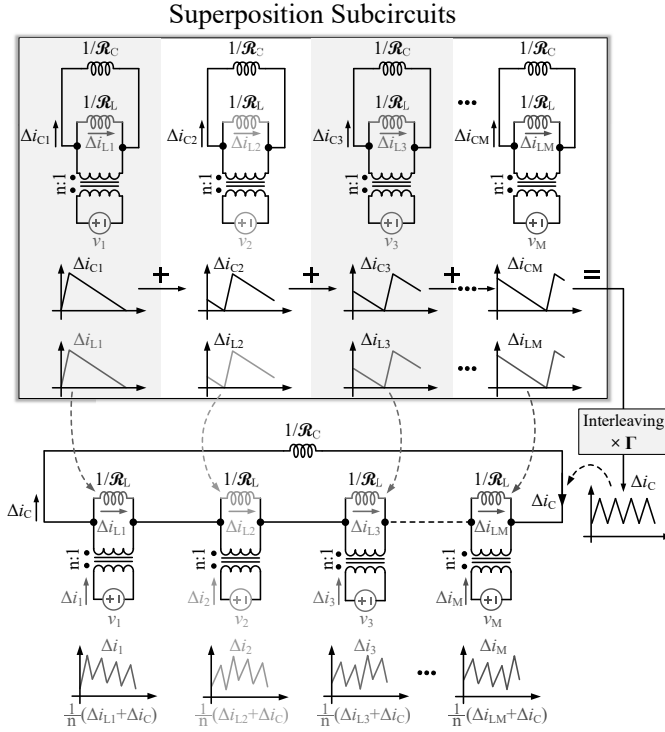


Fig. 5. Detailed superposition procedures for phase current ripple analysis.

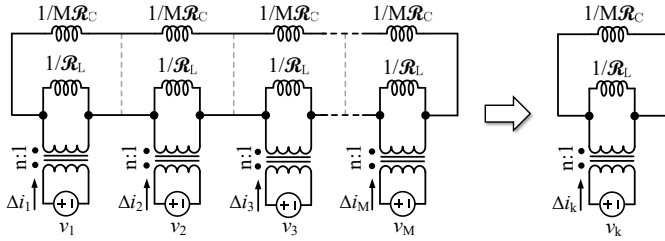


Fig. 6. Equivalent inductance dual model per phase for non-interleaved voltage excitations.

model, effective resistance can be further added in parallel with $1/\mathcal{R}_C$ and $1/\mathcal{R}_L$ to capture the core loss of each portion of the magnetic core, or in series at each port to capture the winding conduction loss [8]. In a well-designed magnetic component, these effective resistors are usually small enough and have negligible impacts on the current ripple. Thus, they are ignored in the analysis below.

As a start, symmetric series coupling with the same winding voltages and number of turns (denoted as n) is considered. Cases with unmatched voltages or number of turns can be converted back to Fig. 3b as long as the series coupled windings have the same voltage-per-turn. More general cases allow unmatched voltage-per-turn for series coupling and are discussed later in Section III-C. In the case of symmetric coupling, series coupled windings driven by identical voltages can be combined as one port delivering the summed winding currents into the inductance network, as shown in Fig. 4b. Summed current ripple of each phase is related to all the voltage excitations v_1, \dots, v_M , which become phase-shifted square wave voltages (in Fig. 4a) under multiphase interleaved

operation. We analytically derive the current ripple based on superposition. Figure 5 illustrates the key steps of the superposition analysis. Denote the summed winding current ripple in the k^{th} phase as Δi_k . Interleaved voltage excitations v_1, \dots, v_M have identical voltage patterns so that their positive volt-second integrals of one cycle are the same (denoted as σ). M superposition subcircuits are created. In each subcircuit, the square wave voltage results in triangular ac currents in the two parallel inductors, and their peak-to-peak ripple values are:

$$(\Delta i_{Lk})_{pp} = \frac{\sigma \mathcal{R}_L}{n}, \quad (\Delta i_{Ck})_{pp} = \frac{\sigma \mathcal{R}_C}{n}. \quad (1)$$

In the inductance dual model, each branch inductor ($1/\mathcal{R}_L$) is only excited by its parallel voltage source, while the shared inductor ($1/\mathcal{R}_C$) is excited by all voltage sources. The overall shared inductor current ripple (Δi_C) is the summation of the interleaved triangular current ripples (Δi_{Ck}) in all subcircuits, so its peak-to-peak current ripple is:

$$(\Delta i_C)_{pp} = \left(\sum_{k=1}^M \Delta i_{Ck} \right)_{pp} = \frac{\Gamma M \sigma \mathcal{R}_C}{n}, \quad (2)$$

where Γ is the ripple cancellation ratio of the summed interleaved triangular currents [8]:

$$\Gamma = \frac{(k+1-DM)(DM-k)}{(1-D)DM^2}, \quad \text{for } \frac{k}{M} \leq D < \frac{k+1}{M}. \quad (3)$$

Since Δi_C and Δi_{Lk} are synchronized to the PWM switching clock, summing their peak-to-peak values results in the peak-to-peak ripple of Δi_k for the interleaved operation:

$$\begin{aligned} (\Delta i_k)_{pp}^{\text{interleaved}} &= \frac{1}{n} ((\Delta i_C)_{pp} + (\Delta i_{Lk})_{pp}) \\ &= \frac{\sigma (\Gamma M \mathcal{R}_C + \mathcal{R}_L)}{n^2}. \end{aligned} \quad (4)$$

If the M phases are not interleaved and driven by synchronized voltage excitations, the inductance dual model can be equivalent to multiple standalone ones as shown in Fig. 6. Then the peak-to-peak ripple of Δi_k becomes

$$(\Delta i_k)_{pp}^{\text{non-interleaved}} = \frac{\sigma (M \mathcal{R}_C + \mathcal{R}_L)}{n^2}. \quad (5)$$

Define the parallel coupling coefficient as $\beta = M \mathcal{R}_C / \mathcal{R}_L$. A higher β indicates a stronger parallel coupling. Define the ratio between the peak-to-peak values of Δi_k with interleaved and non-interleaved operations as γ :

$$\gamma \stackrel{\text{def}}{=} \frac{(\Delta i_k)_{pp}^{\text{interleaved}}}{(\Delta i_k)_{pp}^{\text{non-interleaved}}} = \frac{(\Gamma M \mathcal{R}_C + \mathcal{R}_L)}{(M \mathcal{R}_C + \mathcal{R}_L)} = \frac{1 + \beta \Gamma}{1 + \beta}. \quad (6)$$

The analysis above reveals that the benefits of parallel coupling fundamentally come from multiphase interleaving. Similar conclusion is drawn from a different perspective in [8]. If parallel-coupled phases are operated in a non-interleaved manner, they are equivalent to multiple discrete inductors of $\frac{n^2}{M \mathcal{R}_C + \mathcal{R}_L}$, as indicated by Fig. 6. In this case, phase current ripples, power losses, magnetic energy storage, and transient speed are all the same as the discrete ones. Only if the parallel phases are both coupled and interleaved, the phase current ripple is reduced by a factor of γ , which is determined by

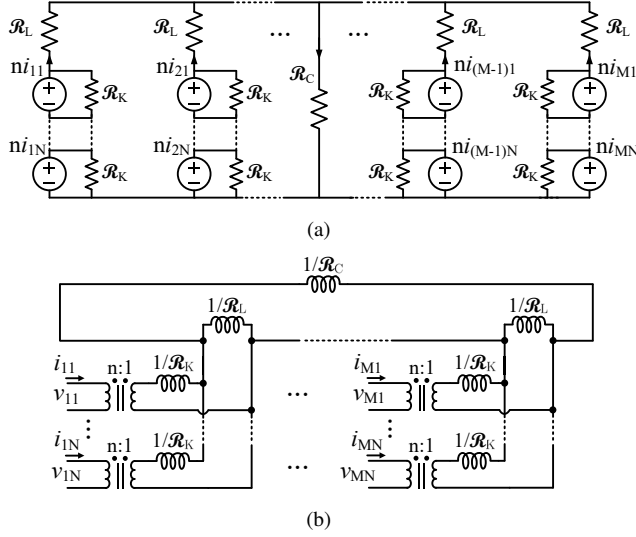


Fig. 7. Magnetic models when considering leakage inductance between series coupled windings on each core leg: (a) magnetic circuit model; (b) inductance dual model.

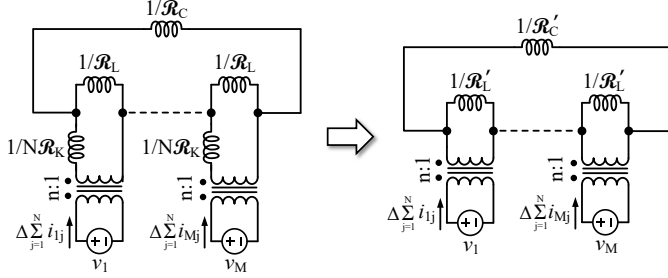


Fig. 8. Mapping the inductance dual model back to the one without \mathcal{R}_K .

β and Γ . As implied by (6), with a strong parallel coupling coefficient (i.e., $\beta \rightarrow \infty$), γ approaches Γ . If the coupling is weak (i.e., $\beta \rightarrow 0$), γ reduces to one, and then no ripple reduction is achieved.

B. Impacts of Series Coupling on Winding Current Ripple Reduction

Equation (6) reveals the benefits of parallel coupling assuming the series coupled windings are perfectly coupled. To capture the impact of non-ideal series coupling, the leakage flux between windings on the same core leg is modeled as a leakage reluctance (\mathcal{R}_K) in parallel with each MMF source as shown in Fig. 7a. In the inductance dual model of Fig. 7b, the parallel leakage path is then converted to a series leakage inductance ($1/\mathcal{R}_K$) at each port. Define the series coupling coefficient as $\alpha = N\mathcal{R}_K/\mathcal{R}_L$. We analyze the current ripple under the impacts of series coupling by mapping its inductance dual model (in Fig. 7b) back to the one without leakage inductance \mathcal{R}_K (in Fig. 3b). The mapping process is illustrated in Fig. 8 with parameter mapping described as:

$$\text{(Fig. 7b)} \quad \begin{bmatrix} \mathcal{R}_L \\ \mathcal{R}_C \\ \mathcal{R}_K \\ \alpha \\ \beta \end{bmatrix} \xrightarrow{\text{Parameter Mapping}} \begin{bmatrix} \mathcal{R}'_L \\ \mathcal{R}'_C \\ \beta' \end{bmatrix} \text{(Fig. 3b).} \quad (7)$$

TABLE I
KEY PARAMETERS OF CURRENT RIPPLE ANALYSIS
FOR SYMMETRIC MATRIX COUPLING

Series Coupling Coefficient	$\alpha = \frac{N\mathcal{R}_K}{\mathcal{R}_L}$
Parallel Coupling Coefficient	$\beta = \frac{M\mathcal{R}_C}{\mathcal{R}_L}$
Matrix Coupling Coefficient	$K_{\alpha\beta} = \frac{\alpha\beta}{1+\alpha+\beta}$
Current Ripple Reduction Ratio	$\gamma = \frac{1+K_{\alpha\beta}\Gamma}{1+K_{\alpha\beta}}$
$(\Delta i_k)_{pp}^{non-interleaved}$	$\frac{\sigma((M\mathcal{R}_C + \mathcal{R}_L) N\mathcal{R}_K)}{n^2}$
$(\Delta i_k)_{pp}^{interleaved}$	$\gamma \times (\Delta i_k)_{pp}^{non-interleaved}$
$(\Delta i_{winding})_{pp}^{interleaved}$	$\frac{1}{N} (\Delta i_k)_{pp}^{interleaved}$

Since the two inductance dual models in Fig. 8 are equivalent and should have the same impedance matrix, the parameter mapping relationship can be obtained as

$$\begin{cases} \mathcal{R}'_L = \mathcal{R}_L || N\mathcal{R}_K \\ M\mathcal{R}'_C = (\mathcal{R}_L + M\mathcal{R}_C) || N\mathcal{R}_K - \mathcal{R}_L || N\mathcal{R}_K \\ K_{\alpha\beta} \stackrel{\text{def}}{=} \beta' = \frac{M\mathcal{R}'_C}{\mathcal{R}'_L} = \frac{\alpha\beta}{1+\alpha+\beta} \end{cases} \quad (8)$$

$K_{\alpha\beta}$, determined by α and β , is the matrix coupling coefficient, which describes the overall coupling strength among all the windings in the matrix coupled magnetics. After model mapping, phase current ripple and its reduction ratio when considering the series coupling coefficient can be analyzed in the same way as in Section III-A.

Table I lists the summarized parameters of the current ripple analysis for symmetric matrix coupling. Here, impacts of both the series and parallel coupling coefficients are included. As indicated by Table I, compared to the non-interleaved operation, multiphase interleaving can reduce the peak-to-peak phase current ripple by a factor of γ . The phase current ripple $((\Delta i_k)_{pp}^{interleaved})$ is the summation of winding current ripples in each phase and will be equally split across the series coupled windings if they have the same leakage inductance ($1/\mathcal{R}_K$). In this case, γ is also the current ripple reduction ratio for each winding current:

$$\frac{(\Delta i_{winding})_{pp}^{interleaved}}{(\Delta i_{winding})_{pp}^{non-interleaved}} = \frac{(\Delta i_k)_{pp}^{interleaved}}{(\Delta i_k)_{pp}^{non-interleaved}} = \gamma \quad (9)$$

A higher α or β results in a higher $K_{\alpha\beta}$ so that γ will be lower. Therefore, both strong series coupling and parallel coupling are preferred in order to achieve lower current ripples and larger benefits for matrix coupled magnetics.

C. Asymmetric Series Coupling and Current Ripple Steering

The above analysis is based on symmetric series coupling when all windings are continuously conducting. In some applications, however, series coupled windings can have different turns ratio and voltages (e.g., tapped-inductor topologies) or intermittent winding currents caused by switching behaviors (e.g., flyback topology). If certain windings are disconnected

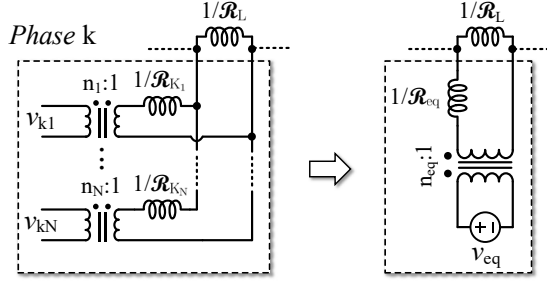


Fig. 9. Generalized series coupled winding configuration in the k^{th} phase and its Thevenin-equivalent network.

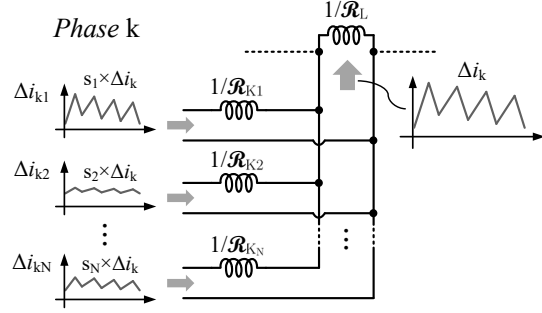


Fig. 10. Current ripple steering among the series coupled windings in the k^{th} phase. If the windings have identical volt-per-turn, the phase current ripple Δi_k will be linearly divided into each winding by a steering coefficient s_j .

due to switching, current ripples will be distributed among the other conducting windings, but the summed current ripple of each phase still follows the analysis above as long as the voltage relationships are always applied. Therefore, without loss of generality, we assume all the windings are always conducting. Figure 9 plots a generalized inductance dual model referring to the series coupled windings in the k^{th} phase. Winding voltage v_{kj} , turns ratio n_j , and leakage inductance $1/\mathcal{R}_{Kj}$ are all independent. As shown in the figure, the multi-source inductance network can be converted to a single-source Thevenin-equivalent network with equivalent quantities as:

$$\mathcal{R}_{eq} = \sum_{j=1}^N \mathcal{R}_{Kj}, \quad v_{eq} = \frac{n_{eq}}{\mathcal{R}_{eq}} \sum_{j=1}^N \frac{\mathcal{R}_{Kj} v_j}{n_j}. \quad (10)$$

n_{eq} is a reference turns ratio and can be anyone of $n_1 \sim n_N$. Then the Thevenin-equivalent network can be substituted into the model in Fig. 8, following the same procedures above to get the phase current ripple Δi_k .

For general asymmetric series coupling, how phase current ripple Δi_k is distributed into series coupled windings depends on winding voltage, turns ratio, and leakage inductance. There is no general solution to the winding current ripple. Instead, it needs to be analyzed case by case. However, if all series coupled windings share the same voltage-per-turn, Δi_k will be linearly split into each winding, proportionally to its leakage reluctance \mathcal{R}_{Kj} , as shown in Fig. 10. As explored in [15], there are opportunities to steer the current ripple among series coupled windings by adjusting the leakage reluctance. The steering coefficient and current ripple for the j^{th} winding in

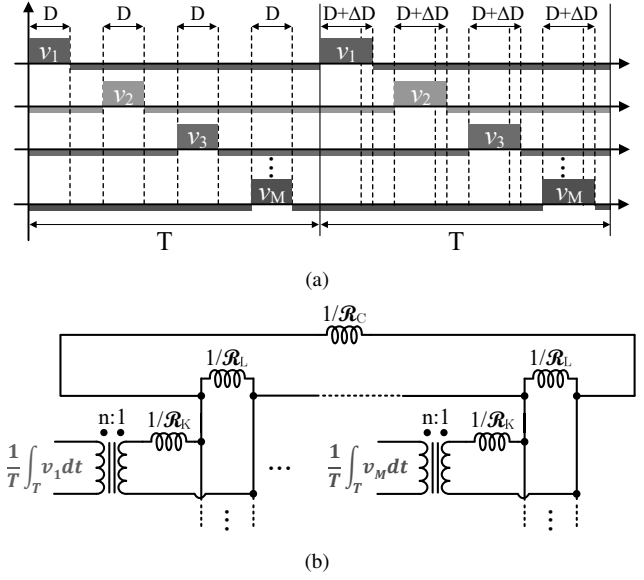


Fig. 11. (a) Duty ratio command for each phase keeps identical during transients. (b) Switching-cycle averaged voltage of each winding is identical.

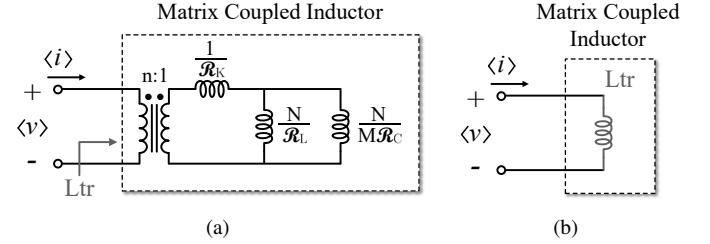


Fig. 12. (a) Switching-cycle averaged model for each winding. (b) Equivalent inductance seen at each winding during transients.

the k^{th} phase are:

$$s_j = \frac{\mathcal{R}_{Kj}}{\sum_{i=1}^N \mathcal{R}_{Ki}}, \quad \Delta i_{kj} = s_j \times \Delta i_k. \quad (11)$$

Equation (11) indicates that, with appropriate adjustment of leakage reluctance, switching current ripples on specific windings can be reduced to nearly zero. Rippleless winding currents can be used at important outputs to supply ripple-sensitive applications or to reduce the filtering capacitor size.

IV. TRANSIENT PERFORMANCE AND FIGURE OF MERIT

Besides the current ripple, another important metric for a matrix coupled inductor is the transient performance, which impacts converter dynamics and control design. The transient performance of the matrix coupled inductor can be analyzed based on switching-cycle averaging. To analytically derive the transient inductance, symmetric matrix coupling is assumed. Asymmetric cases can emulate the analysis below.

In a multiphase PWM converter with the matrix coupled inductor, duty ratios of parallel phases are usually identical. Under the control methods that maintain the same duty ratio for parallel phases during transients, all the windings will always have identical square wave voltages (same amplitude and pulse width), as shown in Fig. 11a. Applying switching-cycle averaging to the inductance dual model (Fig. 11b),

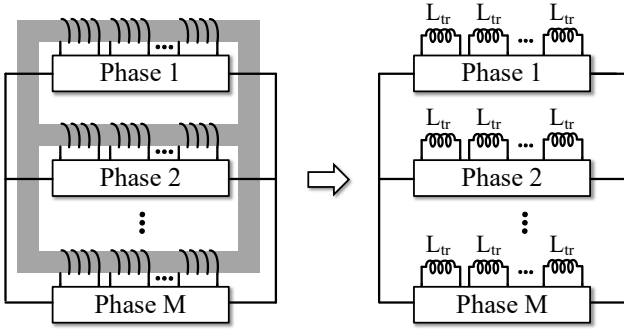


Fig. 13. Switching-cycle averaged dynamics of the converter with the matrix coupled inductor are the same as that with discrete inductors of L_{tr} .

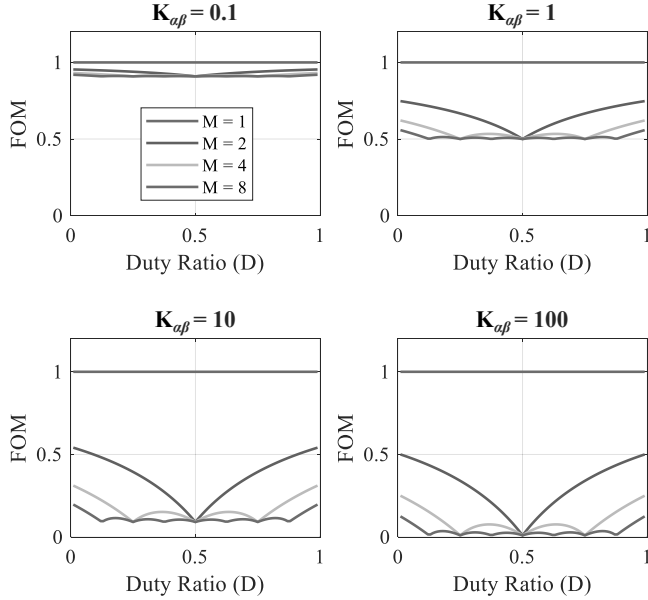


Fig. 14. FOM as a function of duty ratio (D) for various numbers of phases (M) and coupling factors ($K_{\alpha\beta}$).

the averaged winding voltage is the same for each winding, regardless of phase shifts. It indicates that in the switching-cycle averaged model, all the windings are always driven by identical voltage excitations. In this case, each winding can be modeled as an individual inductance network, as shown in Fig. 12a. Therefore, the equivalent inductance seen at each winding during transient (defined as transient inductance L_{tr} in Fig. 12b) is:

$$L_{tr} = \frac{n^2 N}{(M\mathcal{R}_C + \mathcal{R}_L) \|\mathcal{N}\mathcal{R}_K}. \quad (12)$$

L_{tr} determines the transient performance of the matrix coupled inductor under common-mode excitations. A smaller L_{tr} enables the designer to achieve a faster transient response with proper closed loop control [24]. This paper only discusses this common-mode transient inductance, for it is typically used to solve the input or output transient speed and can indicate the scaling trend of the transient performance for matrix coupled magnetics. Transient response for parallel coupled inductors under differential-mode excitations is discussed in [30].

Under common-mode excitations, the averaged component voltages and currents of using the matrix coupled inductor is the same as using discrete inductors L_{tr} . Therefore, the large- and small-signal models can be developed by treating the matrix coupled inductor as multiple discrete L_{tr} , as illustrated in Fig. 13. To quantify the benefits of matrix coupling, a figure of merit (FOM) is defined by comparing the current ripple of a matrix coupled inductor (under interleaved operation) to that of using discrete L_{tr} :

$$\text{FOM} \stackrel{\text{def}}{=} \frac{(\Delta i_{winding})_{pp}^{\text{matrix-coupled}}}{(\Delta i_{winding})_{pp}^{\text{discrete-}L_{tr}}} = \frac{1 + K_{\alpha\beta}\Gamma}{1 + K_{\alpha\beta}} = \gamma. \quad (13)$$

The FOM describes the current ripple reduction ratio of using a matrix coupled inductor compared to using discrete inductors given the same transient performance. A lower FOM indicates a lower current ripple than that of discrete inductors and larger benefits. Accordingly, the effective steady state inductance L_{ss} that has the same steady state current ripple can be expressed as: $L_{ss} = L_{tr}/\gamma$.

Equation (13) also implies that the ripple reduction ratio between using matrix coupled inductor and discrete L_{tr} equals the ripple reduction ratio between interleaved and non-interleaved operations for the matrix coupled inductor itself. This is consistent with the fundamental characteristics of matrix coupling: L_{tr} is in effect the equivalent winding inductance under common-mode voltage excitations, so it is equal to the effective winding inductance when operated by non-interleaved (synchronized) PWM signals. Consequently, current ripple of discrete L_{tr} is the same as that of the matrix coupled inductor under non-interleaved operation, and thus FOM equals γ . Figure 14 plots the FOM as a function of duty ratio with different phase numbers (M) and coupling factors ($K_{\alpha\beta}$). Conclusion can be drawn that a higher number of parallel phases or a stronger matrix coupling coefficient results in lower FOM across the full duty ratio range.

V. PROTOTYPE DESIGN OF A FOUR-PHASE MATRIX COUPLED SYNCHRONOUS SEPIC CONVERTER

A. Matrix Coupled Inductor Design

To validate the matrix coupled magnetic structure and the theoretical analysis, a four-phase matrix coupled synchronous SEPIC converter is designed and built. Figure 16 shows the circuit topology, in which eight discrete PWM inductors are merged into one matrix coupled inductor. The matrix coupled inductor is implemented as planar PCB integrated magnetics utilizing a four-leg planar magnetic core as shown in Fig. 17. The magnetic core is built with Ferroxcube 3F4 material and takes up 12 mm × 13 mm board area. Two core pieces are stacked as an EE-type structure with 5.25 mm total height. The magnetic core is four-way symmetric, allowing for identical parameters across the four phases. Details about this core shape design are provided in [29]. A ladder core structure as presented in [8] is also applicable.

Figure 17b plots the cross-section view of the magnetic core and annotated inductor winding configurations. The labeled winding current directions follow the defined ones in Fig. 16.

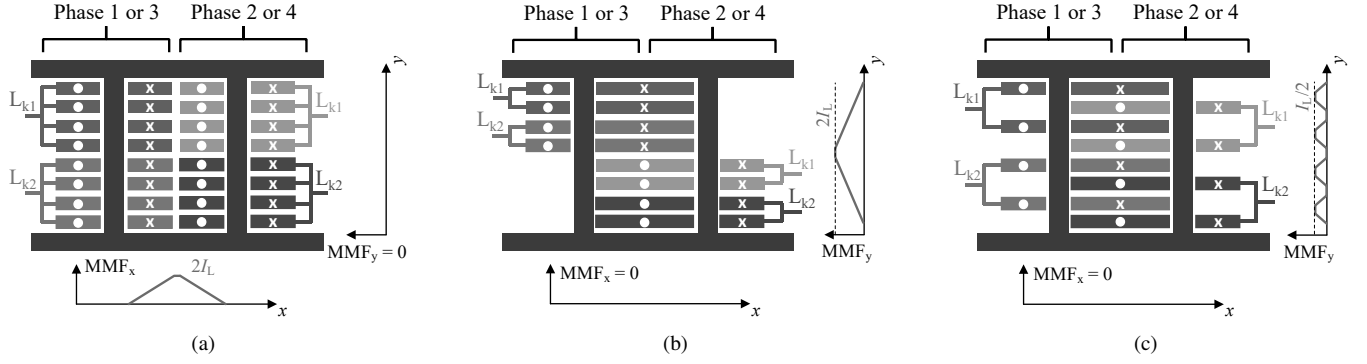


Fig. 15. Alternative winding designs of the matrix coupled inductor based on an 8-layer PCB board of 3-oz copper thickness: (a) side by side; (b) non-interleaved overlapping; (c) interleaved overlapping. Assume each inductor current is I_L . MMF diagrams for windings in the window area are plotted along horizontal and vertical directions.

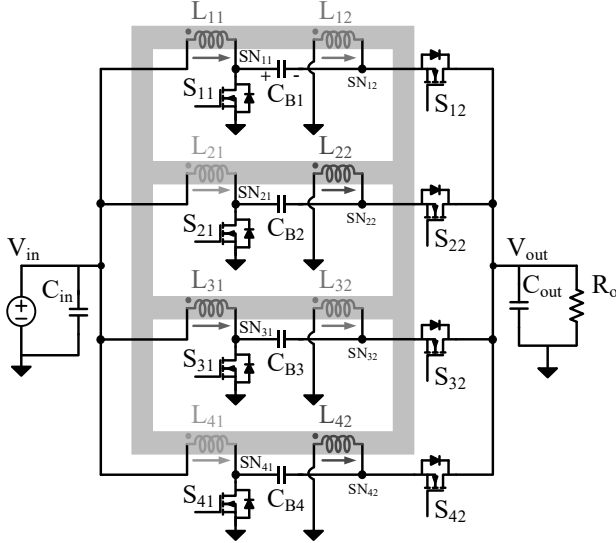


Fig. 16. Circuit topology of the four-phase matrix coupled synchronous SEPIC converter.

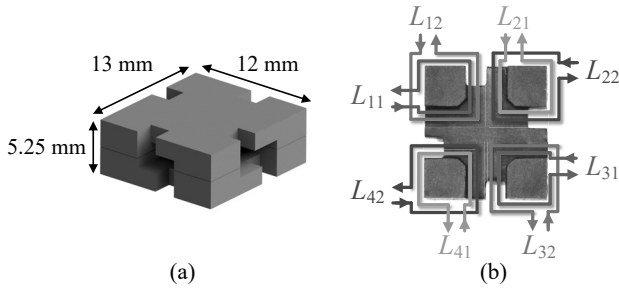


Fig. 17. Four-leg magnetic core built with Ferroxcube 3F4 material: (a) EE-type core structure; (b) cross-section view and inductor winding annotations.

As shown in Fig. 17b, two inductor windings of each phase are wound on the same core leg and their ac currents flow in the same direction, whereas ac winding currents of neighboring phases flow reversely in the shared window area. It might lead to concentrated currents on adjacent conductor surfaces between phases due to the proximity effect. Thus, an appropriate winding design is needed to reduce the ac resistance.

Figure 15 shows three feasible PCB winding designs based on an 8-layer PCB board of 3-oz copper thickness. MMFs of the windings are plotted in both horizontal and vertical directions across the window area. Figure 15a shows a side-by-side winding design, where windings of neighboring phases are placed side by side in the window area. Each inductor comprises four layers of windings connected in parallel and takes up half of the window width. Assume each inductor current is I_L . In the window area, MMFs of two reverse inductor currents on the same layer cancel each other, so the MMF along vertical direction remains zero. Along horizontal direction, the opposite winding currents on the left and right sides enhance the magnetic flux, resulting in a maximum MMF of $2I_L$ in the center. Figure 15b shows a non-interleaved overlapping design, in which windings between phases take up the full window width and are overlapped in the window area. Winding layers between phases are not interleaved but separated into top and bottom halves of the PCB. Each inductor is comprised of two layers of windings connected in parallel. Due to the overlapped windings, MMFs of reverse currents cancel along horizontal axis, but the opposite currents of the top and bottom halves result in a maximum MMF of $2I_L$ in the middle of vertical direction. Figure 15c plots the interleaved overlapping winding design, where windings between neighboring phases are both overlapped in the window area and interleaved across PCB layers. The interleaved winding layers can effectively reduce the MMF along vertical direction. The maximum MMF along vertical direction is $I_L/2$, and MMF along horizontal direction remains zero. Accordingly, the interleaved overlapping winding design maintains low MMFs in both the horizontal and vertical directions.

For the three winding designs in Fig. 15, dc resistance of the windings in the window area is the same, but ac resistance varies. Figures 18 and 19 shows the finite-element-method (FEM) simulations of magnetic field distributions and ac winding current distributions respectively. The simulations are performed by applying a 1-MHz sinusoidal current excitation of 10-A amplitude to each inductor, and eddy current effects are captured for each winding. Since the core has a large permeability $\mu_{core} \gg \mu_0$, the H field of leakage flux in the window area is much higher than in the core. The FEM simulation results are consistent with the MMF analysis in

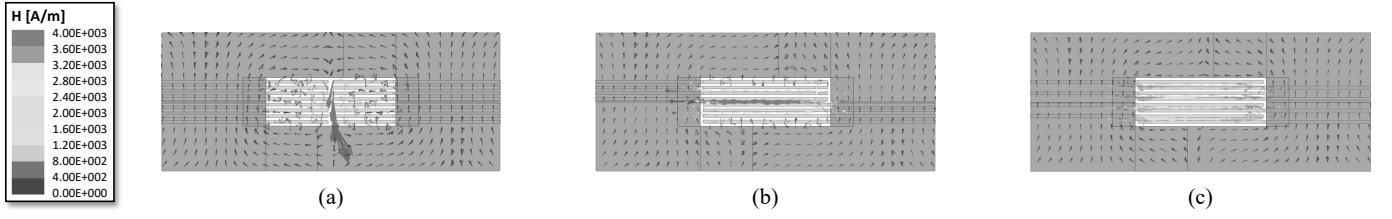


Fig. 18. FEM simulation of magnetic field strength distributions inside core and window area in the designs of (a) side by side; (b) non-interleaved overlapping; (c) interleaved overlapping. Each inductor is driven by a 1-MHz sinusoidal current excitation of 10-A amplitude. Copper thickness and current directions are consistent with Fig. 15.

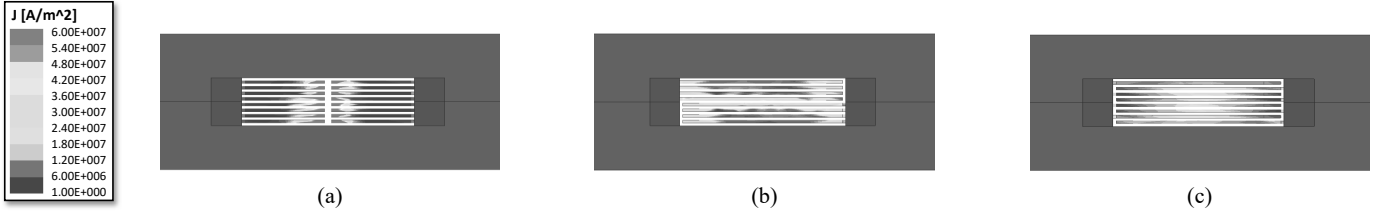


Fig. 19. FEM simulation of ac winding current distributions in the designs of (a) side by side; (b) non-interleaved overlapping; (c) interleaved overlapping. Simulation conditions are the same as in Fig. 18.

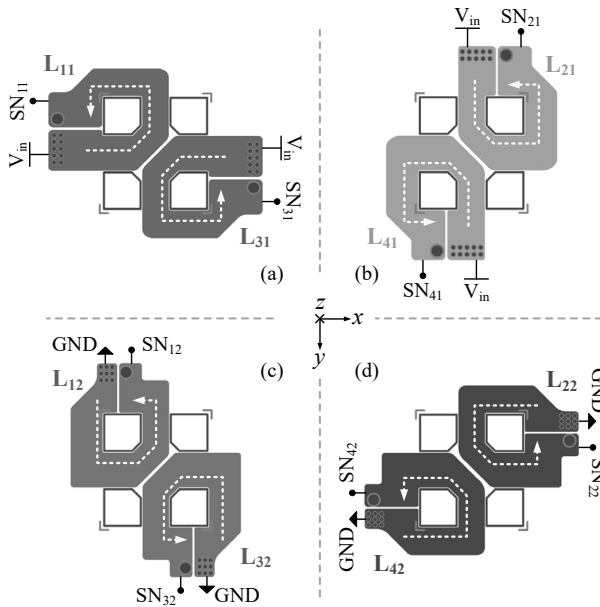


Fig. 20. PCB winding patterns on (a) layer 1 & layer 3, (b) layer 2 & layer 4, (c) layer 5 & layer 7, and (d) layer 6 & layer 8.

Fig. 15. For the side-by-side or non-interleaved overlapping design, the H field mainly flows vertically in the center of the window area or flows horizontally and concentrates between middle layers. As for the interleaved overlapping design, the major H field in the window area also flows horizontally along the conductor layers, but it maintains low and is well balanced across different layers. The high H field in the side-by-side and non-interleaved overlapping design causes concentrated current at nearby conductor surfaces with increased ac resistance, as shown in Fig. 19. Consequently, the interleaved overlapping design has the most balanced ac current distribution with the lowest ac resistance, and thus is

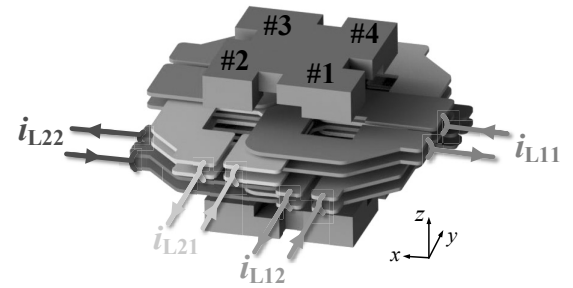


Fig. 21. 3-D structure of the matrix coupled inductor. Winding terminal connections of phases 1 & 2 are plotted for demonstration. Phases 3 & 4 are centrosymmetric to phases 1 & 2. The multilayer overlapped implementation of multiple windings enables greatly reduced ac resistance.

selected.

Detailed winding pattern design on each PCB layer is plotted in Fig. 20. Circuit connections and current flow direction of each winding (as defined in Fig. 16) are labeled in the figure. The overall 3-D structure of the planar matrix coupled inductor is shown in Fig. 21, where parallel winding terminal connections of phases 1 & 2 are drawn for demonstration. Winding patterns and terminal connections of phases 3 & 4 are symmetric to phases 1 & 2.

B. Prototype of the Matrix Coupled SEPIC Converter

The matrix coupled SEPIC prototype is designed to flexibly deliver power from 1 V~5 V input to 1 V~5 V output. Figure 22 shows the annotated prototype from top, bottom, and side views. The prototype measures 35 mm \times 35 mm in area and 5.25 mm in height. Its total volume is 6431 mm³ (i.e., 0.392 in³). On the converter, the matrix coupled inductor is located in the center with four phases of SEPIC surrounding it. As a result, both the matrix coupled inductor and the overall converter structure are centrosymmetric, facilitating keeping balanced parameters across the four phases.

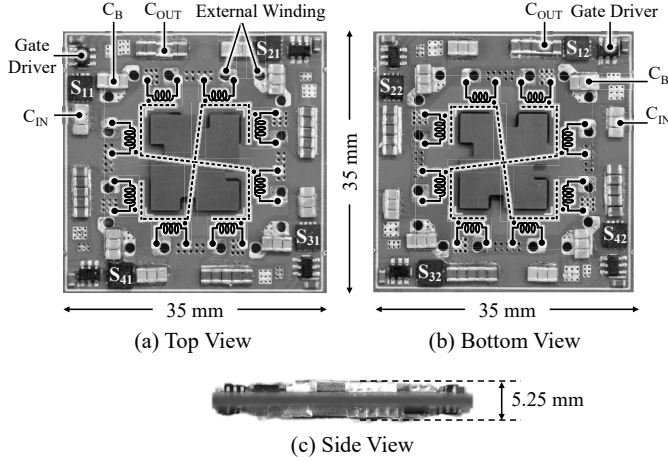


Fig. 22. Annotated matrix coupled SEPIC prototype: (a) top view; (b) bottom view; (c) side view. The prototype measures 35 mm \times 35 mm \times 5.25 mm.

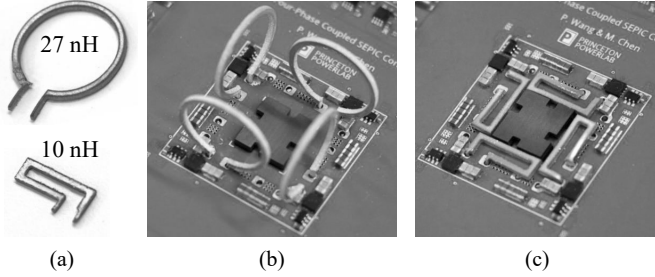


Fig. 23. External winding setup: (a) two winding options; (b) current measurement setup; (c) compact winding setup for high power density;

In the matrix coupled SEPIC converter, blocking capacitors might resonate with the leakage inductance of the coupled inductor. To avoid resonance and keep the blocking capacitors working as dc sources, sufficient leakage inductance is needed for maintaining the resonant frequency far less than the switching frequency [36]. In this design, as shown in Fig. 22, through-hole connections for external windings are reserved to adjust the leakage inductance. Figure 23a shows two alternative external windings: current measurement loop (27 nH) and compact rectangular winding (10 nH), and their assembly setups are shown in Figs. 23b and 23c, respectively. To achieve high power density, the compact rectangular winding is designed to reduce the height so that the prototype thickness is only determined by the magnetic core as shown in Fig. 22c. In the following experiments, all the current measurements are performed with the current measurement loop. Efficiency and maximum output power are measured based on the compact rectangular winding. As implied by Fig. 7, the external winding inductance can be merged into $1/\mathcal{R}_k$ to directly leverage the developed analysis of current ripple and transient performance. Table II lists detailed component descriptions and equivalent magnetic parameters of the two external winding setups. Following experiments are performed based on the parameters in Table II, unless otherwise specified. The leakage inductance of external windings can be further integrated into the matrix coupled

TABLE II
BILL-OF-MATERIAL OF THE MATRIX COUPLED SEPIC PROTOTYPE

Device & Symbol	Description
Low Side Switch, $S_{11} \sim S_{41}$	Infineon BSZ010NE2LS5
High Side Switch, $S_{12} \sim S_{42}$	Infineon BSZ011NE2LS51
Switch Gate Driver	TI LM5114
Blocking Capacitor, $C_{B1} \sim C_{B4}$	X5R 6.3 V, 100 uF \times 6
Input Capacitor, $C_{IN1} \sim C_{IN4}$	X5R 6.3 V, 100 uF \times 6
Output Capacitor, $C_{OUT1} \sim C_{OUT4}$	X5R 6.3 V, 100 uF \times 10
Core Material	Ferroxcube 3F4
Core Leg Reluctance, \mathcal{R}_L	$1.02 \times 10^6 \text{ H}^{-1}$
Leakage Reluctance, \mathcal{R}_C	$19.9 \times 10^6 \text{ H}^{-1}$
Winding Leakage Reluctance, \mathcal{R}_k^*	① $36.9 \times 10^6 \text{ H}^{-1}$ ② $99.0 \times 10^6 \text{ H}^{-1}$

* Equivalent \mathcal{R}_k including the external winding inductance. ① is for the current measurement loop. ② is for the compact rectangular winding.

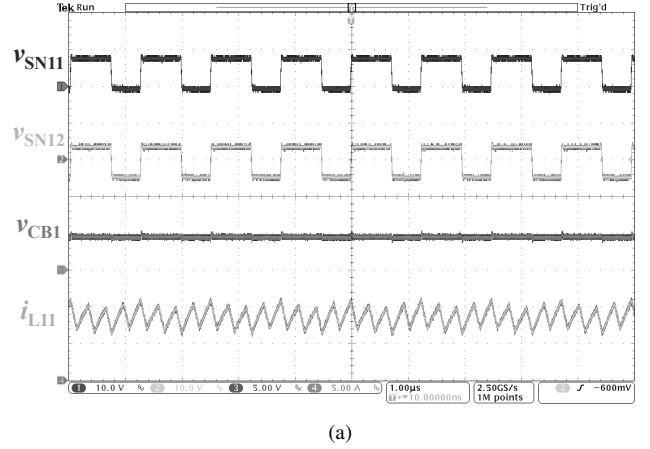


Fig. 24. Measured two switch-node voltages, a blocking capacitor voltage, and an inductor current (as defined in Fig. 16), when $V_{in} = 5 \text{ V}$, $V_{out} = 3.3 \text{ V}$, $I_{out} = 50 \text{ A}$, and $f_{sw} = 806 \text{ kHz}$.

inductor design for maximizing the power density.

Figure 24 plots the measured steady state operation waveforms when the prototype is switching at 806 kHz and converting 5 V into 3.3 V with 50 A load current. As shown in the figure, the blocking capacitor remains stable voltage without resonance, functioning like a dc source as expected. Inductor current ripple is reduced at a frequency of four times the switching frequency due to the multiphase interleaving.

VI. EXPERIMENTAL RESULTS

A. Inductor Current Ripple and Converter Dynamics

Current ripple and transient speed are usually tradeoffs for discrete inductors, whereas the matrix coupled inductor can achieve both low current ripple and fast transient speed at the same time. This subsection experimentally validates the analysis of current ripple reduction, current ripple steering, and converter dynamics as discussed in Sections III and IV.

Figure 25 plots the current ripple reduction ratio (γ) as a function of duty cycle (D) for the two external winding setups and for the case without external winding. Larger external winding leakage inductance leads to lower coupling coefficient and larger transient inductance. According to the magnetic parameters in Table I, matrix coupling coefficients

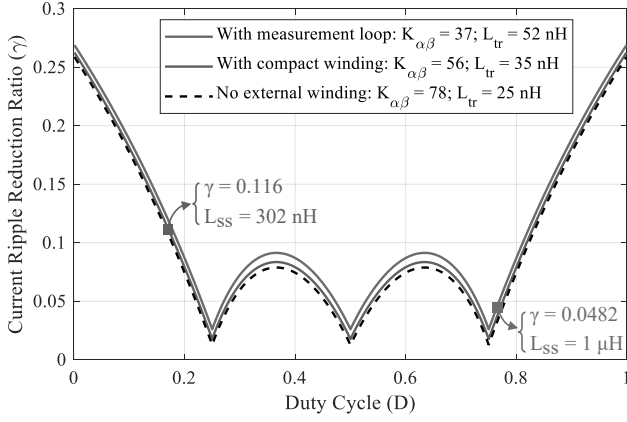


Fig. 25. Current ripple reduction ratio as a function of duty ratio with different external winding setups.

and equivalent transient inductances for the current measurement loop and compact winding setups are: $K_{\alpha\beta} = 37$ & 56 and $L_{tr} = 52$ nH & 35 nH respectively. When directly connecting without external winding, they are $K_{\alpha\beta} = 78$ and $L_{tr} = 25$ nH. Figure 25 implies that the coupling coefficients with the two external winding setups are sufficiently high so that the ripple reduction ratios with and without external windings are similar. The major difference lies in the transient inductance L_{tr} that varies from 25 nH to 52 nH, resulting in the variation of steady state inductance L_{ss} as well as winding current ripple. The figure also indicates that inductor current ripple of the four-phase matrix coupled SEPIC will approach almost zero when $D = k/4$, $k = 1, 2, 3$.

To verify the analysis of current ripple reduction, the matrix coupled SEPIC prototype (with measurement loop) is tested under both interleaved and non-interleaved operations when converting voltage from 1 V to 3.3 V at 1 MHz switching frequency. In this case, $L_{tr} = 52$ nH and $L_{ss} = 1.07$ μ H, as indicated by Fig. 25. Figure 26 shows the measured inductor current ripples, which are well-balanced across the four phases, indicating a good symmetry of the prototype. Under interleaved operation, inductor current ripple is the same as using discrete L_{ss} and is only 0.8 A. Under non-interleaved operation, it is the same as using discrete L_{tr} and increases to 15.5 A. The measured ripple reduction ratio at this duty cycle is 5.2% , reflecting about $20\times$ current ripple reduction compared to using discrete inductors with the same transient speed. The measured current ripples under interleaved and non-interleaved operations as well as ripple reduction ratio match well with the theoretically calculated ones (0.72 A, 14.8 A, 4.8%).

The matrix coupled SEPIC prototype is also tested with asymmetric series coupling to validate current ripple steering. In the experiment, external winding leakage is adjusted by changing the size of current measurement loop. Phases 1 & 3 are selected for demonstration. In phase 1, two external winding leakages are identical (both are 27 nH), while in phase 3, they are 22 nH and 37 nH respectively. Figure 27 shows the measured winding current ripples of phases 1 & 3. As indicated by the figure, the summed phase current ripples

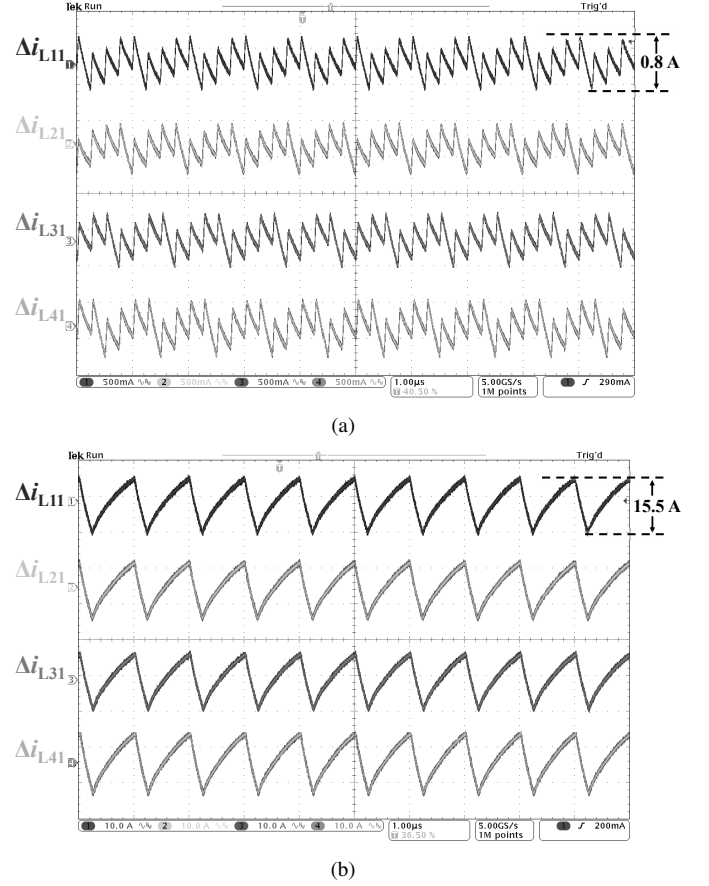


Fig. 26. Inductor current ripple under (a) interleaved operation and (b) non-interleaved operation. $V_{in} = 1$ V, $V_{out} = 3.3$ V, $f_{sw} = 1$ MHz, and tested in the setup with current measurement loops.

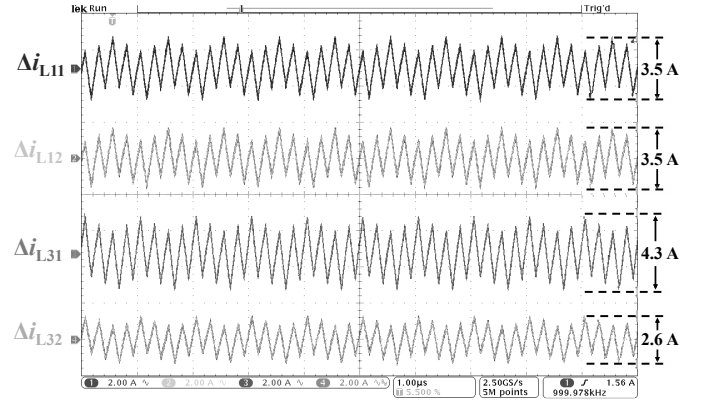


Fig. 27. Measured waveforms for verifying current ripple steering due to asymmetric series coupling. In phase 1, two external winding leakages are both 27 nH, while in phase 3, they are 22 nH and 37 nH respectively. The ripple steering ratio is inversely proportional to external winding leakage inductances.

are still balanced between phases 1 & 3 (i.e., 7 A \approx 6.9 A), because the lumped leakage inductances of the series coupled windings in the two phases are identical (i.e., $27||27$ nH \approx $22||37$ nH). Due to asymmetric series coupling, however, phase current ripple is unevenly distributed between the two windings in phase 3. The distributed ripple percentage is inversely proportional to external winding leakage inductances,

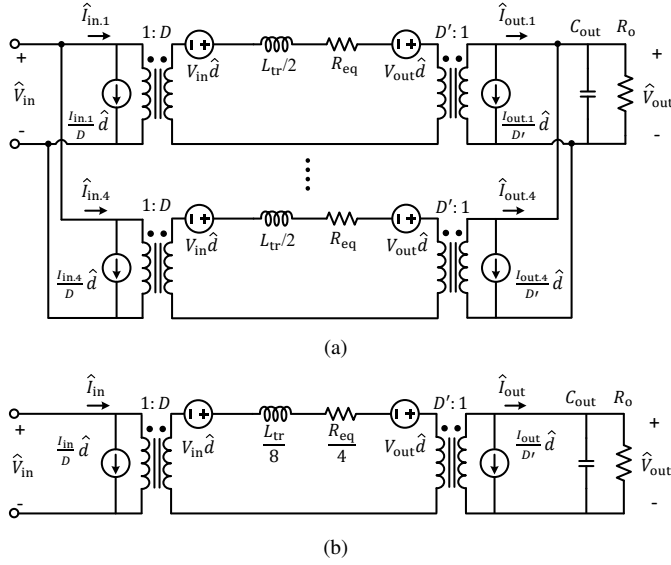


Fig. 28. (a) Small-signal circuit model of the four-phase matrix coupled SEPIC converter. (b) Simplified small-signal circuit model. D is the gate driving duty ratio of the lower switch S_{k1} , and $D' = 1 - D$. Assume blocking capacitors have stable voltages and can be treated as constant voltage sources.

consistent with the analysis in Section III-C.

As discussed in Section IV, converter dynamics of the matrix coupled SEPIC can be analyzed by replacing the matrix coupled inductor with discrete L_{tr} . Then existing modeling methods for SEPIC converter can be directly applied. Figure 28 plots the small-signal circuit model of the four-phase matrix coupled SEPIC. In Fig. 28a, each phase is modeled in the same way as a conventional SEPIC converter with discrete L_{tr} , and small-signal circuits of multiple phases are connected in parallel. An R_{eq} is inserted to capture the power losses of each phase. The simplified small-signal circuit of four parallel phases is plotted in Fig. 28b, indicating that the matrix coupled SEPIC converter is a second-order system. Accordingly, the control (\hat{d}) to output (\hat{v}_{out}) transfer function can be derived:

$$\frac{\hat{v}_{out}}{\hat{d}} = \frac{1}{MR_o D'^2 + R_{eq}} \cdot \frac{(MR_o - \frac{D}{D'^2} R_{eq} - \frac{D}{2D'^2} L_{tr}s) V_{IN}}{\frac{s^2}{\omega_n^2} + \frac{s}{\omega_n Q} + 1}, \quad (14)$$

$$\omega_n = \sqrt{\frac{2R_{eq} + 2MR_o D'^2}{L_{tr} R_o C_{out}}}, \quad Q = \frac{\sqrt{2L_{tr} R_o C_{out}}}{L_{tr} + 2R_{eq} R_o C_{out}} \quad (15)$$

To testify the transfer function, the matrix coupled SEPIC prototype was operated at 3.3-V input to 3.3-V output with 2.5-k Ω R_o and 168- μ F effective C_{out} (considering dc bias degradation). The equivalent R_{eq} is 15.5 m Ω . The control to output transfer function is measured from gate signal to output voltage in the same way as in [30]. Figure 29 compares the measured and modeled transfer functions. The discrepancies mainly come from the errors in the estimated resistance (R_{eq}), non-linear effects in inductors and capacitors, and other factors that the small-signal circuit model doesn't capture, such as deadtime and switching loss.

Figure 30 shows the measured transients during a duty ratio perturbation from 50 % to 53 %. In this test, the effective output capacitance $C_{out} = 8.8 \mu$ F, and the load resistance

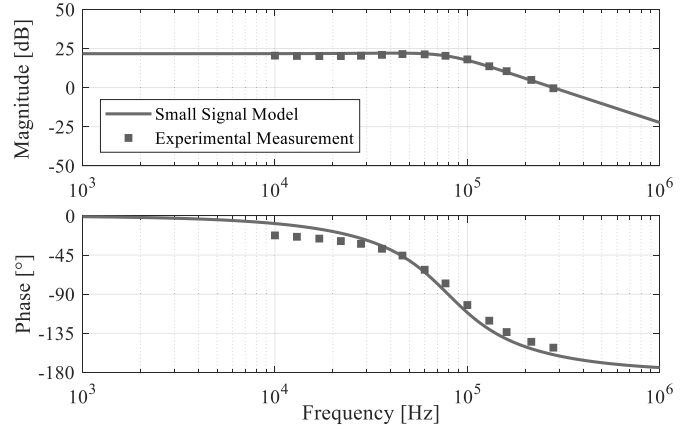


Fig. 29. Modeled and measured bode plots of the control (\hat{d}) to output (\hat{v}_{out}) transfer function. $V_{in} = 3.3$ V, $V_{out} = 3.3$ V, $f_{sw} = 1$ MHz, effective $C_{out} = 168 \mu$ F, $R_o = 2.5$ k Ω , and tested in the setup with current measurement loops.

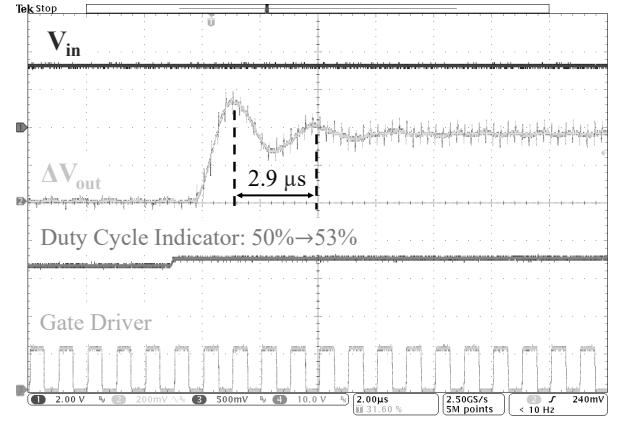


Fig. 30. Duty ratio perturbation from 50 % to 53 %. $V_{in} = 3.3$ V, $V_{out} = 3.3$ V, $f_{sw} = 1$ MHz, effective $C_{out} = 8.8 \mu$ F, $R_o = 0.4 \Omega$, and tested in the setup with current measurement loops. Duty ratio is indicated by the controller DAC output, using 0 ~ 3.3 V to represent 0 ~ 100 % duty ratio.

$R_o = 0.4 \Omega$. According to Eq. (15), the resonant frequency of the control-to-output transfer function is $f_n = \frac{\omega_n}{2\pi} = 333$ kHz. The transient output voltage in Fig. 30 is a typical underdamped second-order system response. The measured resonant frequency of the output voltage waveform is 345 kHz, which is close to the theoretical calculation.

B. Efficiency Measurement and Magnetics Comparison

Figure 31 shows the measured converter efficiency of different conversion ratios when switching at 806 kHz. The peak efficiency and maximum output power for the 5 V-to-3.3 V, 5 V-to-1 V, and 1 V-to-3.3 V conversions are (93.2%, 430 W), (90.3%, 185 W), and (93.5%, 170 W) respectively. The maximum output power in each case is obtained when the hot-spot temperature reaches around 95 $^{\circ}$ C under 36 CFM airflow, as demonstrated in Fig. 32. The measurement results indicate that the matrix coupled SEPIC prototype can flexibly deliver power from 1 V~5 V input to 1 V~5 V output and can deliver up to 185-A output current at 5 V-to-1 V voltage conversion with power density over 470 W/in³.

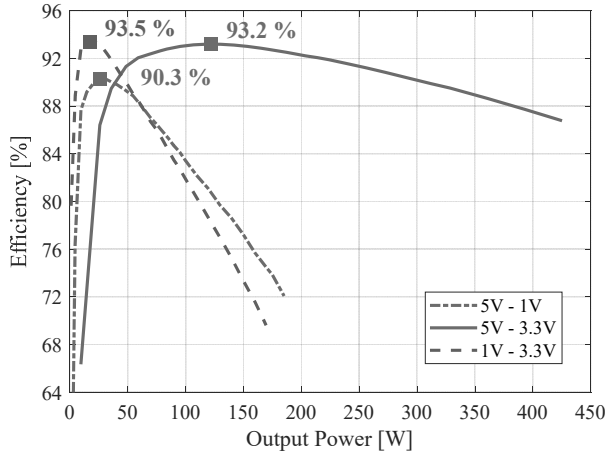


Fig. 31. Measured efficiency of different voltage conversion ratios at 806 kHz switching frequency. Measured with compact winding setup until 95 °C hot-spot temperature, when it is marked as the maximum power.

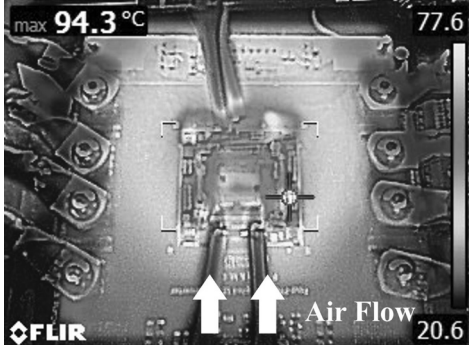


Fig. 32. Full-load hot-spot temperature of the prototype under 36 CFM airflow. ($V_{in} = 5$ V, $V_{out} = 1$ V, $I_{out} = 185$ A, and $f_{sw} = 806$ kHz.)

Detailed power loss breakdown versus output current for the 5 V-to-1 V voltage conversion is plotted in Fig. 33a. In the figure, the calculated efficiency based on the estimated power loss is compared with the measured efficiency. Figure 33b shows the power loss proportion in the peak-efficiency load condition and full load condition. At light load, the switching losses of high side and low side switches dominate and limit the peak efficiency, while at full load, conduction losses of inductor windings and high side switches dominate. In the loss breakdown, winding conduction loss takes up a large portion, especially at heavy load. Therefore, one straightforward way of improving converter efficiency is to integrate the external leakage inductance into the matrix coupled inductor to achieve lower winding resistance. Besides, by replacing the switches with lower current-rated ones that have smaller parasitic capacitance, the switching loss can be reduced, and converter light-load efficiency (including the peak efficiency) can be further improved. The tradeoffs are the increased $R_{ds(on)}$ and the decreased maximum power rating. It is noticeable that the switching loss of low side switches is much higher than their conduction loss, especially at light load. However, the low side switches are still supposed to keep a similar current rating to that of the high-side switches in order to maintain balanced

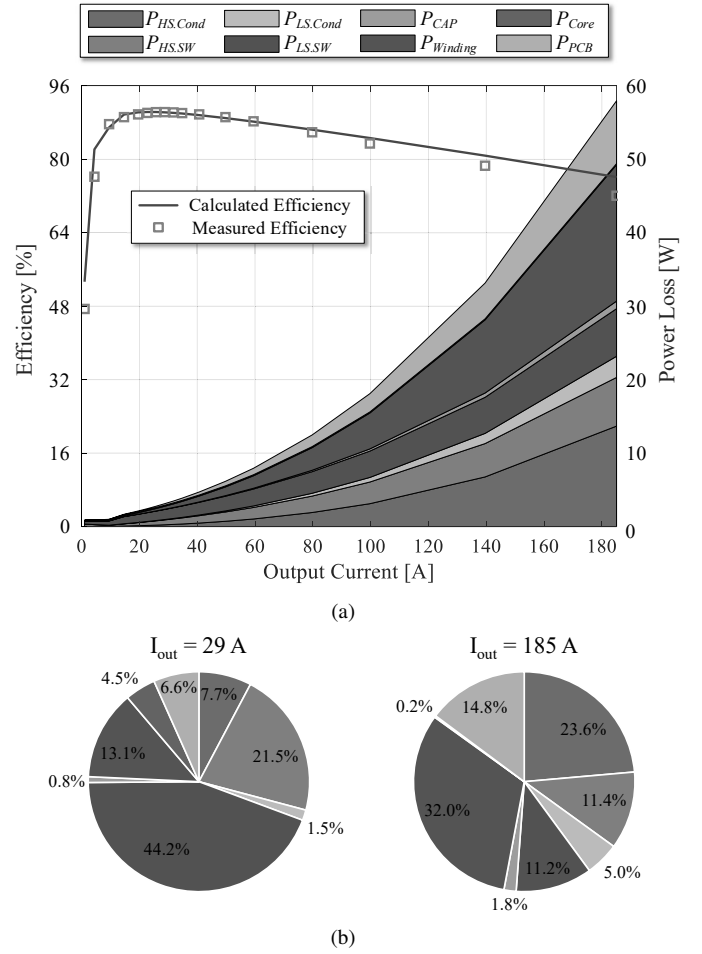


Fig. 33. (a) Detailed power loss breakdown and calculated efficiency for 5 V-to-1 V voltage conversion at 806 kHz switching frequency. (b) Power loss proportion in the peak-efficiency load condition ($I_{out} = 29$ A) and full load condition ($I_{out} = 185$ A). Loss breakdown includes conduction loss and switching loss of high side and low side switches, $P_{HS.Cond}$, $P_{HS.SW}$, $P_{LS.Cond}$, $P_{LS.SW}$; ESR loss of blocking capacitors P_{Cap} ; inductor winding loss and core loss, $P_{Winding}$, P_{Core} ; conduction loss of PCB traces and vias, P_{PCB} .

performance across wide buck and boost conversion range.

According to Fig. 25, the designed matrix coupled inductor (with compact winding) has the same fast transient speed as a 35-nH discrete inductor and maintains the same low current ripple as a 302-nH discrete inductor at 5 V-to-1 V voltage conversion. Figure 34 compares the matrix coupled inductor with the state-of-the-art commercial discrete inductors. Here, Coilcraft SER1412-301ME inductor that has similar current ripple and current rating is selected. Both the magnetic core and inductor windings (i.e., PCB & external windings) are included in the matrix coupled inductor for the size comparison. The box volume of eight discrete inductors and one matrix coupled inductor are 16,978 mm³ and 3,024 mm³, respectively, indicating over 5.6 times size reduction.

To further compare the converter performance, the four-phase SEPIC prototype is also tested with discrete inductors as shown in Fig. 35a. Figure 35b plots the converter efficiency with the matrix coupled inductor and with discrete inductors, which are almost the same. It is consistent with the analysis

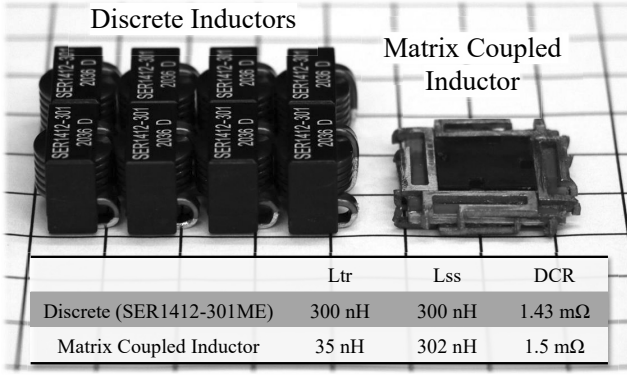


Fig. 34. Size comparison between commercial discrete inductors and the matrix coupled inductor. The background grid cell size is 1 cm. Comparison is based on the same current ripple, similar winding dc resistance (DCR), and similar current ratings (i.e., $I_{rms} \geq 40$ A with inductor temperature rise less than 40 °C) when converting voltage from 5 V to 1 V at 806 kHz switching frequency. Box dimensions (length×width×height) of the eight discrete inductors and the matrix coupled inductor are $44 \times 30.48 \times 12.66$ mm³ and $24 \times 24 \times 5.25$ mm³, respectively.

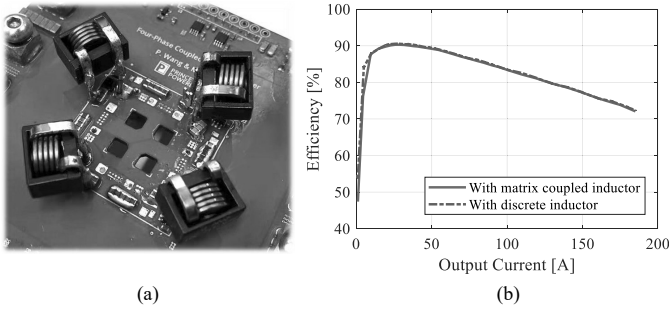


Fig. 35. (a) Four-phase SEPIC prototype equipped with discrete inductors. (b) Efficiency comparison of the SEPIC prototype with one matrix coupled inductor (compact winding) and with eight discrete inductors.

since they have the same current ripple and similar winding resistance. Figure 36 shows the measured open-loop transient response of the two inductor setups during a duty ratio step change. As indicated by the figure, the matrix coupled inductor can significantly improve the transient performance by reducing both settling time and voltage overshoot. Consequently, compared to commercial discrete inductors, the designed matrix coupled inductor can reduce total magnetic volume by over 5.6 times and improve the transient speed by over 8.5 times (i.e., L_{tr} reduced from 300 nH to 35 nH) while maintaining similar current ripple and current rating.

VII. CONCLUSION

This paper presents a matrix coupled magnetic structure that combines both series coupling and parallel coupling. A systematic analysis of the current ripple reduction is performed, which implies that current ripple reduction fundamentally comes from multiphase interleaving, and coupling coefficients will scale the ripple reduction ratio gained from interleaving. To have lower current ripple, both stronger series coupling and parallel coupling are preferred. Current ripple steering due to asymmetric series coupling is discussed, and steering ratios are derived. By adjusting steering ratios, ripple

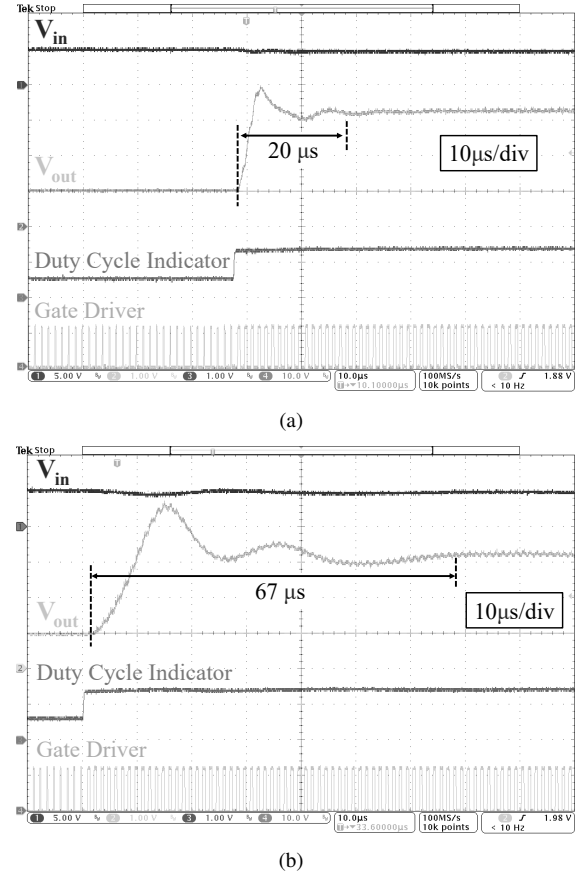


Fig. 36. Measured open-loop transient waveforms of the SEPIC prototype with (a) matrix coupled inductor (compact winding); (b) discrete inductors. Duty ratio steps from 17% to 41.9%. $V_{in} = 5$ V; V_{out} changes from 1 V to 3.3 V; $I_{out} = 20$ A; $f_{sw} = 806$ kHz; effective $C_{out} = 300$ μF.

can be steered away from specific windings, beneficial to ripple-sensitive applications. The transient performance of the matrix coupled inductor is demystified, providing guidance on converter dynamics analysis and large- or small-signal model derivation. To quantify the benefits of matrix coupling, a FOM is defined by comparing the current ripple of a matrix coupled inductor to that of a discrete inductor given the same transient speed. The comparison results indicate that a higher number of phases and a stronger matrix coupling coefficient will amplify the benefits of matrix coupled inductors compared to discrete ones. A 1 V-to-5 V input, 1 V-to-5 V output, four-phase matrix coupled synchronous SEPIC converter was designed and built. The matrix coupled inductor is implemented as a PCB planar magnetic component with an optimized winding design to reduce ac resistance. The matrix coupled SEPIC prototype achieves a maximum power density over 470 W/in³ at 5 V-to-1 V voltage conversion. Compared to discrete commercial inductors, the designed matrix coupled inductor has a 5.6 times smaller size and 8.5 times faster transient speed with similar current ripple and current rating. The experimental results validate both the matrix coupling concept and the theoretical analysis.

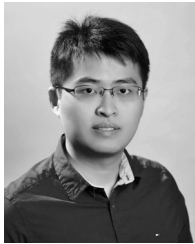
ACKNOWLEDGMENT

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy

(ARPA-E), U.S. Department of Energy, under Award Number DE-AR0000906 in the CIRCUITS program monitored by Dr. Isik Kizilyalli. The work was also jointly supported by pSemi Corporation, the NSF CAREER award (#1847365). The views and opinions of the authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

REFERENCES

- [1] P. Wang, D. Zhou, V. Yang and M. Chen, "Matrix Coupled All-in-One Magnetics for PWM Power Conversion," in *Proc. IEEE Workshop Control Model. Power Electron.*, 2021, pp. 1-8.
- [2] C. R. Sullivan, B. A. Reese, A. L. F. Stein and P. A. Kyaw, "On Size and Magnetics: Why Small Efficient Power Inductors are Rare," in *Intl. Symp. 3D Power Electron. Integr. Mfg.*, Raleigh, NC, 2016, pp. 1-23.
- [3] I. A. Bassett, "Constant frequency ZVS converter with integrated magnetics," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1992, pp. 709-716.
- [4] A. Kats, G. Ivensky and S. Ben-Yaakov, "Application of integrated magnetics in resonant converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1997, pp. 925-930 vol.2.
- [5] W. Chen, G. Hua, D. Sable and F. Lee, "Design of high efficiency, low profile, low voltage converter with integrated magnetics," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1997, pp. 911-917 vol.2.
- [6] M. H. Ahmed, A. Nabih, F. C. Lee and Q. Li, "Low-Loss Integrated Inductor and Transformer Structure and Application in Regulated LLC Converter for 48-V Bus Converter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 589-600, March 2020.
- [7] B. K. Kang, S. K. Chung, and D. S. Oh, "Integrated magnetics for boost PFC and flyback converters with phase-shifted PWM," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 1018-1024.
- [8] M. Chen and C. R. Sullivan, "Unified Models for Coupled Inductors Applied to Multiphase PWM Converters," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14155-14174, Dec. 2021.
- [9] C. Zhao, S. D. Round and J. W. Kolar, "An Isolated Three-Port Bidirectional DC-DC Converter With Decoupled Power Flow Management," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2443-2453, Sept. 2008.
- [10] P. Wang, Y. Chen, J. Yuan, R. C. N. Pilawa-Podgurski and M. Chen, "Differential Power Processing for Ultra-Efficient Data Storage," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4269-4286, April 2021.
- [11] P. Wang and M. Chen, "Analysis and Design of Series Voltage Compensator for Differential Power Processing," *IEEE Trans. Emerg. Sel. Topics Power Electron.*
- [12] Y. Chen, P. Wang, Y. Elasser and M. Chen, "Multicell Reconfigurable Multi-Input Multi-Output Energy Router Architecture," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13210-13224, Dec. 2020.
- [13] Y. Chen, Y. Elasser, P. Wang, J. Baek and M. Chen, "Turbo-MMC: Minimizing the Submodule Capacitor Size in Modular Multilevel Converters with a Matrix Charge Balancer," in *Proc. IEEE Workshop Control Model. Power Electron.*, 2019, pp. 1-8.
- [14] M. Liu, P. Wang, Y. Guan and M. Chen, "A 13.56 MHz Multiport-Wireless-Coupled (MWC) Battery Balancer with High Frequency On-line Electrochemical Impedance Spectroscopy," in *Proc. IEEE Energy Convers. Cong. Expo.*, 2019, pp. 537-544.
- [15] S. Čuk, "A New Zero-Ripple Switching DC-to-DC Converter and Integrated Magnetics," *IEEE Trans. Magn.*, vol. 19, no. 2, pp. 57-75, March 1983.
- [16] S. Čuk and Z. Zhang, "Coupled-Inductor Analysis and Design," in *Proc. IEEE Power Electron. Specialists Conf.*, 1986, pp. 655-665.
- [17] J. Betten, "Benefits of a Coupled-Inductor SEPIC Converter," *Texas Instruments Analog Applications Journal*, 2011.
- [18] K. Yao, M. Ye, M. Xu and F. C. Lee, "Tapped-inductor buck converter for high-step-down DC-DC conversion," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 775-780, July 2005.
- [19] Q. Zhao, F. Tao and F. C. Lee, "A front-end DC/DC converter for network server applications," in *Proc. IEEE Power Electron. Specialists Conf.*, 2001, pp. 1535-1539 vol. 3.
- [20] *Desktop Platform Form Factors Power Supply Design Guide*, Intel, Santa Clara, CA, USA. [Online]. Available: <https://www.intel.com/content/dam/www/public/us/en/documents/guides/power-supply-design-guide-june.pdf>
- [21] C. Shi, A. Khaligh and H. Wang, "Interleaved SEPIC Power Factor Preregulator Using Coupled Inductors in Discontinuous Conduction Mode with Wide Output Voltage," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3461-3471, July-Aug. 2016.
- [22] J. Baek, Y. Elasser, K. Radhakrishnan, H. Gan, J. P. Douglas, H. K. Krishnamurthy, X. Li, S. Jiang, C. R. Sullivan and M. Chen, "Vertical Stacked LEGO-PoL CPU Voltage Regulator," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6305-6322, June 2022.
- [23] Y. Chen, P. Wang, H. Cheng, G. Szczeszynski, S. Allen, D. M. Giuliano and M. Chen, "Virtual Intermediate Bus CPU Voltage Regulator," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6883-6898, June 2022.
- [24] P.-L. Wong, "Performance Improvements of Multi-Channel Interleaving Voltage Regulator Modules with Integrated Coupling Inductors," Ph.D. Thesis, Virginia Tech, 2001.
- [25] Y. Dong, "Investigation of Multiphase Coupled-Inductor Buck Converters in Point-of-Load Applications," Ph.D. Thesis, Virginia Tech, 2009.
- [26] J. Li, A. Stratakos, A. Schultz and C. R. Sullivan, "Using Coupled Inductors to Enhance Transient Performance of Multi-Phase Buck Converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2004, pp. 1289-1293 vol.2.
- [27] C. R. Sullivan and M. Chen, "Coupled Inductors for Fast-Response High-Density Power Delivery: Discrete and Integrated," in *Proc. IEEE Cust. Integr. Circuits Conf.*, 2021, pp. 1-8.
- [28] A. Ikriannikov, "The benefits of the coupled inductor technology," Maxim Integrated, San Jose, CA, USA, Tutorial 5997, 2014.
- [29] Y. Elasser, J. Baek, C. R. Sullivan and M. Chen, "Modeling and Design of Vertical Multiphase Coupled Inductors with Inductance Dual Model," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 1717-1724.
- [30] D. H. Zhou, Y. Elasser, J. Baek and M. Chen, "Reluctance-Based Dynamic Models for Multiphase Coupled Inductor Buck Converters," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1334-1351, Feb. 2022.
- [31] P. Wang, Y. Elasser, V. Yang and M. Chen, "WAN Converter: A Family of Multicell PWM Converter with All-in-One Magnetics," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 1035-1042.
- [32] Peng Xu, Qiaoqiao Wu, Pit-Leong Wong and F. C. Lee, "A novel integrated current doubler rectifier," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2000, pp. 735-740 vol.2.
- [33] S. Chandrasekaran, V. Mehrotra and H. Sun, "A new matrix integrated magnetics (MIM) structure for low voltage, high current DC-DC converters," in *Proc. IEEE Power Electron. Specialists Conf.*, 2002, pp. 1230-1235 vol.3.
- [34] T. Qian and B. Lehman, "Coupled Input-Series and Output-Parallel Dual Interleaved Flyback Converter for High Input Voltage Application," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 88-95, Jan. 2008.
- [35] M. Noah, K. Umetani, J. Imaoka, and M. Yamamoto, "Lagrangian dynamics model and practical implementation of an integrated transformer in multi-phase LLC resonant converter," *IET Power Electron.*, vol. 11, no. 2, pp. 339-347, 2018.
- [36] T. Ge and K. D. T. Ngo, "Omnicoiled Inductors (OCI) Applied in a Resonant Cross-Commutated Buck Converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4894-4902, June 2021.
- [37] D. Maksimović, "Synthesis of PWM and Quasi-Resonant DC-to-DC Power Converters," Ph.D. Dissertation, California Institute of Technology, 1989.
- [38] H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson and D. Maksimovic, "A 98.7% Efficient Composite Converter Architecture With Application-Tailored Efficiency Characteristic," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 101-110, Jan. 2016.
- [39] M. H. Ahmed, C. Fei, F. C. Lee and Q. Li, "Single-Stage High-Efficiency 48/1 V Sigma Converter With Integrated Magnetics," *IEEE Trans. Ind. Electron.*, vol. 67, no. 1, pp. 192-202, Jan. 2020.
- [40] MIT EE Staff, *Magnetic Circuits and Transformers*, Cambridge MA, USA: MIT Press, 1943.
- [41] F. E. Terman, "Section 2: Circuit Elements," in *Radio Engineers' Handbook*, 1st ed., New York, NY, USA: McGraw-Hill, 1943.
- [42] E. C. Cherry, "The Duality between Interlinked Electric and Magnetic Circuits and the Formation of Transformer Equivalent Circuits," in *Prof. of the Physical Society*, vol. 62 part 2, Section B, 1949, pp. 101-111.
- [43] S. El-Hamamsy and E. I. Chang, "Magnetics Modeling for Computer-Aided Design of Power Electronics Circuits," in *Proc. IEEE Power Electron. Specialists Conf.*, 1989, pp. 635-645 vol.2.
- [44] G. W. Ludwig and S. El-Hamamsy, "Coupled inductance and reluctance models of magnetic components," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 240-250, April 1991.



Ping Wang (Student Member, IEEE) received the B.S. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2017, and the M.A. degree in electrical engineering in 2019 from Princeton University, NJ, USA, where he is currently working toward the Ph.D. degree.

His research interests include high-efficiency/high-density power converters, multiport dc-dc converters, and high-performance power electronics design for data center and telecom applications.

Mr. Wang received two Prize Paper Awards of the IEEE Transactions on Power Electronics in 2020 and 2021 respectively, two National Scholarship Awards in 2014 and 2016 at Shanghai Jiao Tong University, two First Place Awards of the IEEE ECCE Best Student Project Demonstration Competition in 2019 and 2021, the First Place Award from the Innovation Forum of Princeton University in 2019, and the outstanding presentation award in the 2022 IEEE APEC.



Jaeh Baek (Member, IEEE) received the B.S. degree in electronics and electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 2011, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2015 and 2018, respectively.

From 2019 to 2022, he was a Postdoctoral Research Associate with the Department of Electrical and Computer Engineering and the Andlinger Center for Energy and the Environment, Princeton University, Princeton, NJ, USA. Since 2022, he has been with the Power Delivery Core Competency Team, Intel Corporation, Chandler, AZ, USA.

His research interests include microprocessor power delivery, point-of-load power converters, grid interface power electronics, digital control approach of converters, and advanced power electronics architecture. Dr. Baek was the recipient of the Research Outstanding Award from the Korea Advanced Institute of Science and Technology, the Global Ph.D. Fellowship and Postdoctoral Fellowship Awards from the National Research Foundation of Korea, the First Place Award of the IEEE ECCE Best Demonstration in 2021, and an Open Compute Project Best Paper Award in 2021.



Daniel H. Zhou (Student Member, IEEE) received the B.A.Sc degree in Mechatronics engineering from the University of Waterloo, Waterloo, Canada, in 2019. He received the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA in 2021 and is currently working towards the Ph.D. degree.

His research interests include ultrafast point-of-load power converters, hybrid switched-capacitor magnetics power converters, dynamic modeling and control of power electronics, and power magnetics.

Mr. Zhou was the recipient of the Colonel Hugh Heasley Engineering Scholarship at the University of Waterloo. At Princeton University, he was awarded the prestigious NSERC Alexander Graham Bell Graduate Scholarship.



Minjie Chen (Senior Member, IEEE) received the B.S. degree from Tsinghua University, Beijing, China, in 2009, and the S.M., E.E., and Ph.D. degrees from Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2012, 2014, and 2015, respectively. He is an Assistant Professor of Electrical and Computer Engineering and Andlinger Center for Energy and the Environment at Princeton University, where he leads the Princeton Power Electronics Research Lab. His research interests include complex power architecture, circuit-magnetics co-design, control, and machine learning methods for power magnetics modeling.

Dr. Chen is the Vice Chair of IEEE PELS Technical Committee on Design Methodologies (TC10), Associate Editor of IEEE Transactions on Power Electronics, Associate Editor of IEEE Journal of Emerging and Selected Topics in Power Electronics, Associate Technical Program Committee Chair of IEEE Energy Conversion Congress and Exposition (ECCE) in 2019, Student Activity Chair of IEEE Energy Conversion Congress and Exposition (ECCE) in 2020, and the Technical Program Committee Chair of IEEE International Conference on DC Microgrids (ICDCM) in 2021.

Dr. Chen is a recipient of the Princeton SEAS E. Lawrence Keyes, Jr./Emerson Electric Co. Junior Faculty Award (2022), five IEEE Transactions Prize Paper Awards (2016, 2017, 2020, 2021, 2021), a COMPEL Best Paper Award (2020), an OCP Best Paper Award (2021), the NSF CAREER Award (2019), a Dimitris N. Chorafas Award for outstanding MIT Ph.D. Thesis (2015), three ECCE Best Demonstration Awards (2014, 2019, 2021), multiple APEC Outstanding Presentation Awards, a Siebel Energy Institute Research Award (2017), a C3.ai DTI Research Award (2021), the First Place Award from the Innovation Forum of Princeton University (2019), and many other awards. He was included in the Princeton Engineering Commendation List for Outstanding Teaching from 2019 to 2022. He holds 7 U.S. patents.



Youssef Elasser (Student Member, IEEE) received the B.S. degree in electrical engineering and computer science with a concentration in electric power from Rensselaer Polytechnic Institute, Troy, NY, USA, in 2018. He is currently working toward the Ph.D. degree with Princeton University, Princeton, NJ, USA.

His research interests include renewable energy storage systems, dc-dc power conversion, and magnetics design and optimization.

Mr. Elasser was the recipient of the Grainger Scholars Award for distinguished undergraduates studying electric power while at Rensselaer Polytechnic Institute, the IEEE Transactions on Power Electronics Prize Paper Award, the first place award for the IEEE Energy Conversion Congress and Exposition Student Demonstration in 2021, the First Place Award from the 2019 Princeton Innovation Forum, and the prestigious National Science Foundation Graduate Research Fellowship while at Princeton University.