Two Pattern Timing Tests Capturing Defect-Induced Multi-Gate Delay Impact of Shorts

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***Abstract*—Achieving high yield in deep-submicron technologies is challenging due to the presence of unforeseen defect mechanisms, requiring increases in test complexity and efficiency. We focus on shorts within standard cells which are traditionally targeted by DC tests. Recent research has shown the need for multi-pattern tests where intermediate defect resistance values are concerned, as opposed to extreme values considered by prevalent test techniques. In this research, we show that there exist ranges of short defect resistance values that escape traditional DC tests while incurring unexpectedly large delay values for specific two-pattern stimuli. It is seen that these resistance values are approximately in the range of defect resistance values observed for realistic short defects in industry. These defects must therefore be prioritized from a circuit level critical path delay testing perspective to minimize overall circuit DPPM. Such catastrophic increase in delay is due to the fact that specific shorts in standard cells influence the delays of logic gates feeding into and out of the standard cell, resulting in path delay increase of 50X-80X with respect to the delay of a single cell. Two-pattern tests are derived for such faults and simulation results on standard cell designs and ripple carry adders are presented to further our arguments.**

***Index Terms*—Delay testing, Short defects, Multi-pattern test generation, Fault model, Cell-Aware Test**

I. Introduction

Scan based structural tests for integrated circuits (ICs) have traditionally been generated based on the classical stuck-at (SA) and transition delay fault (TDF) models. These tests target permanent and delay faults at the circuit nodes that form the input and output connections between the logic gates and/or standard cells in the design. Such a methodology can sometimes fail to detect defects inside the gates and standard cells themselves, since such cell-internal faults are not explicitly targeted. While many are fortuitously detected by the tests that target faults on the circuit interconnects, other internal defects, particularly in large complex library cells, can escape detection. To plug this test coverage hole, the "cell aware" test generation methodology has been developed over the past decade. Here shorts and opens, including resistive defects, are injected and simulated in the library cells, and tests are generated to detect those that can cause errors at the circuit outputs. Published experiments with cell aware tests have reported hundreds of DPPM reduction in defect levels for complex SoC parts. However, there remains some debate in industry with regard to the cost effectiveness of the approach. Extensive analog simulation of the entire cell library for each injected defect can be extremely expensive. An even more significant increase in test cost results from the much larger test sets generated by such an approach. Test pattern counts can be multiple times of those for traditional SA and TDF tests, requiring prohibitively long test application time. Consequently, not all the possible resistive open and short defects that can be injected into the cell library can be targeted for ATPG and tested in practice. This has motivated research on test prioritization based on the likelihood of occurrence and impact of each cell-internal defect that is targeted. The goal is to rank order tests based on their potential impact on DPPM so that the most effective tests can be selected for any test time budget. Test prioritization requires a thorough understanding and classification of the different types of cell internal defects. This paper is a study of resistive shorts in CMOS logic gates towards this goal.

Key Contributions: The key contribution of this paper is the significantly new understanding of the behavior of realistic short defects in causing circuit timing errors, and methods to target them during test. Specifically, we show that:

(1) Depending on the type of CMOS gate, defect location, and processes parameters, resistive short defects above some critical resistance in the 0-10 Kohm range are DC undetectable, and can only be detected by two-pattern delay tests. Note that in practice, the vast majority of actual resistive defects are observed to be well within this relatively low resistance range, and therefore necessitate delay tests for testing these shorts. Shorts should be targeted at VDDmin to maximize the likelihood of detection by DC tests, while at the same time maximizing delay effects to aid the timing tests if it is DC undetectable. *(2)* The magnitude of the increase in path delay due to a realistic resistive short can be $> 50X$ as compared to the fault free gate delay. Importantly, only a small part of this large delay increase is reflected in the defective gate itself. Other fault free gates along the path also experience large delays, from the weakened output drive strength of the faulty gate, and slow input ramp rates, resulting in a *cumulatively large path delay*. This important understanding of delay accumulation is missed by most current test methodologies, including CAT (cell aware test) technique, that focuses on delay metrics for a *single* cell. *(3)* Because of this distributed delay impact of shorts, the worst case path delay increase from resistive shorts is more than an order of magnitude

greater than that for realistic resistive opens. Consequently, detection of the former should be prioritized since they are more likely to lead to timing errors. Currently, shorts are generally not explicitly targeted by two-pattern delay tests. Further, for shorts in transistors, gate-source and source-drain shorts have a significantly greater delay impact than gate-drain shorts.

The rest of the paper is organized as follows: Section II discusses the prior works and the relevance. Section III presents an overview of the short defect analysis and the preliminary results are shown in section IV. Section V presents the primary experimental results.

II. Prior Work and Relevance

In the past, IDDQ tests have been used for detection of bridging faults [1]–[3]. This suffers in short defect sensitivity for large circuits and incurs significant test time. Consequently, logical testing [4] [5] is preferred for testing short defects among current test methodologies. In [6], the generation of logic tests for transistor stuck-on and bridging faults using the functional description of logic gates in the circuit-under-test is developed. Voltage based tests presented in this work focus mainly on DC test based detection of bridging faults. Open defects are known to require delay tests for their detection. Multi-pattern requirement for resistive open defects has been studied in [7]. More complex fault models have been published such as CAT [8] and its effectiveness in reducing DPPM [9] [10] [11] [12]. In [13], timing-aware Cell-Aware test (CAT) is presented and targets small delay defects in FinFET technology designs for DPPM reduction. In the CAT approach, the test patterns are generated by performing analog SPICE simulations on the standalone standard cells. The defect behavior is also estimated based upon the isolated simulations. In [14] and [15], the test generation approach using SL-ATPG (switch level ATPG) is presented, which is shown to reduce the test generation time as compared to CAT methodology. In [16], ATPG scheme to target increasingly weaker defect and its comparison to CAT approach is studied.

It has been shown in the past [17], that the propagation delay of a logic gate depends on the input transition time as shown by Equation 1.

$$t_{pHL}, t_{pLH} = \left(\frac{1}{2} - \frac{(1-(V_{TH}/V_{DD}))}{(1+\alpha)}\right) t_T + \frac{C_L V_{DD}}{2 I_D} \quad (1)$$

The first term on the right hand side of the equation is the input waveform dependent term, proportional to the input waveform transition time t_T. C_L is the load capacitance, I_D is the drain current and V_{TH} is the threshold voltage. It has been shown in [17] that for specific values of α, the delay depends on the input transition time. This means that the delay behavior of the logic gate depends on the signal generated by the driving gate and the transition time of the output signal affects the delay of the driven gate. Based on this, delay effects can accumulate over multiple gates in a sensitized circuit path. Our current work uses this distributed delay phenomenon as its basis. As opposed to [18], where multi-pattern test for weak short defects (high defect resistance) were investigated using a purely circuit simulation based approach for *standard cells only*, in this work we develop specific two pattern tests for strong short defects (low defect resistance) which can cause exceptionally high *path delay increase across interconnected logic gates*.

III. Overview: Shorts Effect Analysis

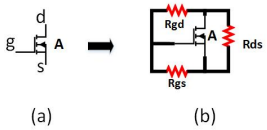

Fig. 1: Fault model for short defects

The delay behavior due to the different short defect types considered in this work (as shown in Figure 1) are discussed below:

(a) Drain-Source short defect: Consider the drain-source short in transistor $N1$ of a NAND2 gate modeled by resistance Rds in Figure 2. To detect this short, we first apply [a2,b2] = [1,1]. This forces the output (out) to logic 0. Next, we apply the vector [a2,b2] = [0,1]. This turns on the transistor $P1$ in the pull-up chain and turns off the transistor $N1$ in the pull-down chain. However, there is voltage division between the "on" resistance R_{P1} of transistor $P1$ and the resistance $(Rds + R_{N2})$, where R_{N2} is the "on" resistance of transistor $N2$. We define $V_{mid} = Vdd/2$ as the mid-point voltage of the gate. When $R_{P1} << Rds + R_{N2}$, the output "out" is interpreted correctly as logic 1. When $R_{P1} >> Rds + R_{N2}$, the output "out" is interpreted as logic 0 and is detected by the DC test [a2,b2] = [0,1]. For values of R_{P1} that are marginally less than or equal to $Rds + R_{N2}$ and depending on the logic threshold of the following gate (inverter G4 in Figure 2), the output voltage on node "out" is approximately close to V_{mid}. This

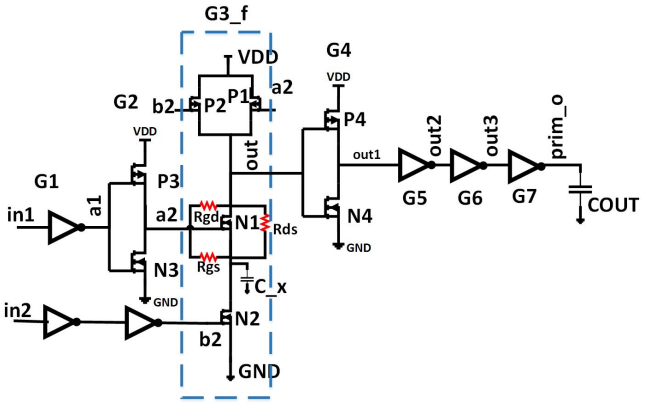

Fig. 2: Testbench for short defect analysis in NAND2

results in a *delay fault* and necessitates application of the two-vector pattern [a2,b2] = [1,1] followed by [a2,b2] = [0,1]. The broad concept presented here for a 2-input NAND gate is easily extended to a drain-source short in transistor $N2$ of the gate as well as transistors in other series-connected chains of N and P-type transistors of other types of NAND, NOR, AND, OR, AOI and other logic gates by symmetry.

For example, for NAND3 logic, the test patterns for drain-source shorts in each of the three pull-down N-type transistors are ([1,1,1],[0,1,1]), ([1,1,1],[1,0,1]) and ([1,1,1],[1,1,0]). Note that the two-pattern tests generated also detect corresponding *gate-open* faults in the P-type transistors of the pull-up chains on NAND logic. Corresponding scenarios are observed for AOI gates. A detailed discussion is omitted for brevity.

(b) Gate-Source short defect: To detect the gate-source short Rgs in transistor $N1$ of Figure 2, we apply the vector [a2,b2] = [0,1], followed by the vector [a2,b2] = [1,1]. The application of [a2,b2] = [0,1] sets the output node of the gate "out" to logic 1. Subsequently, when the vector [a2,b2] = [1,1] is applied, voltage division occurs between the "on" resistance R_{P3} of the inverter *driving the faulty NAND2 gate* and the series resistance $Rgs + R_{N2}$. For $R_{P3} << Rgs + R_{N2}$, the gate functions correctly. For $R_{P3} >> Rgs + R_{N2}$, the transistor $N1$ is cut-off or close to cut-off and the defect is detected by a specified two pattern test. However, when $[(Rgs + R_{N2})/(R_{P3} + Rgs + R_{N2})] \cdot Vdd <= V_{tn}$, where V_{tn} is the threshold voltage of transistor $N1$, the latter is partially conducting with an intermediate drain-source resistance value R'_{N1}, where $R'_{N1} > R_{N1}$ and R_{N1} is the nominal "on" resistance of transistor $N1$. For sufficiently large R'_{N1}, the transition (capacitive discharge) time of the output "out" from 1 to 0 is significantly extended, incurring a *large delay value*. One other issue is that the fall time of the output "out" depends on how quickly the transistor $N1$ switches from OFF to ON. The lower the value of $Rgs + R_{N2}$, the longer it takes for the transistor $P3$ of the driving gate to pull up the gate input value $a2$ to turn the transistor $N1$ on (or semi-on as discussed above). This directly affects the fall time above. Hence, every transistor in the series NAND pull-down chain must be turned from OFF to ON by a dedicated input vector pair. Hence, both input vector pairs ([0,1],[1,1]) and ([1,0],[1,1]) are needed to test for gate-drain shorts in the transistors $N1$ and $N2$ of Figure 2.

It is easily seen that the same vector pairs above detect drain-source shorts in all the P-type transistors of the NAND2 gate as well as gate open shorts in all the series N-type transistors of the pull-down chain of the NAND2 gate. As before, the tests can be extended to other types of logic gates by symmetry. The vector pairs for a NAND3 gate are ([0,1,1],[1,1,1]), ([1,0,1],[1,1,1]) and ([1,1,0],[1,1,1]) by symmetry.

(c) Gate-Drain short defect: To detect the gate-drain short Rgd in transistor $N1$ of Figure 2, we apply the vector [a2,b2] = [1,1] followed by the vector [a2,b2] = [0,1]. The vector [a2,b2] = [1,1] sets the output "out" to logic 0. It should be noted that for very low resistance shorts the output "out" will not be logic 0, these values of resistances will be detected by DC test (For Rgd=10ohms "out" is 0.6V). As the value of Rgd is decreased from a high value, the high logic level of a2 is also reduced since the transistors $N1$ and $N2$ are both ON. When the input vector is changed to [a2,b2] = [0,1], the transistor $P1$ is turned ON and the output voltage is the result of voltage division between the resistances R_{P1} and $Rgd + R_{N3}$. In the case of $R_{P1} << Rgd + R_{N3}$, the output goes to logic 1 and the gate functions correctly. When $R_{P1} >> Rgd + R_{N3}$, the output voltage is very low and is detected by the DC test [a2,b2] = [0,1]. When R_{P1} and $Rgd + R_{N3}$ are approximately equal, the output voltage is close to V_{mid} and the transition incurs a large delay. This large delay causes the delays of driven gates to increase as well as discussed in Section V. Another observation is that the Rgd threshold for single pattern DC detection has weak dependence on the driving resistance of the transistor network connected to the NAND2 input due to active (negative) feedback between the output voltage and the resistance R of transistor N1.

An interesting point to note is that for the NAND2 gate of Figure 2, the three vector pairs ([1,1],[0,1]), ([1,1],[1,0]) and ([0,1],[1,1]) detect all gate open and transistor drain or source open defects. However, to detect all drain-source, gate-source and gate-drain shorts, an additional vector pair ([1,0],[1,1]) is also needed. In general, to detect all transistor stuck-open faults on transistor terminals of an n-input NAND gate, $n+1$ vector pairs are needed. To detect in addition, all transistor shorts as above, $2n$ test vector pairs are necessary.

IV. Critical Resistance and Delay Impact

In an n-input NAND gate, drain-source shorts on the N-type transistors in the pull-down chain of the gate with low values of Rds are detected by a DC test (e.g. vector [a2,b2]=[0,1] for the NAND2 gate of Figure 2). A DC test response can also be modeled as an infinitely large rise time of the gate output signal "out" in response to the two-vector pattern ([1,1],[0,1]). As Rds increases, this rise time decreases from ∞ to a large value and the signal "out" settles to a final DC value just larger than V_{mid} (or the logic threshold of the succeeding gate). As Rds increases further, the rise time becomes smaller and the signal settles to a value closer to Vdd, until it exhibits fault-free behavior. As an example, consider the drain-source short given by Rds of transistor $N1$ of Figure 3. The Y-axis shows the voltage at the node *out* and the X-axis shows time (the vector [a2,b2] = [1,1] transits to [a2,b2]=[0,1] at 10nS). The switching threshold is considered as 50% of Vdd for simplicity. As can be seen Rds values less than 3.8K are detectable with DC tests. Rds values between 3.8K and 8.75K are detectable with delay tests and Rds values larger than 8.5K are deemed fault-free.

Corresponding arguments as above, can be posted for gate-source and gate-drain shorts in other N-type and P-type transistors as well as for other types of logic gates including complex gates (e.g. AOI). The problem then is to compute a value for Rds, Rgs or Rgd, as the case may be, that is *not DC test detectable* (assuming that the DC measurement made within a finite time of test application is *independent of prior applied inputs*), is not fault-free, but *incurs the largest cumulative delay along a selected circuit path*. The corresponding value is defined to be the *critical resistance value*. It is seen that for this critical resistance value, the corresponding path delay can be *as large as 50X-80X of a single gate delay*. We argue that tests corresponding to such defects need to be prioritized in

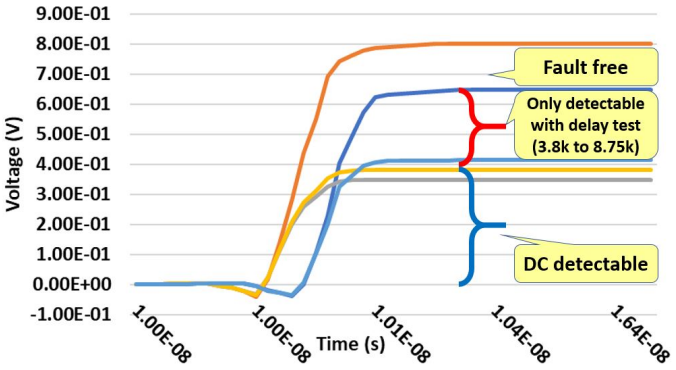

Fig. 3: Transient response for varying Rds in transistor $N1$ of NAND2 gate

the global test selection process.

In our experiments, the critical resistance $R_{critical}$ is found using an adaption of Bisection Algorithm. The algorithm starts with a large resistance interval with DC detectable lower bound R_L and DC undetectable upper bound R_H. In each iteration, testbench is simulated with defect size being the midpoint of the interval, $R_M = (R_L + R_H)/2$. If R_M is DC detectable, R_L is replaced with R_M, else R_H is replaced with R_M. The iterations successively reduce the size of the interval and stop when the interval is sufficiently small, making R_H a sufficiently good approximation of $R_{critical}$.

V. Experimental Results

We run experiments on the circuit of Figure 2 to prove our hypothesis. In addition, we also run experiments on NAND3, NAND4, AOI standard cells (DUTs) and ripple carry adders where the faulty NAND2 gate (DUT) of Figure 2 is replaced with these circuits. Resistive short defects (Rgd, Rds and Rgs) are injected between the gate-drain, drain-source and gate-source terminals of each MOSFET of the DUT. We use a chain of 2 fault-free inverters to drive the DUT inputs and a chain of 4 fault free inverters connected to the cell output terminated by a load capacitance *COUT* to model a logic path containing the DUT. CMOS standard cells from the Nangate standard cell library [19] based on NCSU 45nm FreePDK technology are used.

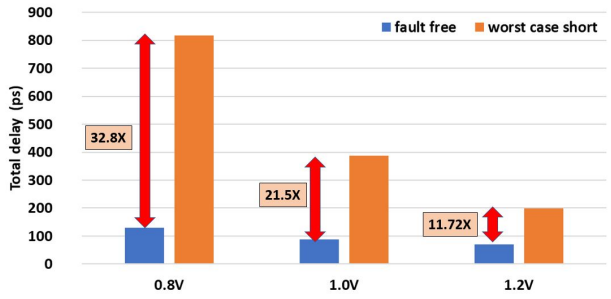

Fig. 4: Total delay increase vs. Vdd: critical gate-source short

(a) Defect sensitivity w.r.t. Vdd: We show path delay experiments for different supply voltages when a defective cell with a short is in the path as shown in Figure 4. We consider three different supply voltages: 0.8V, 1.0V and 1.2V. The fault considered is a gate-source short Rgs in transistor $N1$ of Figure 2. For each supply voltage, we show the path delay through all the inverters of Figure 2 for the fault free circuit and for critical values of Rgs. The Y-axis of Figure 4 shows the total delay in picoseconds (ps), the blue bars represent the fault free case and the orange bars represent the delay with critical resistance. The increase in delay is shown by the *delay increase factor*, which is the total path delay increase w.r.t. the fault free delay of the NAND2 gate. The total delay increases by 32.8 times for 0.8V, by 21.5 times for 1.0V and 11.72 times for 1.2V. It can be seen that maximum delay increase is seen for the lowest Vdd considered, which suggests that the circuit should be tested at the *lowest* of the three supply voltages. The analysis of supply voltage recommendation for very low voltage testing is presented in [20].

(b) Defect sensitivity w.r.t. defect location: Figure 5 shows the results of path delay experiments for the test circuit of Figure 2 for Rgs, Rds and Rgd short defects in transistor $N1$. The Y-axis shows the total delay in ps, blue bars show the fault free delays, orange bars show the delay for the resistive short of value 1kohm above the critical resistance and the gray bars show the total delay for the critical resistance value. It can be seen that for all the faults, the delay increases to its maximum value when the short resistance value approaches its critical value $R_{critical}$. Another observation is that gate-source and drain-source shorts have a much larger impact on total path delay as compared to gate-drain shorts.

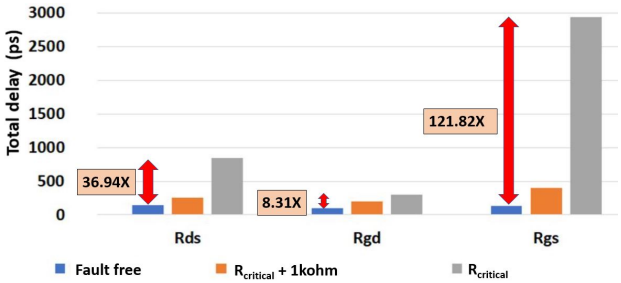

Fig. 5: Total delay increase vs. defect location: NAND2 $N1$

(c) Delay distribution analysis: Figure 6 shows the relative delay increases (in percentage terms) in different gates along a path consisting of the faulty NAND2 gate and inverters of Figure 2 with gate-source (path delay increase of 121.8X), gate-drain (path delay increase of 8.3X) and drain-source (path delay increase of 36.9X) critical resistance values inserted into the transistor $N1$ of gate G3 (faulty NAND2 gate) in Figure 2). It can be seen that the delay increase distribution is different for each kind of defect. For the gate-source short defect, the delay increase is the largest for the faulty gate G3_f while the rest of the gates exhibit comparatively lower delay increase. For the drain-source defect, the largest delay increase is seen in the gate G4. This is also discussed in Section III. It is observed from these experiments that although the short defect is restricted to only gate G3 (NAND2 gate) in Figure 6, 17%, 98% *and* 87% *of the increase in path delay* for gate-

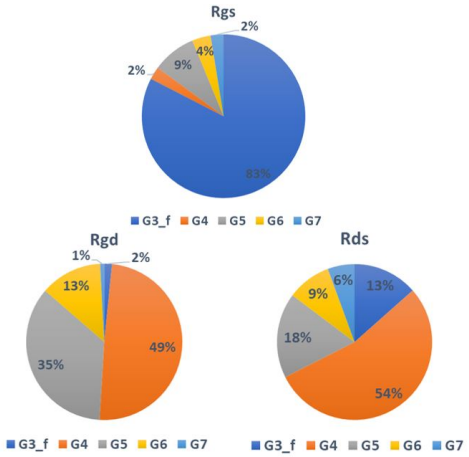

Fig. 6: Delay distribution vs. defect location: NAND2 $N1$

source, gate-drain and drain-source shorts in G3, respectively, *is contributed by the fault-free logic gates along the path*. Another observation from this experiment is that gates further away from the defective gate experience less delay increase.

(d) Defect sensitivity w.r.t. number of inputs: In this experiment, the faulty gate in Figure 2 is replaced by 2, 3 and 4 input NAND and NOR standard cells and simulation of short defects on different transistors is performed. We show results for path delay increase due to gate-source short defects in the pull down network consisting of N-type transistors of 2, 3 and 4-input NAND gates, NAND2, NAND3 and NAND4, respectively, in Figure 7. Blue, orange, grey and yellow bars represent transistors $N1$, $N2$, $N3$ and $N4$ of the gates as applicable. The transistor $N1$ is the N-type transistor closest to the gate output with $N2$, $N3$ and $N4$ of gates NAND2, NAND3 and NAND4, respectively, connected to the ground terminal. It can be seen that the delay increase due to short defects is larger as the number of inputs to the gate increases for a fixed defect location. Within an NAND gate, the delay increase is highest (460X) for defect in transistor $N1$ and lowest for defects in transistors connected to the ground terminal.

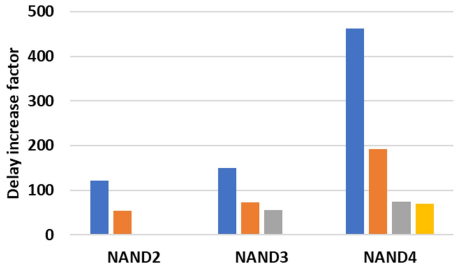

Fig. 7: Total delay increase vs. number of inputs: NAND Rgs

(e) Delay increase experiments on ripple carry adder (RCA): To investigate the impact of short defects in standard cells embedded in combinational circuits, we replace NAND2 with an 8-bit Ripple Carry Adder in the circuit of Figure 2. The defect is injected into a NAND2 gate within one of the full adders of the RCA testbench (Figure 8), which consists of 72 NAND2 gates and 6 inverters. Input A is set to [a0,a1,...,a7] = [1,1,...,1] and input B is set to [b0,b1,...,b7] = [0,0,...,0]. An input transition is injected to the carry-in signal C_{in}, which is driven by a chain of 2 fault-free inverters. Similar to the test circuit for a single standard cell, the output C_{out} also drives a chain of 4 fault-free inverters. The propagation delay is measured along the critical path of the circuit, from the input C_{in} to the output C_{out}. The bisection algorithm is used to determined the critical resistance of each defect. A key point to note is that the critical resistance value for a specific transistor terminal short defect within a gate depends on the location of the gate within the RCA circuit.

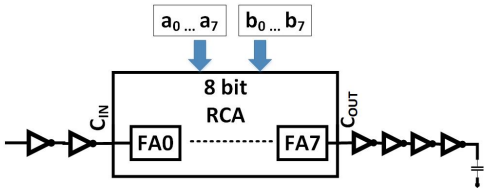

Fig. 8: Test circuit for shorts defect analysis in a 8-bit RCA

We analyse the full adder circuit to identify the short defects that can be sensitized and propagated to the circuit outputs based on the two-vector pattern discussed earlier. Figure 9 shows the NAND logic implementation of a full adder. Only gate G5 and gate G9 are located in the critical path from C_{in} to C_{out}. It is observed that only the short defects in transistors $N2$ and $P2$ of gate G5 and the short defects in transistors $N1$ and $P1$ of gate G9 are activated by the applied test. The total number of detectable short defects in each full adder is thus 12. For each full adder, we insert drain-source short defects Rds at 2 different locations within the adder: transistors $N1$ of G9 and $N2$ of G5. A similar analysis is then performed for the NOR logic implementation of the full adder circuit. The number of defect locations remains the same for this case as well.

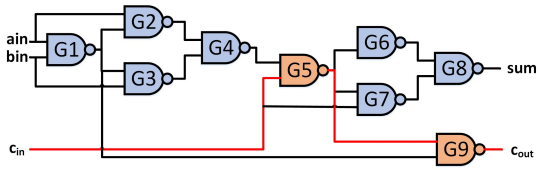

Fig. 9: Full adder using NAND2

Experiments for defects at various locations in the critical path of the ripple carry adder are performed for NAND and NOR based RCA implementations. The delay increase for the drain-source short defect in G5 described above for FA0, FA4, and FA6 is shown in Figure 10. The different bars show delays for FA0 (blue) to FA7 (brown) for fault free and faulty cases. The faulty full adder experiences the most increase in delay while a distributed delay increase effect is observed in the next full adder stage. The effect diminishes after 3 stages (including the faulty FA).

Figure 11 shows the delay increase due to a drain-source short in gate G9 of FA0 , FA4 and FA6 (described earlier)

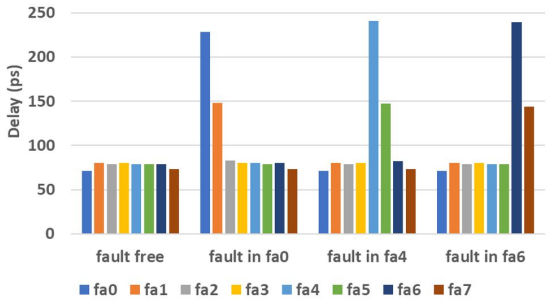

Fig. 10: Delay increase analysis for NAND2 based RCA: Fault in gate G5

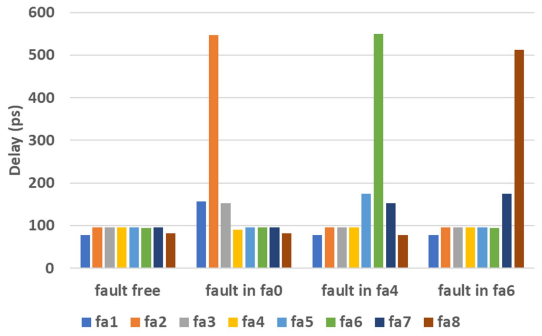

Fig. 11: Delay increase analysis for NOR2 based RCA: Fault in gate G9

in the NOR gate implementation of the RCA. Note that the relevant drain-source short in gate G9 of FA0 has a greater impact on the delay of the following gate in the sensitized path of the RCA. As seen earlier, the delays of multiple full adders along the sensitized RCA path are affected. For the experiment of Figure 10, the total RCA path delay increase for the drain-source short defect in $N2$ of gate G5 is from a nominal value of 620ps to 850ps on average, which is 3.2 times the delay of a full adder with NAND logic and 10.5 times the delay of a single 2 input NAND gate. Similarly, for Figure 11, the total path delay increase for the drain-source short defect in $N1$ of gate G9 is from a nominal value of 729ps to 1289ps on average, which is 7.18 times that of a full adder with NOR logic and 16 times the delay of single 2 input NOR gate.

(f) Delay impact experiments for different shorts resistances: Experiments were conducted to explore how the total path delay (see Figure 2) increase is impacted by variations around the critical gate-source and drain-source resistive short values on transistors $N1$ and $N2$ of NAND2, NAND3 and NAND4 gates (see Defect type in Table I). Delay factor increases are shown for different shorts resistance values ($R_{critical}$, $R_{critical} + 0.5K$, $R_{critical} + 1K$, $R_{critical} + 2K$) around the corresponding critical resistance value. It is evident that not only the delay increase is highest at the critical defect resistance value but a significant delay increase persists for values up to 2-3K ohm around the critical value as shown.

(g) Broader studies to investigate vulnerability to shorts with significant delay impact: Experiments were performed to find

TABLE I: Delay increase vs critical resistance

		Delay factor increase			
Defect type	Rc (ohm)	Rc	Rc+0.5k	Rc+1k	Rc+2k
NAND2RgsN1	4.21K	121.8X	21.5X	11.8X	6.1X
NAND2RdsN1	3.43K	36.9X	10.1X	6.0X	3.3X
NAND2RgsN2	4.29K	54.7X	13.4X	7.6X	3.8X
NAND2RdsN2	1.56K	18.4X	3.9X	2.3X	1.2X
NAND3RgsN1	4.29K	150.0X	41.1X	23.1X	11.0X
NAND3RdsN1	2.34K	30.3X	9.1X	5.8X	3.1X
NAND4RgsN2	4.45K	462.6X	108.4X	55.3X	22.0X
NAND4RdsN2	0.07K	6.8X	6.0X	5.3X	4.0X

the critical resistance value for short defects in cells NAND2, NAND3, NAND4, NOR2, NOR3, NOR4, AOI21, OAI21. Drain-source, gate-source and gate-drain shorts in different transistors of the above library of gate designs are simulated. For each defect, the delay increase factor relative to the fault-

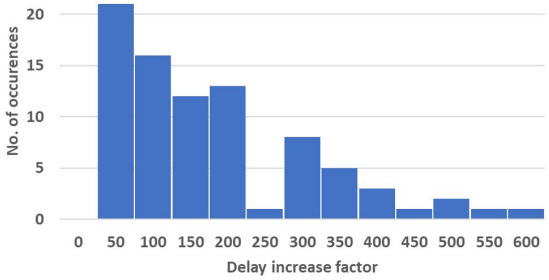

Fig. 12: Delay factor increase for critical resistances

free gate is calculated for the corresponding critical shorts resistance value. Figure 12 shows a histogram of the delay increase factor vs. no of occurrences across all defects in N-type and P-type transistors of the cells considered. It is seen that for specific defects the delay increase factor was greater than 600X.

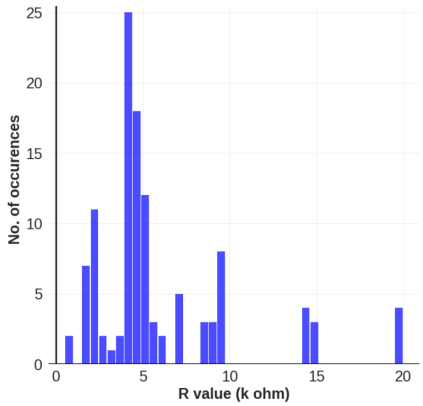

Fig. 13: Critical short defects analysis

Figure 13 shows the distribution of short defect values in increments of 500 ohms in N-type and P-type transistors for the same experiment above, that result in an increase of $> 5X$ in delay compared to the fault-free delay for the cells considered. A very interesting observation is that shorts resistance values from 1K-20K ohm result in delay increases of $> 5X$. This falls well within the domain of shorts resistance

values typically seen in practice [21], [22] *indicating the very practical and increased vulnerability of CMOS logic to the shorts defects studied in this research*.

VI. Conclusions

Short defects in standard cells are typically tested using DC tests. In this work, we show that for critical short defect resistance values two pattern delay tests are needed to test these defects. We investigate strong short defects (low resistance defect) which can escape the traditional DC testing and are exclusively detected by specific two pattern delay tests and can cause exceptionally high (up to 600X) path delay increase across interconnected logic gates. We further show that the resistance of short defects which cause these delays range from 1-20K ohm which are also *practical short defect resistance values seen in manufactured ICs*, hence the tests for such defects must be prioritised.

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