A Low-cost Novel Method to Fabricate Integrated Magnetic Core Inductor Embedded in Organic Substrate

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The strong demand for 3D packaging technology has accelerated the miniaturization of passive devices, and inductors are facing challenges because the inductance value will be sacrificed when the size is shrinking. Adding magnetic core is one of the solutions due to its enhancement of inductance density but it will also add complexity to the fabrication process. However, previous research [1-3] shows that the performance enhancement brought by the magnetic core could be shadowed by the process complexity. A novel method to fabricate the magnetic core inductors on flexible substrates is proposed in this work. The inductor has a stacking structure of three layers: the Cu trace layer, and the two layers of magnetic core (under and above the Cu). The Cu trace is patterned by the wet etch process on the flexible PCB, a polyimide layer is then coated and planarized on the Cu surface as insulation, and the upper layer magnetic core is directly sputtered on the Cu trace layer. For the lower magnetic core layer, a polyimide layer on the carrier wafer is prepared as the substrate and it is also patterned by the liftoff process. Then, the finished layers are aligned and bonded with a flip-chip bonder with high precision and efficiency. Before the whole fabrication process, the device patterns are designed and optimized by the finite element analysis software. Finally, the finished devices are measured with the radiofrequency probe station. The result shows that the inductance density and the quality factor of the magnetic core inductor could be 3.61 nH/mm^2 and 6.22, respectively, with the device size being only 0.95 mm^2. Compared with the air core inductor with the same Cu trace pattern, the magnetic core inductor elevates the inductance by 10% and still keeps the same low profile, of which the thickness of the whole device is within 100 μm. These parameters are measured and extracted at 100 MHz and this is the potentially used frequency for the power delivery applications such as the in-chip integrated voltage regulators.

***Index Terms*—magnetic core, organic substrate, integrated inductor, packaging.**

I. INTRODUCTION

Currently, the trend to miniaturize the passive components has been boosted by the development of semiconductor industry, including the new packaging technology, the scaling down of the devices, and the emerging application scenarios. For example, the in-package air core inductor (ACI) was used for the Fully Integrated Voltage Regulator (FIVR) module, starting from Intel's 22nm node CPUs (Haswell) [4]. Owning to the relatively large footprint and thick substrate, the ACIs had a high quality factor in the beginning, which, however, would be challenged because of the shrinking footprint and the thinner substrate core. Most of the parameters of ACIs, such as the inductance, DC resistance (R_{DC}), are proportional to the number of coils, and trace width, respectively, suggesting a severe performance drop as the chip size continues to scale down. The magnetic inductor array (MIA) was first introduced in the 10th generation Intel CPUs (14nm node), with an iron-alloy based nanoparticle (NP) mixed in epoxy matrix being used as magnetic core, of which the inductance is 2.5-3.0 nH [5]. Compared with ACIs, the MIAs take about half of the area and the thickness is below 180 μm. Moreover, the coaxial magnetic integrated inductor (Coax MIL) is also under development, which is directly fabricated in the plated through hole (PTH) in the substrate core layer with a straight Cu trace surrounded by the magnetic core, which requires smaller footprint and is more suitable for mobile CPUs [6].

The other application, automotive electronics, places emphasis on footprint/size, integration compatibility, and mechanical stability. Details of the latter two factors are different from the cases in the Intel's examples. The working condition requires the substrate material to be more durable under high temperature and wide-range vibration, indicating that more complex packaging form like heterogeneous packaging has to be considered [7]. Under this circumstance, integration compatibility with polyimide, FR4, or even ceramic materials is important to the passive components [8]. For instance, an embedded inductor in eWLB (Embedded Wafer Level Ball Grid Array) package is able to better suppress the voltage-controlled oscillator (VCO) phase noise, compared with the on-chip inductor, directly elevating the integration density and the system performance of the automotive radar transceiver module [9].

In the two applications that have been mentioned above, the demand for die size scaling and the substrate thickness shrinking has put the air core inductor in a dilemma because the inductance and R_{DC} would deteriorate and further affect the quality factor or efficiency of the whole module. Adding the magnetic core is a solution to improve the inductance deterioration (such as Intel's MIA, MIL) [5, 6], but the additional integration complexity cannot be ignored. Also, the selection of the magnetic materials also affects the integration compatibility with the substrate materials. Metallic NP mixed in epoxy matrix has been implemented due to its low deposition difficulty. However, the permeability of these materials is relatively low (less than 10) and the inductance enhancement is limited [6]. Another option is to use the sputtered alloys, which have a much higher permeability, but the substrate requirement for the sputter process is stricter [10]. Also, the stacking of the different layers (magnetic core layers, Cu trace layers) has to be finished by multiple lithography process, which comes with several baking process and high cost [2]. So far, each kind of topology of the Cu trace have been investigated intensively, such as spiral[11, 12], solenoid[13], and toroidal[14].

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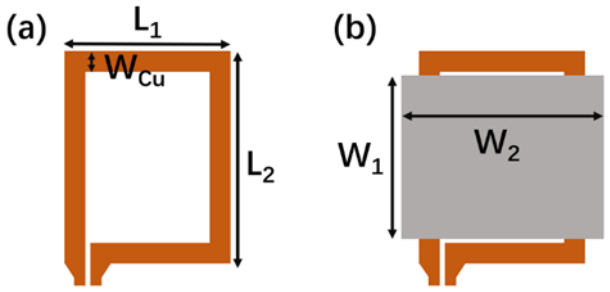

Fig.1 The schematic diagrams of the (a) air-core inductor and (b) magnetic core inductor. The key parameters and their annotations are indicated in the diagram.

Incorporated with the magnetic core, it has been reported[11-14] these inductors can achieve 30-100 nH when the frequency is lower than 100 MHz, nonetheless, the large device area (3-10 mm2) and DC resistance (above 0.2 Ω) would result in difficulty to the integration into the power delivery module and sacrificing the efficiency ratings. Basically, the total length of Cu trace required by the complicated topology and the interface of the Cu Via[15] are responsible for the two issues mentioned above. Under this circumstance, the straight line one-turn magnetic core inductor would be a solution to lowering the DC resistance and miniaturization.

In this report, a novel process method to fabricate the integration inductor with dual-layer magnetic core will be presented, which is an extension of the group's prior work on both rigid [16, 17] and organic substrates [18]. Basically, the inductor trace is made on a commercially available flexible PCB with the wet etch process, of which the thickness of Cu layer is 18 μm to obtain a low DC resistance. The magnetic core is fabricated with sputter and patterned by a standard lift-off process, enabling its good compatibility with the semiconductor process used in industry. In the device assembly step, the flip-chip bonder was utilized, providing a fast and well-aligned bonding. The following RF/DC measurement results show that the magnetic core can effectively increase the inductance by 10%, while it can still keep the low-profile form factor, low DC resistance (15 mΩ) and the finished device shows great flexibility and provides a good potential for the integration into various package forms.

II. Inductor Design and Simulation Result

There are several methods to increase the inductance. In the aspect of the topology, adding the number of turns of the Cu trace is straightforward for a solenoid or a spiral structure. However, the high DC resistance (series resistance) could downgrade the efficiency of the whole module in most of the applications[19-22]. Also, the proximity effect caused by the multiple-turn inductor would further decrease the efficiency as the frequency elevates[23, 24]. Our goal is to use a simple structure of the Cu trace to suppress DC/AC resistance and improve the inductance by adding the magnetic core.
Four prototype designs of the inductors were examined in the Ansys Maxwell software, including the two magnetic core inductors and their non-core version with only the Cu trace. The schematic diagram is shown in Fig.1 and the parameter details are listed in Table I. Besides, the gap between the magnetic core and the Cu trace is 15 μm in the simulation and the thickness of Cu/magnetic core is 18 μm and 3 μm, respectively, in both simulation and the fabricated devices. The gap in the device will be described later in the next part about fabrication. And each device has two contact pads for both ends of which the width is designed to be 65 μm. For the magnetic core material, the permeability is 107 and the saturation magnetization is 1.4 Tesla. The simulation results are shown in Table II, including the inductance, AC resistance and the quality factor of air-core/magnetic-core for design1 and design2.

Table I The parameters of the two inductor prototype designs (μm)

	design-1	design-2
L_1	430	1116
L_2	3460	1410
W_{Cu}	130	130
W_1	3000	1000
W_2	400	1330

Table II The simulation results (100 MHz) of the two prototype designs

	design-1		design-2	
	mag.-core	air-core	mag.-core	air-core
L (nH)	3.67	3.12	3.19	2.37
ACR (Ω)	0.339	0.086	0.203	0.058
Q factor	8.02	22.84	9.18	25.74

III. Fabrication Process

A. *Cu Pattern Preparation*

The flexible PCB Cu sheet was commercially purchased from PCBWay and is used as the Cu layer. This material consists of 18μm thick Cu and 25μm thick cured polyimide and it is widely used for the flexible or wearable device fabrication, and as the substrates of MEMS sensor. After the flexible PCB was attached to the handling wafer, the pattern of the inductor traces was achieved with a wet etch process, as shown in Fig.2(a)(b). First, the AZ4330 photoresist was spin coated on the Cu surface and patterned after exposure; then the flexible PCB with photoresist was immersed into the CE-100 Cu etchants for 10 minutes till the inductor trace patterns can be observed clearly. A finished 2"×2" Cu layer is shown in Fig.3(a).

B. *Magnetic Core Preparation*

The two layers of the magnetic core are designed to be above and below the Cu inductor traces, respectively. The 3 μm magnetic core was laminated into 15 layers with the oxide layers made by creating the oxygen ambient in the sputter chamber between each two laminations, which can suppress the eddy current. The upper and the lower core layers were

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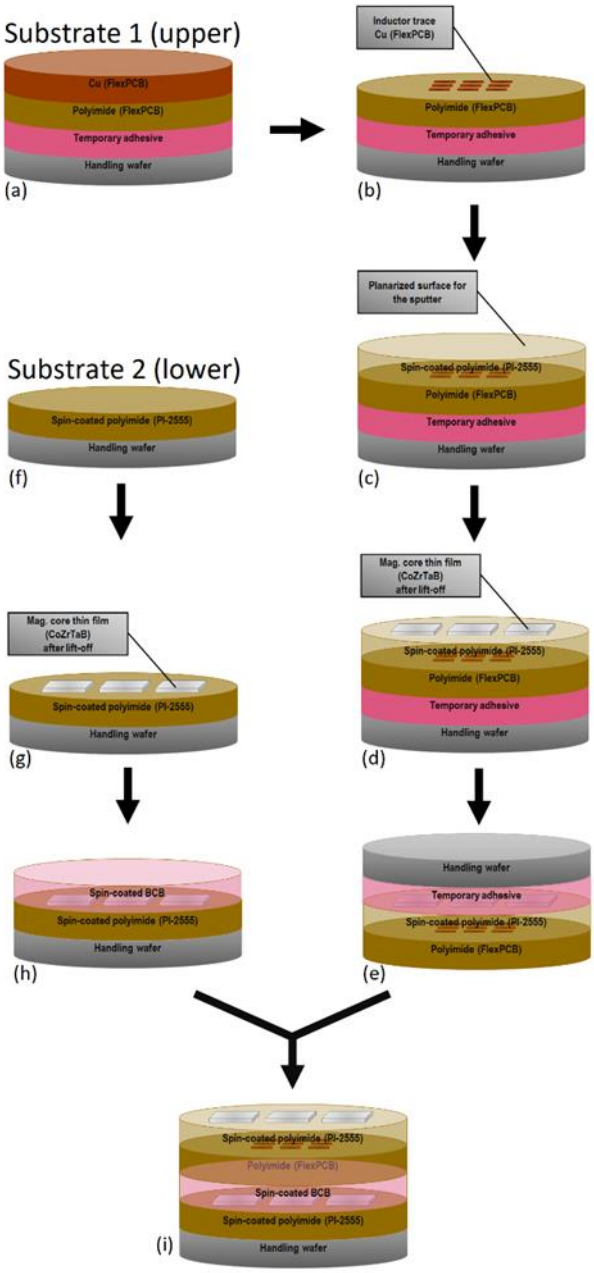

Fig.2 Fabrication flow chart. The upper layer fabrication process: (a) Flexible PCB attached on a handling wafer. (b) Cu trace pattern finished with wet etch. (c) A planarized polyimide layer added on the Cu trace. (d) Magnetic core patterned by lift-off. (e) Another handling wafer attached to this layer. The lower layer fabrication process: (f) Polyimide on handling wafer. (g) Patterned magnetic core on polyimide. (h) Coating BCB on the magnetic core layer. (i) Finished device after bonding.

fabricated in a same sputter session, but their substrates were prepared separately.

After the PI-2555 polyimide precursor was spin coated and cured on the handling wafer (Fig.2(f)), the lower core layer was sputtered on this polyimide substrate to fundamentally guarantee its compatibility to the different packaging form factors. Then the core pattern was made by a standard lift-off process (Fig.2(f)) with the nLOF 2070 photoresist, which was

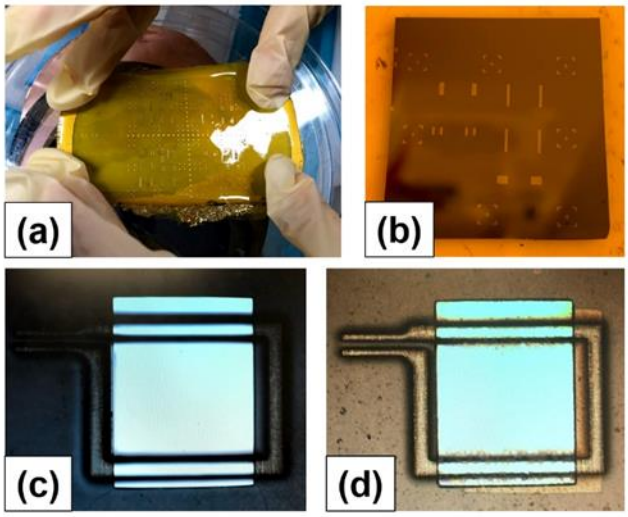

Fig.3 The partially finished device part. (a) The finished Cu trace based on FlexPCB. (b) The finished lower magnetic core pattern on cured polyimide. (c) The finished Cu trace covered with the upper magnetic core. (d) The finished whole device.

initially spin coated at 1500 rpm to achieved 9 μm thickness. Fig.3(b) shows the microscopic view of the after-lift-off lower core pattern.

The upper core layer (shown in Fig.3(c)) was also made with the same lift-off process; however, a relatively complicated substrate preparation is needed. For this upper core layer, the finished Cu layer could be regarded as its substrate, but the uneven surface of the Cu pattern would be a challenge to the magnetic core sputtering. Consequently, an additional planarized insulation layer between the Cu layer and the upper core layer is needed.

C. Final Assembly

The last step is to use the flip-chip bonder manufactured by Fintech to bond (align and attach) the two layers: (a) the lower core layer (Fig.2(h)); (b) the finished "combination" of the Cu layer and the upper core layer (Fig.2(e)). The upper layer was first removed from the original thermal release tape (temporary adhesive in Fig.2(d)), and then attached to another handling wafer with the same temporary adhesive tape (Fig.2(e)). The two handling wafers can protect the surface and enable a good attachment to the vacuum mount of the flip-chip bonder. After this, the BCB (Cyclotene) was spin-coated for the final bonding, which has a good adhesion with polyimide surface and the curing temperature is relatively low (250°C). During the bonding process, the thermal and pressure were also provided by the flip-chip bonder. The finished devices are shown in Fig.2(i) and Fig.3(d).

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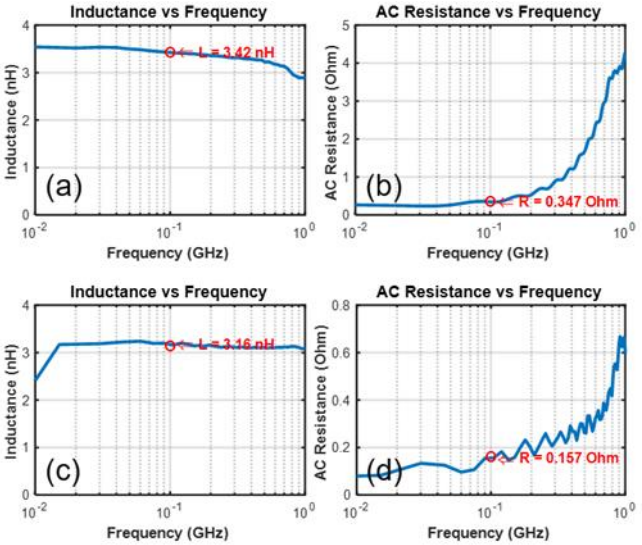

Fig.4 The measurement results of (a) inductance and (b)AC resistance of magnetic core inductor (design1); and (c) inductance and (d) AC resistance of the air core inductor (design1). The frequency range is from 10 MHz to 1 GHz.

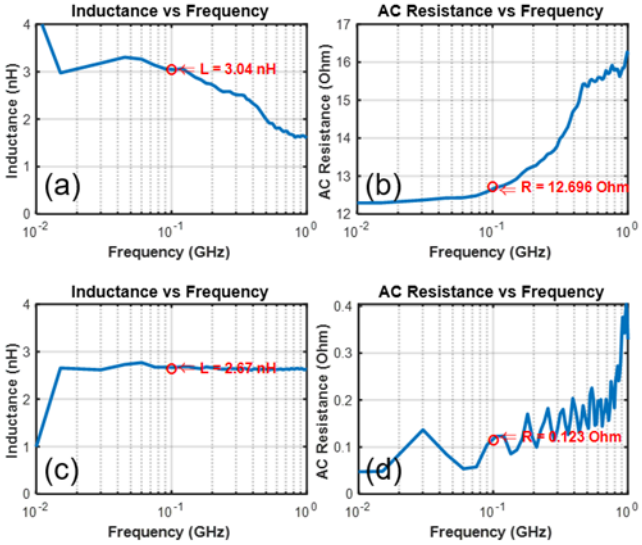

Fig.5 The measurement results of (a) inductance and (b) AC resistance of magnetic core inductor (design2); and (c)inductance and (d) AC resistance of the air core inductor (design2). The frequency range is from 10 MHz to 1 GHz.

IV. Measurement Results and Analysis

A. Inductance

Generally speaking, the addition of magnetic core can bring 10%-15% inductance enhancement for the two designs under the frequency from 10 MHz to 200 MHz, which covers a large portion of the applications, such as the integrated voltage regulators or the power management module of processors. To be more specific, the design1 magnetic core inductor achieves 3.42 nH at 100 MHz, providing a high inductance density of 3.61 nH/mm^2. Beyond 200 MHz, the air core inductors demonstrate a more attractive performance because no inductance degradation appears within this frequency range, as shown in Fig.4(c) and Fig.5(c).

Compared with the simulation results discussed previously, the measured inductance loses 7.3% and 4.9% of its value, respectively. This difference can be explained by the large value of the actual distance between Cu layer and core layer, the offset created by the bonding process, and the de facto hysteresis loop (magnetization-applied field) plot varying from the settings in the simulation. The first two factors can be eliminated by optimizing the fabrication process or the material selection; the last one was caused by the surface roughness and the sputter condition [18], and it has been reported that compare with the thin film on Si substrate, the CoZrTaB thin film on rougher surface shows a lower saturation magnetization and higher anisotropy field [10].

The effective permeability is determined by the following equation[25]

$$\mu_{eff} = \frac{M_S}{H_{eff}} = \frac{M_S}{H_k + N_d M_S} = \frac{1}{\frac{H_k}{M_S} + N_d} \qquad (1)$$

where M_s is the saturation magnetization, H_k is the anisotropy field, and N_d is the demagnetization factor. As a result, the lower M_s and the higher H_k introduced by the fabrication process both diminish the permeability, disadvantaging the inductance value of the device.

B. DC/AC Resistance and Quality Factor

For the DC resistance of both design1 and design2, the measured value is 15 mΩ, even after the magnetic core was added. The elimination of Cu Via successfully keeps the DC resistance at a very low level.

For the AC resistance of design1 in Fig.4(b)(d), both of the air core and magnetic core inductor only show dramatical increase beyond 200 MHz, while the measured value at 100 MHz of magnetic core inductor matches the simulation result (the deviation is only 2.4%) much better than the air core inductor (the deviation is 82.6%). The measured value of the air core design2 still shows the similar deviation (112.1%) compared with the air core design1, but the extremely high AC resistance of the magnetic core design2 inductor indicates that, empirically, some unexpected factor compromised the measurement condition, such as the severe surface oxidation, the improper probing caused by the uneven surface or the deformation of the substrate.

As for the quality factor, it is highly related to the inductance and the AC resistance. Both of the two air core inductors demonstrate relatively high value, of about 14, extracted at 100 MHz, while the two magnetic core inductors vary a lot (6.22 for design1 and 0.16 for design2).

V. Conclusion

In this paper, the fabrication process of a multilayer integrated inductor was described in detail, which is highlighted by the utilization of the flip-chip bonder. This will greatly ease the fabrication complexity and bring more opportunities to implement the multilayer stacking structure to the integrated inductor. The measurement result shows that the added

symmetric double layer magnetic core can increase the inductance by 10%. And it has great potential to further improve the performance if the surface treatment or a better technology to planarize the polyimide is applied, or the core thickness is increased linearly. On the other hand, the air core inductor based on the wet etch flexible PCB shows stable inductance value and low AC resistance under a large frequency range. Also, the whole device is fabricated on organic flexible substrate and the good DC/AC resistance suppression can be extended to above 100 MHz, enabling the possibility many application scenarios like the in-package or on-package inductor for redistributed layer (RDL), wearable electronics, communication/power module of mobile devices, in which the high integration-flexibility or the dimension restrictions are required.

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