Electro-Thermal Device-Package Co-Design for Ultra-Wide Bandgap Gallium Oxide Power Devices

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***Abstract*— The ultra-wide bandgap (UWBG) of Ga_2O_3 allows it to achieve over nearly 10^{33}-times lower intrinsic carrier concentration than silicon (Si), permitting Ga_2O_3 devices to operate at much higher temperatures. However, its low thermal conductivity and the associated self-heating could cause the device to exceed its safe operating temperature as prescribed by the gate dielectric, device passivation, and packaging material limitations. The objective of this study is to develop an electro-thermal device-package co-design modeling framework for Ga_2O_3 power semiconductors. A series of models were built to integrate the physics-based material/device-level model with a package-level thermal finite element analysis (FEA) model. These models were then evaluated against more traditional methods of device and package simulation to understand the potential benefits of such a method.**

Keywords*—*gallium oxide, ultra-wide bandgap semiconductor, electro-thermal co-design, packaging

I. Introduction

There is a compelling need for power electronics components and systems capable of operation at ambient temperatures exceeding 250 °C in automotive, aerospace, military, and down-hole applications [1] [2]. However, the inherent limitation of semiconductors is the concentration of intrinsic carriers, which increases with temperature. Thanks to the UWBG of Ga_2O_3 (4.8 eV, compared to 1.1 eV for Si, 3.2 eV for SiC, and 3.4 eV for GaN), it achieves nearly 10^{33}-times lower intrinsic carrier concentration than Si. Furthermore, compared to Si, SiC, and GaN devices, unipolar Ga_2O_3 devices have a superior theoretical limit for the tradeoff between on-resistance and breakdown voltage, enabling higher power conversion efficiency and power density. High-voltage Ga_2O_3 diodes have been demonstrated to steadily operate at high temperatures up to 327 °C [3].

While Ga_2O_3 shows promise in these respects, due to its low thermal conductivity a traditional approach to modeling and package design may not be suitable. The low thermal conductivity (over 20-times lower than that of SiC) causes most conventional packaging and cooling strategies to be insufficient, resulting in higher peak temperatures and thermo-mechanical stresses during operation. Recent experimental work shows that junction-side or double-side cooling are essential for Ga_2O_3 devices [4].

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In the co-design of a device and its associated packaging, it is critical to accurately observe the thermal interactions and account for the self-heating of the device that may cause high internal junction temperatures and leakages [2]. This becomes even more important in the higher-temperature/power applications offered by Ga_2O_3 devices, where thermal management is paramount to the successful and reliable operation of compact and power-dense electronics packages [5].

Typical package-level FEA simulations usually assume a uniform power dissipation over the junction side of the device and measure the resulting temperature distribution while neglecting the electro-thermal effects such as drift-diffusion, electron concentration/scattering, and lattice heating that occur in the sub-micron device structures. Conversely, the typical physics-based TCAD simulations more-accurately model the electro-thermal behaviors within the device, but simplifies the packaging into a nominal boundary thermal resistance or heat extraction coefficient, neglecting larger packaging elements in the heat flow path (e.g., the substrate and baseplate) [6]. It is anticipated that these interdependencies will be paramount when dealing with a low-thermal-conductivity material that will inevitably exhibit higher overall temperatures, greater temperature differences, and potentially larger thermo-mechanical stresses. This work seeks to understand the interactions between the device layout and packaging structures and how their designs affect each other by developing a co-design modeling strategy to quantify and mitigate the limitations of typical modeling methods. In addition, to ascertain the impacts of the lower thermal conductivity of Ga_2O_3, SiC devices, which have over 20-times higher thermal conductivity than Ga_2O_3, were also simulated and trends between the two device types were analyzed. Lastly, the proposed electro-thermal co-design was used to explore the impacts of the device dimensions and junction-side-cooling on the junction temperature.

II. Modeling Methodologies and Rationale

In this work, several modeling methods were explored for the electro-thermal device-package co-design simulations. The first method selected was a commonly used 3D FEA simulation where an averaged power distribution is applied equally over the surface of a solid object with the properties of the bulk semiconductor material to represent the device. The resulting temperature distribution due to joule heating is observed. This method is widely used due to its low computational demands

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and ability to model not only the heat interactions between material interfaces but also a convection coefficient at the boundary. However, to achieve a more accurate representation of the device temperature distribution, an electro-thermal model that can solve the current continuity, drift-diffusion, heat generation, and the heat diffusion equations (many of which are temperature dependent) to derive the electrostatic potential, electron concentration, and lattice temperature is needed [7]. The lack of consideration of the micro-/nano-scale device structures, lattice-based heating, and electron scattering, which influence the device heating and resulting temperature distribution and may limit the thermal modeling accuracy.

2D and 3D physics-based TCAD models account for these device physics effects, but the high computational power required due to the large difference in length scales between the electrically-active regions (e.g., nanometer-sized edge termination structures and drift regions) and the thermal diffusion regions (e.g., millimeter-sized packaging structures) as well as the more involved iterative method physics-based solution method limits their use when package components need to be considered. 2D TCAD models do not account for 3D heat spreading, which can reduce the accuracy of the thermal model [8]. While 3D TCAD models account for this heat spreading, they require a more involved meshing strategy, which is challenging when multiple design iterations are needed. In addition, these methods do not have the ability to model a convection coefficient and are limited to conductive heat transfer [9].

In order to directly compare the modeling methodologies an additional body to emulate the convection coefficient in a "thermal node" method (similar to that described in [10]) was used. The convection coefficient for the thermal node is found by taking the power dissipated and dividing by the temperature at the thermal boundary of the FEA simulation and then again at some known distance away from the boundary, taking the difference and multiplying by the area (1).

$$k = \frac{P}{(T_{boundary} - T_{node})\, l_{node}\, w_{node}} \quad (1)$$

where k is the convection coefficient, P is the power dissipation, $T_{boundary}$ is the peak temperature at the applied thermal boundary condition, T_{node} is the peak temperature at the on the bottom surface of the thermal node, l_{node} is the length of the thermal node, and w_{node} is the width of the thermal node.

To achieve the fast simulation time of FEA with the device-physics modeling of TCAD, it has been proposed in the literature to use a combination of these two thermal modeling methodologies [11]. The combination of TCAD and 3D FEA provides an accurate representation of the device while reducing computational intensity when simulating the package structures. In this work, it is proposed to use 2D TCAD to design for electrical parameters (e.g., edge termination and breakdown voltage), and then transfer the device to a 3D TCAD model to account for 3D heat spreading while maintaining the physics-based electro-thermal effects. The resulting device temperature distribution is then exported and used as a load condition in the 3D FEA simulation for full package thermal and thermo-mechanical simulations. This method can reduce the computational demand of the full package thermal simulations while maintaining the more accurate electro-thermal distributions provided by the physics-based models. The co-design process flow is shown in Fig. 1.

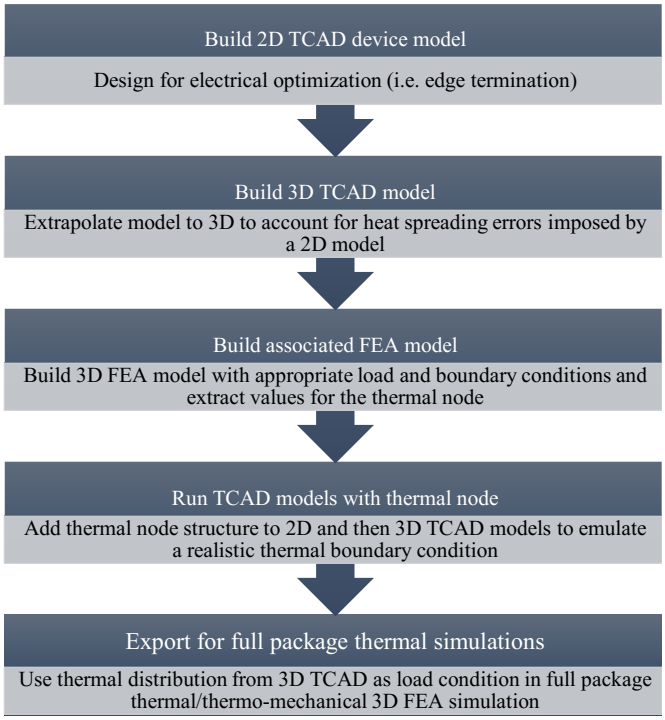


Fig. 1. Proposed co-design process flow

A summary of the benefits and limitations for the proposed FEA and TCAD simulations and the combination of the two for a packaged device are provided in Table I. In this work, ANSYS Workbench was selected as the FEA software and Silvaco TCAD was chosen for the TCAD software.

TABLE I. MODELING METHODOLOGIES

Method	Benefit(s)	Limitation(s)
ANSYS Workbench	Quick solve time/ability to model convection coefficient	No electron scattering/no micro or nano scale device structures
Silvaco TCAD 2D	Accurate electro-thermal interactions	Potential 2D-3D heat spreading differences/no convection model
Silvaco TCAD 3D	Accurate electro-thermal interactions	Very long solve time/no convection model
TCAD → 3D ANSYS	Quick solve time/accurate device level electro-thermal interactions	Static junction temperature

III. CO-DESIGN SIMULATION SETUP

The structure, load, and boundary conditions shown in Fig. 2 were implemented in 3D FEA, 2D TCAD, and 3D TCAD models. Despite being common electro-thermal simulation tools, a direct comparison between the models still holds value in evaluating whether or not the higher computational demands

of the physics-based TCAD models are warranted or if a sufficiently accurate temperature distribution is attainable from an FEA model. This comparison will be made by applying identical loads and thermal boundary conditions (emulated by the thermal node for use in the TCAD models and validated against the FEA model). The results of these simulations will be used to evaluate the benefits and limitations of the FEA, 2D TCAD, 3D TCAD, and proposed combined TCAD/FEA modeling methods for device-package co-design.

The die thickness, area, and anode diameter were 500 µm, 25 mm^2, and 3 mm diameter. These dimensions were selected according to the recently-fabricated large-area vertical Ga_2O_3 Schottky rectifier reported in [12]. This diode has been fabricated at the Center for Power Electronics Systems at Virginia Tech, and will be used to experimentally validate the simulation results in the future. This diode shows a forward current over 20 A and reverse blocking voltage of about 600 V. The thicknesses of the direct bonded copper (DBC) substrate were 0.38 mm and 0.2 mm for the AlN ceramic and copper, respectively, and the area was selected based on a 45º heat spreading assumption such that the full heat interaction between the device and the first-level packaging could be observed.

As previously stated, one of the most attractive features of Ga_2O_3 is its low intrinsic carrier concentration which enables high-temperature operation. As such, the load condition of 10 W and the thermal boundary condition of 500 W/m^2K were selected based on a resulting junction temperature of 350 ºC for the Ga_2O_3 device baseline case. This will allow us to observe the thermal behavior at elevated temperatures where Ga_2O_3 devices are promising.

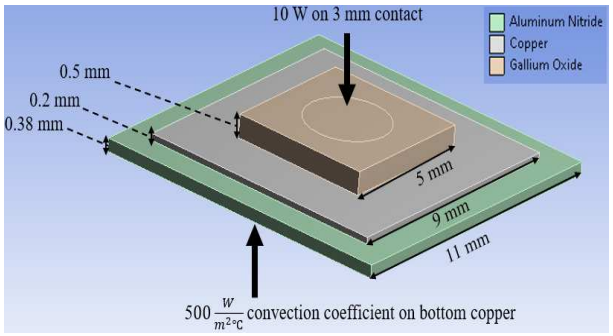


Fig. 2. Model dimensions, load conditions, and boundary conditions used in all simulations.

Fig. 3 depicts the device structure used in the TCAD models [12]. This device has a Ni/Au Schottky contact with SiO_2 edge termination structures and a Ti/Au ohmic contact. The n^- epi layer has a doping concentration of 2.1 x 10^{16} cm^{-3} while the n^+ bulk substrate has a doping concentration of 1.3 x 10^{19} cm^{-3}. All together the device has a total thickness of just over 500 µm. Fig. 4 shows the 2D TCAD model with the DBC substrate and thermal node applied. The thermal node emulates the convection coefficient and serves as the thermal boundary condition.

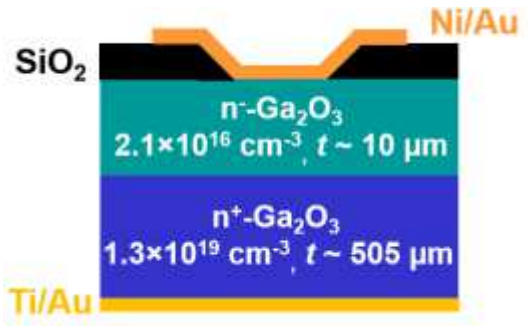


Fig. 3. Large area Ga2O3 Schottky barrier diode [13].

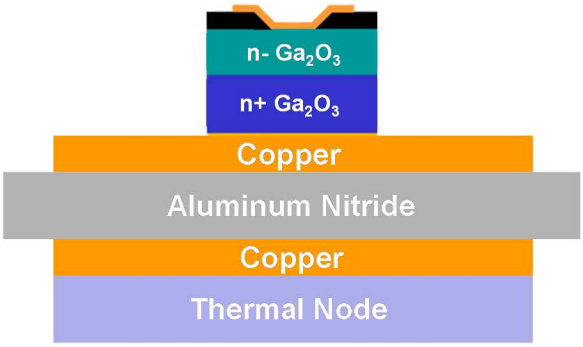
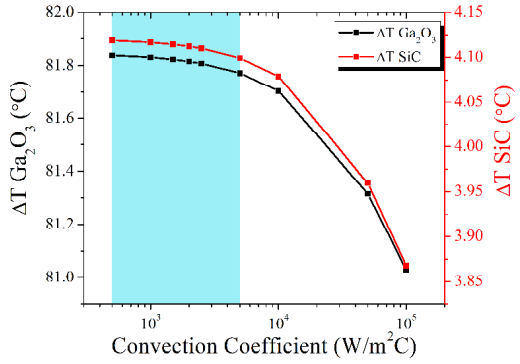


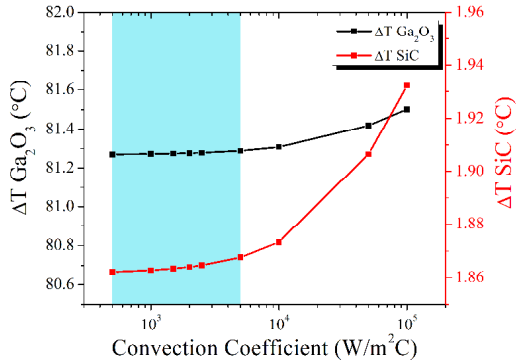
Fig. 4. 2D TCAD model of the Ga_2O_3 Schottky barrier diode, DBC substrate, and thermal node strucure to emulate the convection coefficient.

To establish a suitable thermal boundary condition for the thermal node, ANSYS Workbench was used to evaluate the influence of the convection coefficient and the thermal conductivity of the semiconductor device on the heat spreading/temperature distribution across the anode surface and vertically through the center of the device. Both a Ga_2O_3 diode with a thermal conductivity of 14 W/mK [14] and a SiC diode with a thermal conductivity of 370 W/mK [15] were simulated, and the convection coefficients for each were swept. This comparison was intended to observe if the thermal distribution in the die would be affected by the low thermal conductivity of Ga_2O_3 under differing convection coefficients or if it would follow a similar trend to the much higher thermal conductivity of SiC.

The resulting temperature profiles for the Ga_2O_3 and SiC diodes are shown in Fig. 5. As can be seen in the highlighted areas, there is negligible difference in heat through or across either device for convection coefficients between 500 and 5,000 W/m^2K. This suggests that even though the peak and overall temperatures may differ for the two semiconductor materials, very similar trends in thermal performance can be seen when the same cooling strategy is employed. The convection coefficient for the remaining simulations was decided to be 500 W/m^2K.



(a)



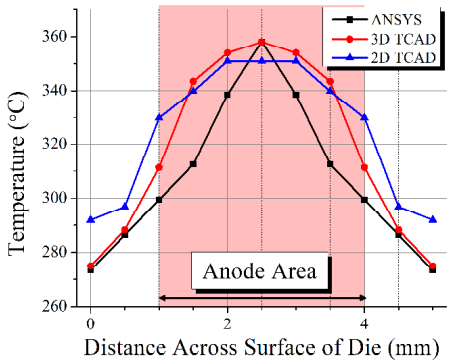
(b)

Fig. 5. Temperature difference vs. convection coefficient (a) across the anode surface (from the center of the die to the edge of the die) and (b) vertically through the device (from the center top to the center bottom) for Ga_2O_3 (black) and SiC (red).

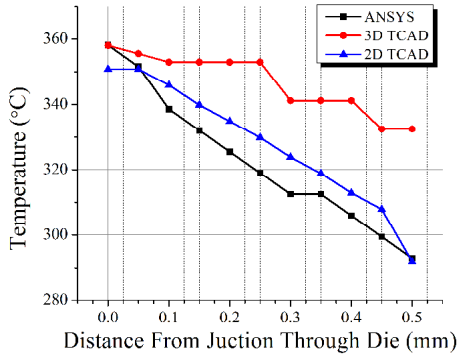
The final step in validating the FEA and TCAD models against each other was to choose an appropriate meshing strategy. The electrically active areas of the TCAD models, not present in the FEA simulations, were meshed with a triangular element size of 3 μm^2 to accurately these smaller fixtures, while the rest of the model was meshed on a grid of 150 μm^2 triangular elements to match that of the ANSYS model where convergence of the steady-state thermal simulations was found. The ANSYS and TCAD models of the bottom-side-cooled diode were then cross-checked against one another using the applied voltage and current densities of the TCAD models to confirm that the desired power dissipation of 10 W over the 3 mm anode surface was being met. The resulting junction temperatures were in close agreeance, which gave confidence that the thermal node was accurately emulating the desired convection coefficient.

IV. Modeling Method Comparisons

The resulting temperature distributions for each model were compared to evaluate how well their resulting temperature distributions agree and where they diverge. The simulated peak temperatures for the three models show approximately 2 % difference. However, as can be seen in Fig. 6, while the temperature difference, ΔT, across the Ga_2O_3 diode surface and vertically through the device for the FEA and 3D TCAD simulations were in close agreement, the 2D TCAD simulation showed more than a 30 % and 10 % difference, respectively. Furthermore, the temperature distribution across the anode area in the FEA model has a steeper decline compared to the TCAD models; the FEA model shows 30 °C lower temperature at the outer edge of the device anode compared to the TCAD models. This discrepenancy can be attributed to the lattice-heating constants and electron scattering effects that are accounted for in the physics-based TCAD simulations, which are neglected by the FEA simulation. These differences could impact both the device and packaging designs governing the material selections and layout considerations to better spread and extract heat from the junction.



(a)



(b)

Fig. 6. Temperature (a) across the Ga_2O_3 diode anode surface (from the center of the die to the edge of the die) and (b) vertically through the Ga_2O_3 device (from the center top to the center bottom) for each modeling method.

Table II lists the key parameters from the FEA and 2D and 3D TCAD models from the simulation of the bottom-side cooled diode shown in Fig. 2. The power dissipation area of the FEA model was restricted to that of the anode contact of the TCAD models to more accurately reflect the power density, heat generation, and tempeature distribution compared to when the power dissipation is applied to the entire top surface of the die.

Based on these findings, a commonplace FEA simulation alone may not sufficiently model potential hot spots, which represent areas most likely to experience the highest levels of thermo-mechanical stress and strain. In [5], several thermal distributions were modeled by varying the cooling strategy for a set device size and thermal load. A 20 % difference in maximum versus minimum strain energy density was observed in the die-

attach layer as a result of the temperature variations. This indicates that a differing thermal distribution can influence the thermo-mechanical stress and strain induced in a package and should be accounted for as accurately as possible during the design stage.

TABLE II. MODELING METHOD COMPARISONS

Method	Solve Time	Peak Temperature	ΔT Across Ga2O3 Diode Surface	ΔT Through Ga2O3 Diode
ANSYS Workbench	~2 minutes	358 °C	85 °C	65 °C
Silvaco TCAD 2D	~7 minutes	351 °C	59 °C	59 °C
Silvaco TCAD 3D	~13 minutes	358 °C	85 °C	68 °C

V. IMPACT OF DEVICE DIMENSIONS ON THE THERMAL PERFORMANCE

One central benefit of this co-design technique is the ability to account for the thermal impacts of the device parameters and the resulting thermal distribution of an entire larger packed device. This permits for analysis of the relationship between device structures and the resulting junction temperature and thermal distribution. Some similar studies have been reported in the literature. In [16], the influence of the device substrate thickness and crystal orientation on the device temperature was evaluated. However, only the device was modeled, and the only thermal boundary condition applied was the thermal conductivity of the bulk substrate which may not be representative of the thermal distribution that occurs when heat is extracted from the device.

In this work, the device thickness, area, and anode diameter were varied to evaluate their impact on the thermal performance. The same power dissipation and thermal node from the previous section were used for each case. Ga_2O_3 and SiC devices were simulated for each case to observe if these variations follow similar thermal trends for semiconductors with different thermal conductivities (14 W/mK for Ga_2O_3 and 370 W/mK for SiC).

A. Device Thickness

Device substrate thinning has been shown to be an effective method of reducing the junction-to-case thermal resistance. In [17], reducing the substrate thickness of an SOI GaN HEMT power device from 500 µm to 100 µm yielded a 35 % reduction of the self-heating thermal resistance. For a set power dissipation, device side length, contact size and thermal boundary condition, a reduction in junction-to-case thermal resistance and in turn a reduction in junction temperature should be observed. Fig. 7 shows the resulting junction temperatures of simulations where the diode substrate thickness was varied from 100 µm to 500 µm (the thickness of commercially available Ga_2O_3 wafers). As expected, the lower junction-to-case thermal resistance provided by thinned substrates shows a 20 % reduction in junction temperature for the Ga_2O_3 device. A similar trend but of lesser magnitude is both expected and observed in the SiC case as its thermal resistance is significantly lower.

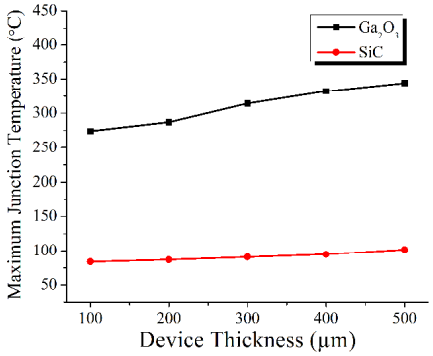


Fig. 7. Device thickness versus junction temperature for Ga_2O_3 and SiC.

B. Device Area

Increasing the device area is another effective way to reduce the junction-to-case thermal resistance. In [18], an increase of the chip length (and in turn the available area for heat spreading) from 0.5 mm to 1 mm while maintaining a set contact size reduced the thermal resistances of a GaN LED by 50 %. In this work, the side length was varied while the power dissipation, contact size and thermal boundary condition were held constant. Fig. 8 shows the resulting junction temperatures for 500-µm-thick devices with areas ranging from 5 mm^2 to 8 mm^2. While the contact area would normally also be scaled with device area, the contact area remained static to observe whether providing additional bulk substrate to widen the heat spreading angle would be an effective method to reduce the junction temperature. This showed a nearly negligible impact on junction temperature for both devices, indicating that altering the device side length alone may not be an effective way of reducing the junction temperature.

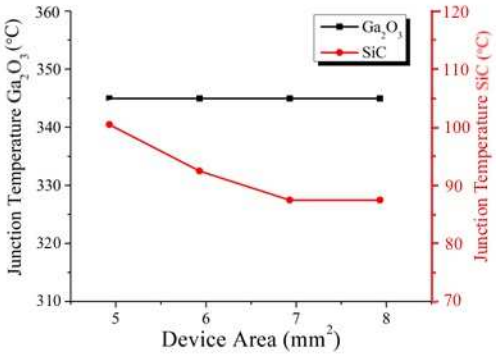


Fig. 8. Device area versus junction temperature of Ga_2O_3 and SiC.

C. Contact Area

An increase in contact area for the same power dissipation, thermal boundary conditions, device side length and deice thickness will in turn decrease the power seen per unit area on along the contact and the associated losses which generate the heat along the contact. This was shown in [19] to be an effective

way to reduce the overall junction temperature for the same applied power. Increasing the anode contact size (i.e., the active area) spreads the power dissipation and therefore the heat over a larger portion of the die, which reduces the peak junction temperature. Fig. 9 shows similar trends between the SiC and Ga_2O_3 devices and confirms that by increasing the contact area size the junction temperature can be greatly reduced. In this instance, both nearly converge to the ambient temperature prescribed by the thermal boundary with the SiC device approaching that value more rapidly than the Ga_2O_3 device.

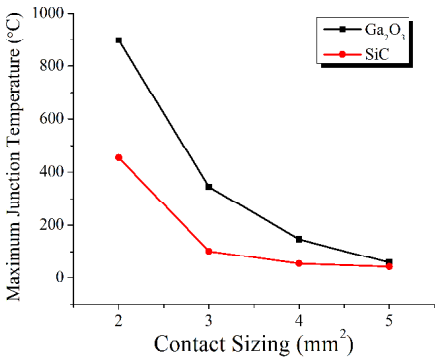


Fig. 9. Device contact area versus junction temperature for Ga_2O_3 and SiC.

D. Summary

Overall, the trends between the SiC and Ga_2O_3 devices are in good agreement, with the magnitude of the Ga_2O_3 junction temperature remaining higher due to the lower thermal conductivity. This means that the substrate thinning is more effective for the Ga_2O_3 device comparatively as it will more meaningfully reduce the overall thermal resistance of the device. Little to no impact is made on junction temperature for both materials by increasing the device area (for the same contact area). Increasing the anode contact size proved to be the most effective method to reduce junction temperature, reducing the temperature of the Ga_2O_3 to the same temperature as the SiC when the full top surface of the device was utilized as the contact surface at the same power dissipation.

Table III summarizes the effectiveness of the different device structure modifications that were explored. They are compared to the baseline case which had a junction temperature of 344ºC.

TABLE III. IMPACT OF GA_2O_3 DEVICE DIMENSIONS ON THERMAL PERFORMANCE

Parameter	Base Case	Range	Min. Junction Temperature	Reduction from Base Case
Substrate Thickness	500 µm	100 – 50 µm	274 ºC (at 100 µm)	20 %
Device Area	5 mm²	5 – 8 mm²	343 ºC (at 8 mm²)	<1 %
Contact Area	3 mm²	2 – 5 mm²	58 ºC (at 5 mm²)	84 %

VI. BOTTOM SIDE VS. JUNCTION SIDE COOLING OF A GA_2O_3 DEVICE

As previously stated, junction-side or double-side cooling are essential for the successful Ga_2O_3 devices and has been experimentally [4]. This stresses the importance of a model being able to efficiently model different package and cooling options. Using the proposed co-design process, a junction-side-cooled model for the Ga_2O_3 diode was built. The device and substrate dimensions as well as the load and boundary conditions were the same as those in Fig. 2. The device was then rotated such that the junction side was bonded to the substrate. This resulted in a peak junction temperature of 249°C which is a 30 % reduction in overall junction temperature from the baseline case. This thermal management is paramount to the operation of these devices at high temperatures and power levels.

VII. CONCLUSION

This work outlines and evaluates an electro-thermal device/package co-design model. This process can be utilized for the efficient and accurate modeling of a Ga_2O_3 device including any hot spots caused by self-heating and their effects on its associated packaging. Several commonplace modeling methodologies were compared, and it was ascertained that a combination of FEA and TCAD models was warranted for an accurate and efficient electro-thermal codesign. This co-design method was then used to explore the impact of device parameters on the temperature distribution. The anode contact area was found to have a significant impact on the device junction temperature and the trends between SiC and Ga_2O_3 devices were similar through all device variations. The co-design platform was then used to simulate a junction-side-cooled configuration for the Ga_2O_3 diode, which yielded a 20-% reduction in the peak junction temperature. Further simulations are needed to validate this methodology for transient load conditions. These simulations should then be eventually verified experimentally through use of thermal imaging.

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