Optimization of Suzuki Stack Circuit to Reduce Power Dissipation

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***Abstract*—Superconductor–semiconductor hybrid circuits can combine the benefits of the high-speed and low-power operation of single-flux quantum circuits and high integration densities of CMOS technology such as memory. The Suzuki stack, a type of Josephson latching driver/amplifier, is a widely used interface circuit in Josephson–CMOS hybrid memories. Due to the limited cooling power at cryogenic temperatures, the power dissipation is becoming an important concern, especially in large-scale systems. An optimization technique to significantly reduce the power dissipation of Suzuki stack circuits is proposed in this article. The proposed design can reduce the power dissipation by 30–70% while causing a voltage drop of 2–9% in the output voltage depending on the circuit parameter configuration. The tradeoffs between the power dissipation and output voltage characteristics are discussed. The proposed design can operate correctly within at least ±20% of process parameter variations as demonstrated with extensive simulations.**

***Index Terms*—Suzuki stack circuit, Josephson latching driver/amplifier, Josephson–CMOS memory, superconductor–semiconductor interface circuits, power dissipation.**

I. Introduction

SUPERCONDUCTING digital electronics, particularly, single-flux quantum (SFQ) circuits can operate at frequencies of tens to hundreds of gigahertz while consuming low power in the order of zJ (zepto J) [1]–[4]. However, large-scale SFQ-based memory is difficult to realize due to the low integration densities [5], [6]. Therefore, there is a need to interface the superconducting electronics with semiconductor (CMOS) technology.

A Suzuki stack (a.k.a., Josephson latching driver/amplifier) is a superconductor–semiconductor interface circuit, first proposed in 1988 by Suzuki *et al.* [7] and still widely used in Josephson–CMOS hybrid memory [8]–[10]. The primary advantages of a Suzuki stack circuit as compared to other interface circuits (e.g., superconducting quantum interference device stack [11], [12], SFQ-to-dc converter [1], [13]) are higher output voltage, on the order of tens to hundreds of millivolt, smaller area [few Josephson junctions (JJs)], and faster operation.

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A Josephson–CMOS hybrid memory uses the Suzuki stack and CMOS amplifier circuits to convert SFQ pulses to CMOS-level voltage signals. For instance, a 64-kb hybrid Josephson–CMOS random access memory (RAM) operating at 4 K has been demonstrated in [9]. In this system, the Suzuki stack circuit is designed to produce the output voltage of 60 mV, with an average power dissipation of 165 μW. The 12-b address inputs, one read, one write, and 16-b data inputs are required to access the 64-kb RAM. As a result, 30 Suzuki stack circuits are needed (i.e., one for each input signal). During the read and write operations, Suzuki stack circuits dissipate 2.31 mW and 4.95 mW, which corresponds to 19.5% and 23.6% of total read and write power, respectively. At 4.2 K, the cooling power is limited to around 1–1.5 W [14], [15], depending on the size of the cryostat. In large-scale systems (e.g., data centers and cloud computing), the improvement in power dissipation in order of tens of milliwatt becomes highly important. For example, Konno *et al.* [16] have proposed a technique to reduce the power dissipation in Josephson–CMOS hybrid memory, where the total write power has been reduced by 15.2 mW. Note that this technique focuses only on the CMOS part of the hybrid memory (decoders, memory cells, and data drivers). Additionally, a nanocryotron (nTron) proposed in [17] has been demonstrated to operate as an interface circuit between SFQ and CMOS circuits [18]. As compared to a Suzuki stack circuit, an nTron has lower area, higher output impedance, and lower power dissipation. A 64-kb Josephson–CMOS hybrid memory with nTrons would consume 0.78 mW and 2.20 mW of read and write power, respectively [19]. Nevertheless, nTron devices have several limitations such as a relatively large thermal transition time in the order of 100 ps (whereas the delay of Suzuki stack is reported as 47 ps in [9]) and immature fabrication technology, which should be refined to produce higher output voltages without using CMOS amplifiers [19]. The state-of-the-art Josephson–CMOS hybrid memory that interfaces SFQ microprocessor [10] still uses Suzuki stack circuits, which consumes a considerable portion of total power dissipation. This article focuses on the reduction of power dissipation in the Suzuki stack circuit.

The following are the key contributions of this article:

1) An optimization technique is proposed to reduce the power dissipation in the Suzuki stack circuit.
2) The proposed optimization technique considers the *I–V* (current–voltage) characteristics of a JJ, which is a basic building block of the Suzuki stack circuit. Accordingly, the nonequal critical current values of a JJ and nonequal distribution of current in left and right branches of a Suzuki

stack circuit are used to add another degree of freedom during the design process.

3) Operating conditions are analytically determined to maintain the specified margins.
4) Tradeoffs such as power dissipation, output voltage, propagation delay, and fall time of the output voltage are analyzed and compared. The proposed technique is, therefore, flexible for a circuit designer to optimize multiple design targets and choose appropriate tradeoffs.

The rest of the article is organized as follows. The concept and *I–V* characteristics of an underdamped JJ are explained in Section II. The operation principle of a Suzuki stack circuit and its possible limitations are discussed in Section III. The proposed optimization technique is presented in Section IV. The conclusions are drawn in Section V.

II. Underdamped JJs

A JJ is a two-terminal device that consists of two electrodes made from superconductor material, which are separated by a weak link. This link weakens the superconductivity between the two layers and could be made of an insulating material, nonsuperconducting metal, or a certain physical constriction [20]. The most widely used type is a superconductor–insulator–superconductor type (e.g., $Nb/AlO_x/Nb$ materials) [3].

The switching behavior of a JJ can be classified as underdamped ($\beta_c \gg 1$) or overdamped ($\beta_c \ll 1$), where β_c is the Stewart-McCumber parameter [3]. This parameter is often controlled with an external resistor connected in parallel to the JJ. This article focuses only on underdamped JJs as underdamped JJs have been widely used in the latching logic, which was actively developed in 1980–1990s [23]–[28]. Besides the latching logic, underdamped JJs are also used in Suzuki stack circuits, which is explained in Section III.

In underdamped JJs, once the current that is flowing through the device exceeds the critical current I_c, the JJ switches from superconducting to a resistive state. The voltage across the JJ in the resistive state is referred to as the gap voltage V_g. The *I–V* (current–voltage) characteristic of underdamped JJs is shown in Fig. 1. As shown in Fig. 1, underdamped JJs exhibit a hysteric behavior, i.e., once the JJ is in the resistive state, it remains in this state even if the current becomes smaller than the critical current. The superconducting state can be achieved by resetting the current to a near-zero value (in Fig. 1, this value is around 10% of the critical current).

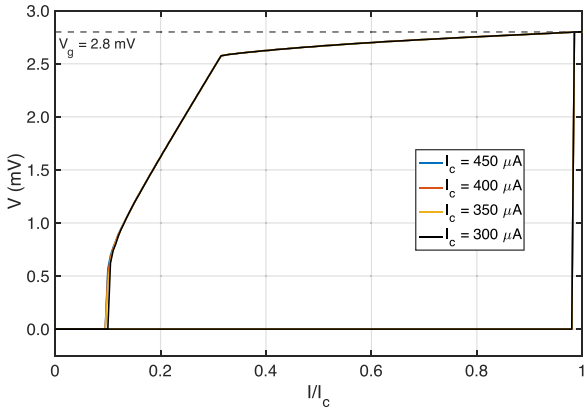

Fig. 1. *I–V* characteristics of underdamped JJs with the critical current of 300–450 μA. The JJ is simulated as a Verilog-A RCSJ model in MIT-LL SFQ5ee 10-kA/cm^2 process [21] by using Cadence Virtuoso schematic editor and Spectre simulator. Underdamped behavior is achieved by connecting in parallel (shunting) resistance of $R_{\rm sh} = 6V_g/I_c$ and inductance of 20 pH [22]. Four lines overlap each other. The Stewart–McCumber parameter β_c ranges from 3.74 to 15.7.

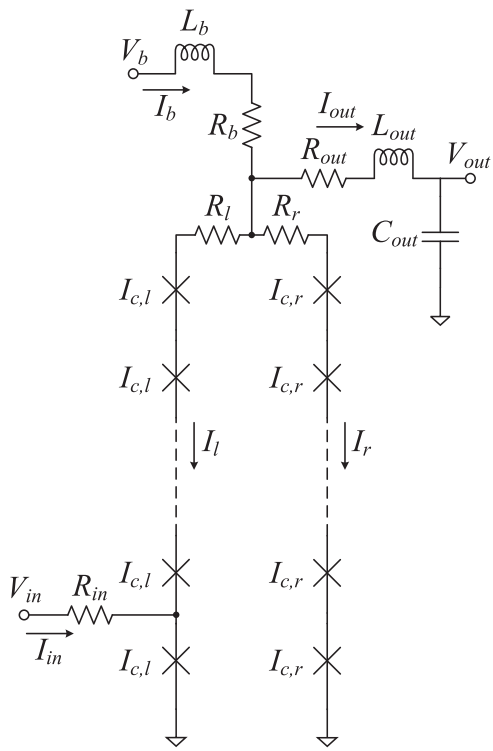

Fig. 2. Schematic of the Suzuki stack circuit.

III. Suzuki Stack Circuits

A. Operation Principle

The schematic of the Suzuki stack circuit is depicted in Fig. 2, which consists of two (left and right) branches connected in parallel. Each branch contains multiple (underdamped) JJs connected in series. The number of JJs that are connected in series determines the output voltage of a Suzuki stack circuit. For example, for N-number of JJs connected in series, the voltage on top of the stack would ideally be equal to NV_g.

The operation of a Suzuki stack circuit is illustrated in Fig. 3. The circuit parameters are selected from [22] and listed in Table I. An underdamped JJ with a critical current of 400 μA is used similar to Fig. 1. Before the input signal arrives, all JJs are biased to around 80% of the critical current (i.e., superconducting state). When the input signal arrives, the input current $I_{\rm in}$ is equal to 140 μA. As a result, the current through the lowermost JJ in the left branch exceeds the critical current, forcing it to switch into the resistive state. Since the left and right branches are no longer

TABLE I
PARAMETERS OF A SUZUKI STACK CIRCUIT FOR VARIOUS DESIGNS

Parameter	**Original from [22]**	$\frac{I_l}{I_b} = 0.50$	$\frac{I_l}{I_b} = 0.55$	$\frac{I_l}{I_b} = 0.60$	$\frac{I_l}{I_b} = 0.65$	$\frac{I_l}{I_b} = 0.70$	$\frac{I_l}{I_b} = 0.75$	$\frac{I_l}{I_b} = 0.80$
Bias voltage V_b	500.0 mV	420.0 mV	381.8 mV	350.0 mV	323.1 mV	300.0 mV	280.0 mV	262.5 mV
Left branch resistance R_l	4.0 Ω	4.0 Ω	3.6 Ω	3.2 Ω	2.8 Ω	2.4 Ω	2.0 Ω	1.6 Ω
Right branch resistance R_r	4.0 Ω	4.0 Ω	4.4 Ω	4.8 Ω	5.2 Ω	5.6 Ω	6.0 Ω	6.4 Ω
Left branch critical current $I_{c,l}$	400 μA	350 μA	350 μA	350 μA	350 μA	350 μA	350 μA	350 μA
Right branch critical current $I_{c,r}$	400 μA	448 μA	407 μA	373 μA	344 μA	320 μA	298 μA	280 μA
Left shunt resistance $R_{sh,l}$	42.0 Ω	48.0 Ω	48.0 Ω	48.0 Ω	48.0 Ω	48.0 Ω	48.0 Ω	48.0 Ω
Right shunt resistance $R_{sh,r}$	42.0 Ω	37.5 Ω	41.3 Ω	45.0 Ω	48.8 Ω	52.5 Ω	56.4 Ω	60.0 Ω
Parasitic series inductance of JJ	0.13 pH *							
Bias resistance R_b	750 Ω							
Bias inductance L_b	200 pH							
Input voltage V_{in}	7 mV							
Input resistance R_{in}	50 Ω							
Output resistance R_{out}	50 Ω							
Output inductance L_{out}	100 pH							
Output capacitance C_{out}	180 fF							

*Value was not specified in [22], taken from [29].

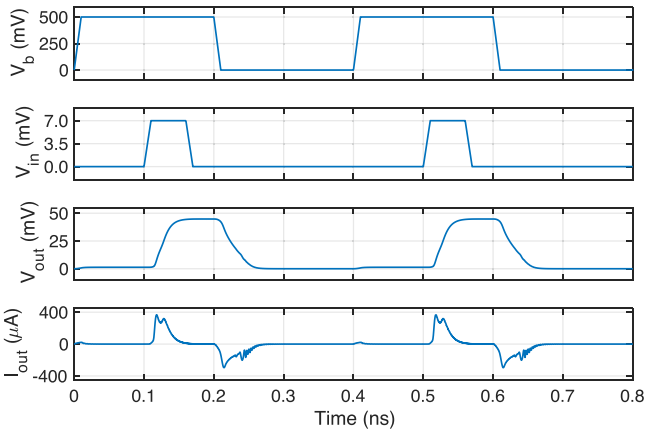

Fig. 3. Operation of a Suzuki stack circuit with 16 JJs connected in series.

symmetric after the lowermost JJ in the left branch becomes resistive, most of the bias current I_b starts to flow through the right branch. Hence, the entire right branch is switched into the resistive state. After that, the portion of bias current flows back to the left branch, where the remaining JJs are finally switched into the resistive state. The output voltage of approximately 44.8 mV remains high even after the input signal becomes low (see Fig. 3). This behavior can be explained by carefully examining Fig. 1. When the input signal is low, all JJs are biased to approximately 80% of the critical current, which results in a minor voltage drop below the gap voltage. Finally, the output voltage resets back to low when the bias signal is low (i.e., the bias current is approximately zero and all JJs are reset to superconducting state).

In Josephson–CMOS memory applications, the Suzuki stack circuit is usually connected to a CMOS amplifier through a resistor and an additional inductor, as shown in Fig. 2. Therefore, the capacitive load is considered throughout this article.

B. Possible Limitations

As previously mentioned, the JJs in Suzuki stack are typically biased to around 70–80% of the critical current after the input signal arrives, which is sufficient to keep the JJs in the resistive state and to maintain a high output voltage. This configuration is common in existing Suzuki stack designs [22], [29]–[31]. However, if one carefully examines the *I–V* characteristic of a JJ with the critical current of 400 μA, as shown in Fig. 1, the JJs can be biased with a lower current, e.g., 50% where the voltage is equal to around 95% of the gap voltage. Therefore, there exists a tradeoff between the output voltage and bias current. A lower bias current would result in lower power dissipation because most of the power is dissipated across the bias resistor R_b that is typically quite large (in our case, 750 Ω). Additionally, one may notice that the critical current values of JJs located in the left and right branches are equal to each other (i.e., $I_{c,l} = I_{c,r} = 400\ \mu$A). Ortlepp *et al.* [22] use equal critical current values in the branches. However, there is no study that investigates any potential advantage of using nonequal critical current values [22]. In Section IV, the idea of using lower bias current and nonequal $I_{c,l}$ and $I_{c,r}$ is explored to reduce power dissipation of Suzuki stack circuits.

IV. PROPOSED OPTIMIZATION TECHNIQUE

In this section, an optimization technique is proposed to reduce the power dissipation of the Suzuki stack circuit. Additionally, the impacts of process variations are considered during the design and verified with the margin analysis.

A. Assumptions

The minimum margin values are assumed to be limited to ±20%. This means that the Suzuki stack circuit should operate correctly when the parameters such as bias current (I_b), critical current values of JJs ($I_{c,l}$, and $I_{c,r}$) are varied by lower than or equal to ±20%. This value can be modified depending on the available fabrication technology.

B. Proposed Conditions

Condition #1: Before the input signal arrives, the current flowing through the left branch (i.e., I_l) should be less than the critical current of JJs located in the left branch (i.e., $I_{c,l}$), which is shown in (1). Since $I_{c,l}$ is larger than I_l, in the worst

case scenario, -20% variation of $I_{c,l}$ should be considered. Therefore, the factor of 0.8 is added to $I_{c,l}$ in (1). This condition ensures that the JJs located in the left branch will not be switched into the resistive state before the arrival of input signal

$$I_l \leq 0.8 \times I_{c,l}. \tag{1}$$

Condition #2: When the input signal arrives, the sum of I_{in} and I_l should be larger than the critical current of the lowermost JJ located in the left branch, which is shown in (2). In the worst case scenario, $I_{c,l}$ could vary by $+20\%$ (i.e., factor of 1.2). This condition ensures that the lowermost JJ in the left branch will be switched into the resistive state upon the arrival of the input signal

$$1.2 \times I_{c,l} \leq I_{\text{in}} + I_l. \tag{2}$$

To represent the maximum margins of $\pm 20\%$ $I_{c,l}$, the inequality signs in (1) and (2) are changed to equality signs. By solving the set of two linear equations, it can be found that $I_{c,l} = 350$ μA and $I_l = 280$ μA.

Condition #3: When the lowermost JJ located in the left branch is switched into the resistive state, the bias current (i.e., I_b) starts to flow through the right branch. Therefore, I_b should be larger than the critical current in the right branch (i.e., $I_{c,r}$), which is shown in (3). Since I_b is larger than $I_{c,r}$, in the worst case scenario, -20% variation of I_b should be considered. This condition ensures that the right branch will switch into the resistive state

$$0.8 \times I_b \geq I_{c,r}. \tag{3}$$

Equation (3) is the main condition that results in a reduction of the power dissipation. In the design proposed in [22] (hereinafter referred to as the *original* design), both left and right branches are biased to around 80% of the critical current (i.e., $I_l \approx 0.8 \times I_{c,l} \approx I_r \approx 0.8 \times I_{c,r}$). By applying Kirchhoff's current law

$$I_b \approx I_l + I_r \rightarrow I_b \approx 0.8 \times 2 \times I_{c,r} = 1.6 \times I_{c,r}. \tag{4}$$

By comparing (3) and (4), one can deduce that the condition #3 results in much lower bias current.

C. Analysis of Various Circuit Parameter Configurations

To determine the values of the remaining parameters, the relation between I_b and I_l needs to be analyzed. The circuit parameter values for $I_l/I_b = 0.50$ to 0.80, with the step size of 0.05 are tabulated in Table I. For $I_l/I_b = a$, the circuit parameters are determined as follows:

$$\begin{aligned} V_b &= I_b R_b = I_l R_b / a \\ I_{c,r} &= 0.8 \times I_b = 0.8 \times I_l / a \\ R_l &= \frac{I_r}{I_b} \times R_{\text{tot}} = (1-a) R_{\text{tot}} \\ R_r &= R_{\text{tot}} - R_l = a R_{\text{tot}} \end{aligned} \tag{5}$$

where R_{tot} is the total branch resistance. For the sake of a fair comparison of power dissipation and area, R_{tot} is set to 8.0 Ω (see Table I). The remaining circuit parameters have the same values as in the original design.

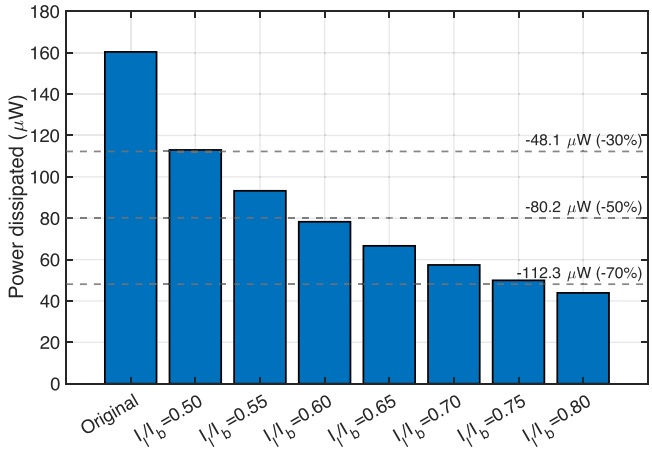

Fig. 4. Comparison of the power dissipation for various designs of the Suzuki stack circuit. Dashed lines show the relative change with respect to the original design (i.e., first column). The switching activity factor is set to 0.5.

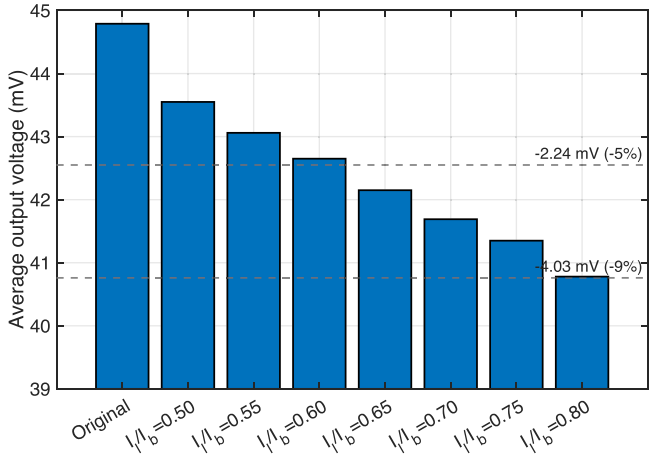

Fig. 5. Comparison of the average output voltage for various designs of the Suzuki stack circuit. Dashed lines show the relative change with respect to the original design (i.e., first column).

The design configurations of the Suzuki stack circuit listed in Table I are simulated and compared, as shown in Figs. 4–6. The following is a list of main observations with corresponding explanations.

1) Power Dissipation: A greater I_l/I_b ratio corresponds to the larger reduction in power dissipation, as shown in Fig. 4. This behavior can be explained by the fact that the bias current is reduced with a fixed I_l value. For example, for $I_l/I_b = 0.60$, the power dissipation is decreased by 51.2% (-82.1 μW) as compared to the original design. In this case, the bias current is reduced from 667 μA to 467 μA. As a result, the power dissipation across the bias resistance R_b, which is equal to 750 Ω, is reduced by 51.0%.

2) Output Voltage: When the I_l/I_b ratio is increased, the JJs are biased with a lower bias current, making the voltage drop across each JJ lower (see Fig. 1). As a result, the average output voltage (when the input signal is applied) is decreased with a larger I_l/I_b ratio (see Fig. 5). Considering the same condition ($I_l/I_b = 0.60$), the average output voltage is decreased by

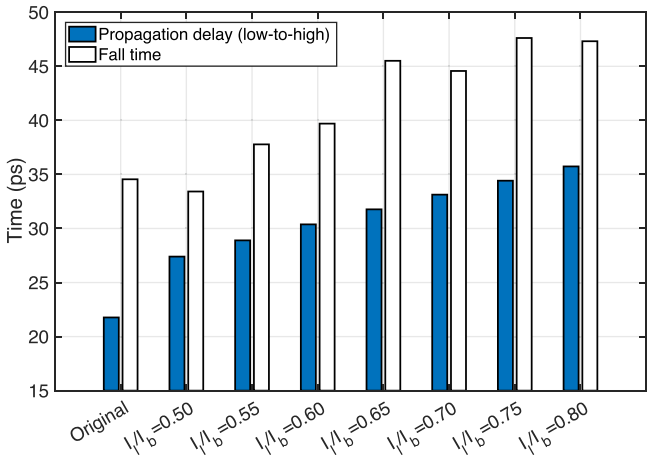

Fig. 6. Comparison of the propagation delay (low-to-high) and fall time (from 90% to 10%) of the output voltage for various designs of the Suzuki stack circuit.

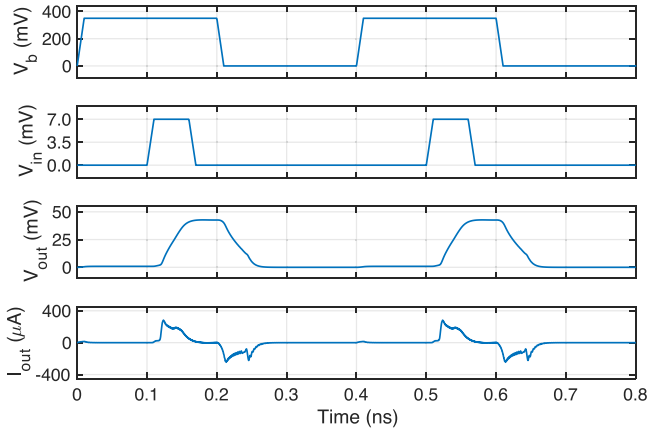

Fig. 7. Operation of the Suzuki stack circuit optimized for lower power dissipation ($I_l/I_b = 0.60$).

4.78% (−2.14 mV) as compared to the original design. Once all JJs are switched into the resistive state, the distribution of current in left and right branches is no longer the same as before the arrival of input signal. In fact, these current values are oscillating such that the total current (i.e., $I_l + I_r$) is approximately equal to I_b. By measuring the average values of I_l and I_r after the input signal is arrived, it can be found that the JJs are biased to around 50%–60% for $I_l/I_b = 0.60$. For the critical current of 350–400 μA, the voltage across the JJ that is biased to 50% (80%) is approximately 95% (98%) of V_g (see Fig. 1). Therefore, for $I_l/I_b = 0.60$, the output voltage has a slightly larger voltage drop as compared to the original design.

3) Propagation Delay: A greater I_l/I_b ratio results in a larger propagation delay of the output voltage because the bias current is reduced, making the load capacitor charge slower (see Fig. 6). For $I_l/I_b = 0.60$, the propagation delay is increased by 39.5% (+8.61 ps) as compared to the original design. By comparing Figs. 3 and 7, one can see that the transient (peak) output current is slightly smaller than that of the original design. This is the main reason for the increase in the propagation delay.

4) Fall Time: Although the effective resistance remains approximately the same across all of the designs listed in Table I,

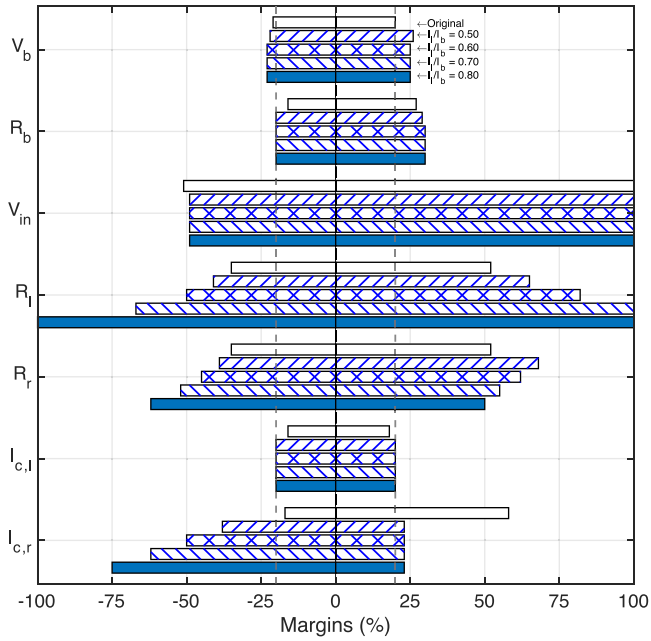

Fig. 8. Design margins of the original and proposed Suzuki stack circuits with lower power dissipation ($I_l/I_b = 0.50, 0.60, 0.70, 0.80$). Two vertical dashed lines show ±20% boundaries.

the fall time of the Suzuki stack circuit does not linearly depend on *RC* time constant. This is because the JJs are not transitioning from resistive to superconducting states at the same time instance. A comparison of the fall time values for each Suzuki stack circuit design is shown in Fig. 6. From this figure, one can notice that the fall time does not linearly depend on the bias current. Nevertheless, the proposed designs with lower power dissipation (i.e., $I_l/I_b = 0.55$ to 0.80) have generally slightly larger fall time values than that of the original design. For example, for $I_l/I_b = 0.60$, the fall time is 14.9% (+5.15 ps) larger as compared to the original design.

As explained above, there exists a tradeoff between the power dissipation, average output voltage, and propagation delay and fall time of the output voltage. The proposed optimization technique can be utilized to determine the circuit parameters depending on the specified constraints on the power consumption and output voltage characteristics.

D. Margins

The simulated margins for the original and proposed designs are shown in Fig. 8. The margins of the designs with lower power dissipation ($I_l/I_b = 0.50$ to 0.80) are not degraded as compared to the original design. Furthermore, all of the parameters are within ±20% variation range, satisfying the initial assumption.

In Fig. 8, for the proposed designs with lower power dissipation, the bias margins stay approximately the same because V_b and R_b have a near linear effect on I_l (as well as I_b and I_r), which is restricted by (1) and (2). Additionally, these equations limit the margins of $I_{c,l}$ to exactly ±20%. Since the proposed designs have the same I_l and $I_{c,l}$ values that are determined in Section IV-B, the margins of V_{in} are identical. Similarly, the upper margins of $I_{c,r}$ are the same due to the condition

(3). Therefore, it is verified that the bias and critical current margins can be controlled within the specified limits by using the proposed conditions in Section IV-B.

E. Discussion

It should be noted that the proposed designs have a slightly lower total area of JJs because the critical current of JJs is smaller than that of the original design. Accordingly, as compared to the original design, the total area of JJs is reduced by 9.63% for $I_l/I_b = 0.60$. By utilizing the available space, a possible improvement for this design can be the addition of one more JJ in each branch. This modification can possibly compensate for the voltage drop of -2.14 mV by adding approximately 2.8 mV (one gap voltage) to the output voltage. By simulating the Suzuki stack circuit with 17 JJs connected in series with $I_l/I_b = 0.60$ parameter configuration, the output voltage of 45.1 mV, power dissipation of 78.2 μW, propagation delay of 31.6 ps, and the fall time of 41.5 ps are achieved. As compared to the original design with 16 JJs, the output voltage and total area of JJs are approximately the same while the power dissipation is reduced by 51.2% (-82.2 μW). It should be noted that the proposed power optimization technique does not account for the number of JJs in each branch because this parameter does not have a significant impact on the power dissipation of the Suzuki stack circuit. A greater number of JJs in the stack results in less reliable performance (i.e., lower margins). Nevertheless, for the Suzuki stack circuit with 17 JJs ($I_l/I_b = 0.60$), the margins are within at least $\pm 20\%$.

V. Conclusion

In this article, an optimization technique that reduces the power dissipation of the Suzuki stack circuit is proposed. By analyzing the operation principle of the Suzuki stack circuit and existing designs, possible strategies to improve the power dissipation are suggested. The proposed optimization technique defines a set of operating conditions to ensure that the circuit continues to operate correctly under given process parameter variations. Various circuit parameter configurations are estimated and compared in terms of power dissipation, average output voltage, propagation delay, and fall time of the output voltage. The corresponding tradeoffs are discussed and explained. The proposed designs have 3070% lower power dissipation as compared to the existing circuit while reducing the output voltage by 2–9% depending on the circuit parameter configuration.

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