Suzuki Stack Circuit With Differential Output

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***Abstract*—Suzuki stack circuits, a type of latching high-voltage driver circuit, are widely used in Josephson–CMOS hybrid memories. The existing Suzuki stack designs utilize only single-ended signaling when connected to a CMOS amplifier. In this article, a Suzuki stack circuit with a differential output is proposed by producing both the positive and negative output voltages. The negative output voltage is produced by using a negative biasing network and a negative single-flux quantum (SFQ) input pulse, which is generated by the proposed positive-to-negative SFQ converter. As compared to a conventional single-ended Suzuki stack circuit, the proposed differential design can provide two times higher output voltage swing and better immunity to noise without degrading the operating margins. Potential advantages and drawbacks of the proposed circuit are explored in this article.**

***Index Terms*—Differential signaling, differential output, Josephson latching driver, Josephson–CMOS memory, negative output voltage, superconductor–semiconductor interface circuit, Suzuki stack circuit.**

I. Introduction

SUZUKI stack circuit (a.k.a. Josephson latching driver) is a latching high-voltage driver circuit, originally proposed in 1988 by Suzuki et al. [1]. This circuit consists of two arrays of serially connected underdamped Josephson junctions (JJs) and can convert a single-flux quantum (SFQ) pulse to a dc voltage signal in the order of tens of millivolts. The comparably higher output voltage is the primary advantage of a Suzuki stack circuit over other interface circuits, such as superconducting quantum interference device (SQUID) stack [2], [3] and SFQ-to-dc converter [4], [5]. In addition, a Suzuki stack circuit occupies lower area (few JJs) and operates faster than a SQUID stack. It should be noted that the Suzuki stack circuit requires an ac-type power supply, whereas the SQUID stack is asynchronous and dc-powered. Therefore, the biasing network of Suzuki stack circuits is more complex as compared to the SQUID stack.

Suzuki stack circuits are commonly used in Josephson–CMOS hybrid memories [6], [7], [8]. This hybrid memory exploits high frequency (tens to hundreds of gigahertz) and low power consumption (zepto J) of SFQ circuits [4], [9], [10], [11] and large-scale integration densities of CMOS technology [12], [13].

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To amplify the output voltage of a Suzuki stack circuit to a voltage level appropriate for CMOS operation, a CMOS amplifier is typically used. A higher output voltage of a Suzuki stack circuit is desired to reduce the power consumption of the CMOS amplifier. However, as the output voltage of a Suzuki stack circuit is increased (i.e., a higher number of JJs are stacked in series), the circuit operation becomes less stable [14].

In state-of-the-art Josephson–CMOS hybrid memories, the Suzuki stack circuit is connected to only one input terminal of the CMOS amplifier, while the other input terminal is connected to either the reference voltage [7] or ground [6]. In high-speed digital link applications, differential signaling is implemented by utilizing a differential SFQ-to-dc converter and differential SQUID stack circuits [15], [16], [17], [18], [19]. The differential signaling provides higher output voltage swing and better noise immunity due to the common-mode rejection property of CMOS differential amplifiers. This article focuses on designing the Suzuki stack circuit with differential output (i.e., two outputs are connected to separate inputs of CMOS differential amplifier).

The following are the key contributions of this article.

1) A Suzuki stack circuit with differential output is proposed for the first time.
2) Two new circuits, such as Suzuki stack circuit with negative output voltage and positive-to-negative SFQ converter, are proposed. These circuits are used as the building blocks of the differential Suzuki stack circuit.
3) The operating margins of the proposed circuit are analyzed.
4) Potential advantages and disadvantages of a differential Suzuki stack circuit are discussed and compared to a single-ended (conventional) design. Particularly, important design parameters, such as noise, stability, power dissipation, fall time, propagation delay, maximum frequency, design extension, area, and biasing network, are considered.

The rest of this article is organized as follows. The operation principle of a conventional Suzuki stack circuit is discussed in Section II. The proposed differential Suzuki stack circuit is presented in Section III. The proposed differential Suzuki stack circuit is compared to a single-ended (conventional) design in Section IV. Finally, Section V concludes this article.

II. Working Principle of Suzuki Stack Circuits

A basic schematic of a Suzuki stack circuit with a four-junction logic (4JL) gate [20] is depicted in Fig. 1. A 4JL gate is placed between the SFQ input and Suzuki stack circuits and used as a preamplifier for input and output stability [6]. The circuit

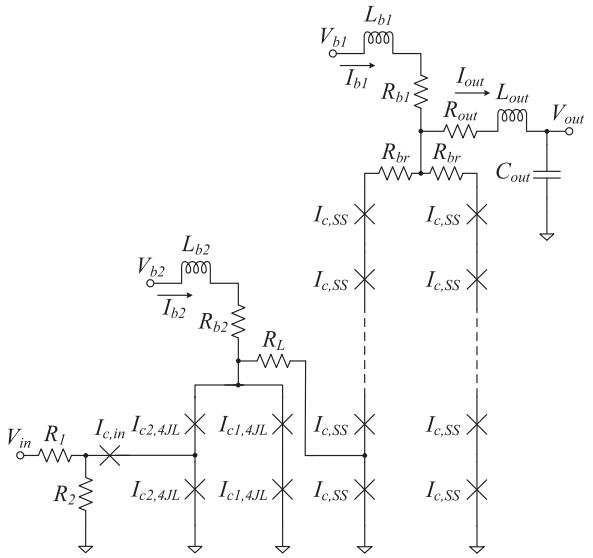

Fig. 1. Schematic of the Suzuki stack circuit with a 4JL gate. The SFQ input pulse is received at V_{in} terminal. V_{b1} and V_{b2} are square-wave ac voltage sources.

TABLE I
PARAMETERS OF THE PROPOSED DIFFERENTIAL SUZUKI STACK CIRCUIT

Circuit	Parameter	Value
Suzuki stack	Bias voltage V_{b1}	500 mV
	Bias resistance R_{b1} *	750 Ω
	Bias inductance L_{b1}	200 pH
	Branch resistance R_{br}	4 Ω
	Critical current $I_{c,\text{SS}}$ **	400 μA
	Output resistance R_{out}	50 Ω
	Output inductance L_{out}	100 pH
	Output capacitance C_{out} ***	180 fF
4JL gate	Bias voltage V_{b2}	61 mV
	Bias resistance R_{b2}	200 Ω
	Bias inductance L_{b2}	200 pH
	Critical current $I_{c1,\text{4JL}}$, $I_{c2,\text{4JL}}$ **	300, 100 μA
	Load resistance R_L	10 Ω
	Critical current $I_{c,\text{in}}$	190 μA
	Resistance R_1, R_2	1, 2 Ω
Positive-to-negative SFQ converter	Bias current I_{b3}, I_{b4}	350, −315 μA
	Critical current $I_{c1,\text{JTL}}$, $I_{c2,\text{JTL}}$	250, 130 μA
	Inductance L_{JTL}	2 pH
	Resistance R_{JTL}	1 Ω
	Coupled inductances L_1, L_2	8, 8 pH
	Coupling coefficient K	1

* The bias resistor R_{b1} is optimized for a 16-channel interface circuit (i.e., 16 Suzuki stack circuits connected in parallel) similar to the circuit proposed in [14].
** In Suzuki stack and 4JL gate circuits, the JJs located in stacks are shunted with resistance $R_{\text{sh}} = 6V_g/I_c$ [14], where V_g is the gap voltage and I_c is the critical current of JJ.
*** Capacitive load is considered to model the subsequent CMOS amplifier stage.

parameters are partially selected from [6], [14], [20], and [21] and listed in Table I.

The simulation results of a Suzuki stack circuit with the 4JL gate are shown in Fig. 2(a). The circuit is simulated by using the Verilog-A RCSJ model of JJ in the MIT Lincoln Lab 10-kA/cm^2 process, which is available as an open-source file in [22]. This RCSJ model of JJ is commonly used in the simulation of superconducting electronics (particularly, SFQ circuits) [23]. In this article, Cadence Spectre is used as the simulation environment, which is a SPICE-class circuit simulator (similar to WRspice and JSIM [23]) and has a native support of Verilog-A modules. The same simulation setup has been utilized in our previous work on the power optimization of Suzuki stack circuits [24]. When an SFQ pulse is applied to V_{in} (see Fig. 1 for notation), the lowermost JJ in the left branch of the 4JL gate switches from superconducting to the resistive state. Owing to the asymmetry in the left and right branches, most of the bias current (I_{b2}) starts to flow through the right branch, switching the right JJs to the resistive state with the critical current of $I_{c1,\text{4JL}}$. After that, a portion of the bias current flows back into the left branch, switching the top-left JJ to the resistive state with $I_{c2,\text{4JL}}$. Since both the left and right branches of the 4JL gate are no longer superconducting, the current starts to flow through the resistor R_L. The JJs in the Suzuki stack circuit switch from superconducting to the resistive state in a similar way as in the 4JL gate. As a result, the output voltage $V_{\text{out}} \approx mV_g$ is produced, where m is the number of JJs connected in series in one branch of the Suzuki stack circuit (i.e., there are $2m$ JJs in total) and V_g is the gap voltage of JJ. For example, for $m = 16$ and $V_g = 2.8$ mV, the output voltage is around 44.8 mV [see Fig. 2(a)]. Owing to the underdamped behavior of JJs (i.e., Stewart–McCumber parameter $\beta_c \gg 1$) used in Suzuki stack circuits, the output voltage remains high as long as the bias voltage V_{b1} is high. When no SFQ input is applied as shown in Fig. 2(a), the output voltage remains low. In this case, all the JJs are in the superconducting state. The output voltage is not exactly equal to zero because of a minor voltage drop across the branch resistors R_{br}, which is around 1.3 mV ($I_{b1}R_{\text{br}}/2$) when V_{b1} is high.

In Fig. 2(a), the Suzuki stack circuit is simulated at 2.5 GHz. The maximum operating frequency depends on the timing constraints of the SFQ input pulse. In the best case scenario when the SFQ input pulse arrives at the beginning of each clock cycle, the simulated maximum frequency is 5.71 GHz. In a more realistic setup, there could be some delay in the arrival of the input signal making the maximum frequency lower. For example, the Suzuki stack circuit with similar parameters has been fabricated and tested in [14] with the frequency of 4 GHz.

III. PROPOSED DIFFERENTIAL INTERFACE CIRCUIT DESIGN

In this section, a differential Suzuki stack circuit design is proposed. The output signaling is implemented similar to a differential SFQ-to-dc converter, which has been presented in [15]. Particularly, when an SFQ input is applied, the first and second output terminals produce positive and negative output voltages, respectively. When no input is applied, both the outputs are set to zero.

To design a Suzuki stack circuit with a negative output voltage, the symmetrical property of a JJ is utilized. By using the same circuit schematic and parameters (see Fig. 1 and Table I) and reversing the polarity of bias and input signals (i.e., V_{b1}, V_{b2}, and V_{in}), a negative output voltage can be produced.

The simulation results of a modified Suzuki stack circuit are shown in Fig. 2(b), which is almost identical to Fig. 2(a) with voltage and current waveforms that have the opposite polarity. Therefore, an output voltage of −44.8 mV is produced. It is expected that the operating margins should be similar to a conventional Suzuki stack circuit (i.e., with positive output voltage).

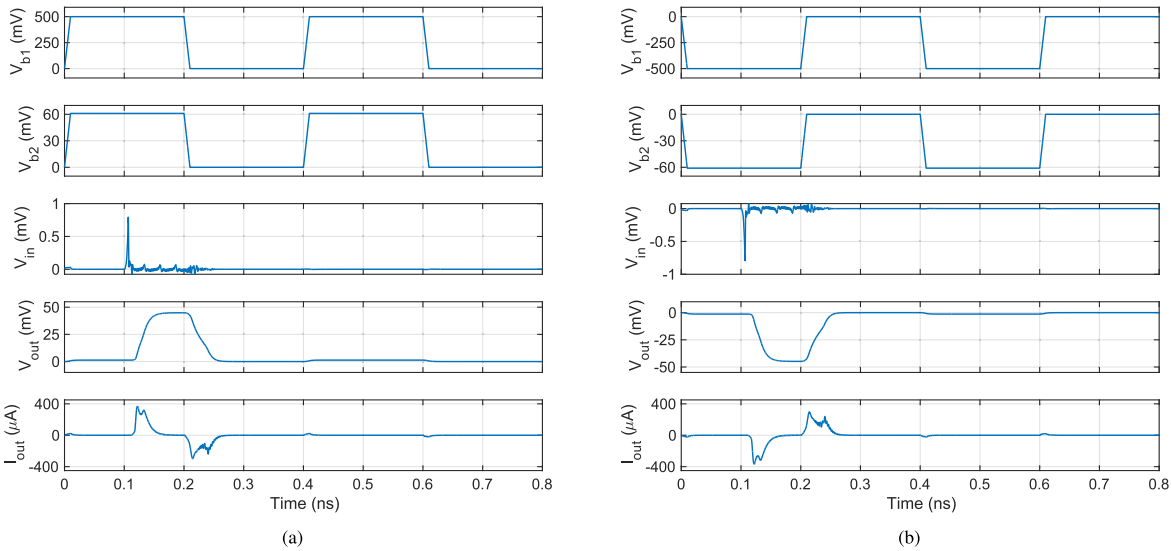

Fig. 2. Simulation of (a) the conventional (single-ended) Suzuki stack circuit and (b) the proposed Suzuki stack circuit with negative output voltage. In both the designs, there are 16 JJs connected in series, i.e., $m = 16$.

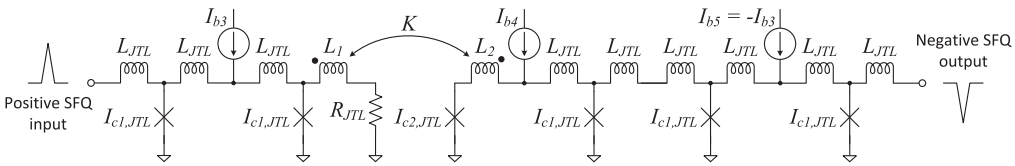

Fig. 3. Schematic of the positive-to-negative SFQ converter followed by the negatively biased JTL cell. Inductors L_1 and L_2 are mutually coupled with a coupling coefficient K.

One may notice that V_{in} waveform in Fig. 2(b) has a negative SFQ pulse. Negative SFQ pulses are common in superconducting electronics, such as reciprocal quantum logic [25], digital SQUID sensor [26], and bipolar SFQ transmitter [27]. In these circuits, both the positive and negative SFQ pulses are applied along the same signal line.

To realize a Suzuki stack circuit with a negative output voltage, one needs to convert a positive SFQ pulse to a negative SFQ pulse. To the best of the authors' knowledge, there is no such converter available in the literature. In this article, a positive-to-negative SFQ converter is proposed. The schematic of this circuit is depicted in Fig. 3. The circuit parameters are partially based on RSFQ Josephson transmission line (JTL) from [28] and listed in Table I.

The concept of mutual inductance is used in, e.g., superconducting lookup tables [29], SQUID transformers [30], and SFQ logic locking [31], [32]. To implement the SFQ conversion, two JTL cells are mutually coupled with inductances L_1 and L_2 (see Fig. 3). The simulation results of the positive-to-negative SFQ converter are shown in Fig. 4. Initially, a JJ with a critical current $I_{c2,\text{JTL}}$ (see notation in Fig. 3) is negatively biased to around -78.5 μA. When the positive SFQ pulse reaches L_1, the current through this inductance (I_{L1}) starts increasing (see Fig. 4). Because of the mutual inductance, I_{L2} becomes lower than $I_{c2,\text{JTL}}$, and the corresponding JJ switches from superconducting to the resistive state producing a negative SFQ pulse. To guarantee the stability of this pulse, an additional negatively biased JTL cell is connected, as shown in Fig. 3 (this JTL cell is also shown in Fig. 5 in a dashed box). The propagation delay of the positive-to-negative SFQ converter with one negatively biased JTL cell is simulated to be approximately 14.4 ps.

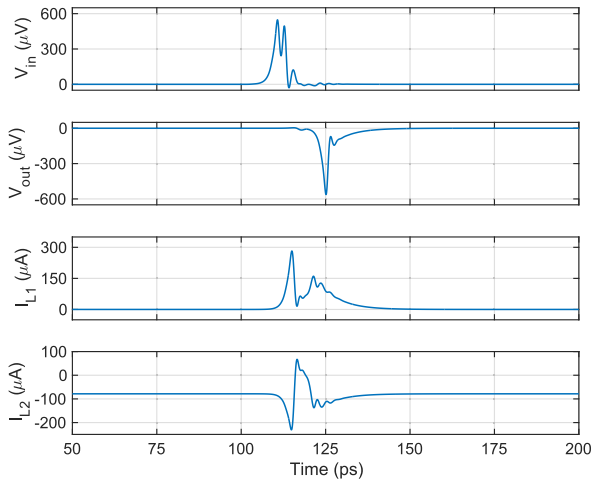

Fig. 4. Simulation of the positive-to-negative SFQ converter that is connected to the negatively biased JTL cell. I_{L1} and I_{L2} correspond to current waveforms of the inductors L_1 and L_2 in Fig. 3, respectively.

The design of the differential Suzuki stack circuit is shown in Fig. 5. Note that the SFQ splitter and JTL designs are taken from the RSFQ cell library [28].

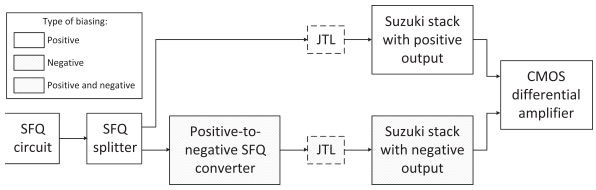

Fig. 5. Block diagram of the proposed differential Suzuki stack circuit. Dashed line shows an optional JTL stage. The Suzuki stack block includes the 4JL gate. The type of biasing is indicated for each block according to the inset figure.

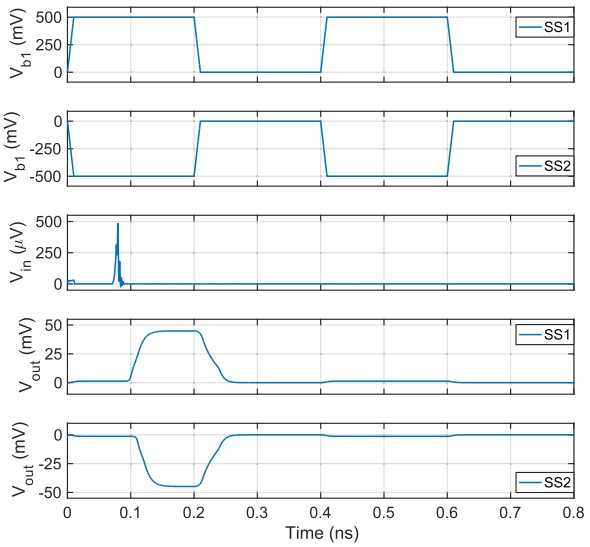

Fig. 6. Simulation of the proposed differential Suzuki stack circuit. Legends "SS1" and "SS2" refer to the waveforms of Suzuki stack circuits with positive and negative outputs, respectively. The differential output voltage ΔV_{out} (i.e., the input voltage swing of subsequent CMOS amplifier stage) is equal to the difference between $V_{\text{out,SS1}}$ and $V_{\text{out,SS2}}$.

When the input SFQ pulse is applied as shown in Fig. 6, the differential output is

$$\Delta V_{\text{out}} = V_{\text{out,SS1}} - V_{\text{out,SS2}} = 89.6\ \text{mV} \tag{1}$$

where $V_{\text{out,SS1}}$ and $V_{\text{out,SS2}}$ are the output voltages of Suzuki stack circuits with positive and negative outputs, respectively. The output voltage swing is, therefore, doubled as compared to the conventional (single-ended) Suzuki stack circuit that is discussed in Section II.

The simulated margins of the proposed differential Suzuki stack circuit are shown in Fig. 7. The Suzuki stack circuits with positive and negative outputs have exactly the same circuit parameters (see Table I). In addition, these circuits receive SFQ pulse with almost identical amplitude and shape (in absolute value) because of the preceding JTL cell (see Fig. 5). Therefore, the margins for Suzuki stack (i.e., V_{b1}, R_{b1}, and $I_{c,\text{SS}}$) and 4JL gate (i.e., V_{b2}, R_{b2}, $I_{c1,\text{4JL}}$, and $I_{c2,\text{4JL}}$) are identical for both the positively and negatively biased circuits (see Fig. 7).

The proposed differential Suzuki stack circuit design has a skew between positive and negative output voltage signals, as can be observed in Fig. 6. This timing skew is caused by the positive-to-negative SFQ converter that is added in one of the paths (see Fig. 5). If the CMOS differential amplifier circuit requires certain timing constraint on the arrival time of input signals, one may use extra JTL stages as a delay element and

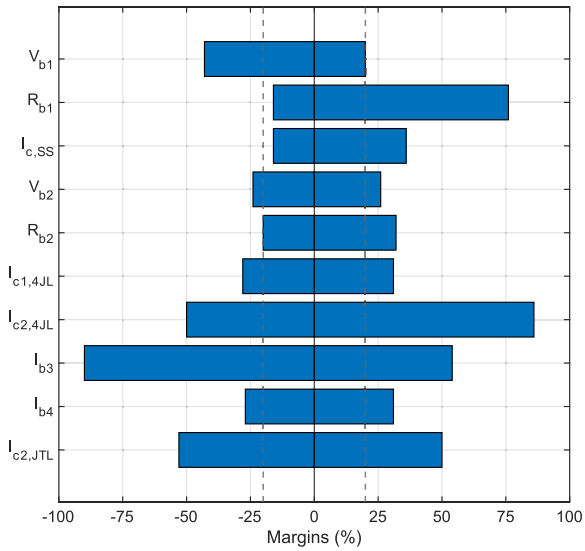

Fig. 7. Simulated operating margins of the proposed differential Suzuki stack circuit. Two vertical dashed lines show $\pm 20\%$ boundaries. The frequency is set to 2.5 GHz, and the circuit parameters are the same as in Table I.

place them at the input of the Suzuki stack circuit with positive output.

Furthermore, the proposed positive-to-negative SFQ converter exhibits wide margins (see I_{b3}, I_{b4}, and $I_{c2,\text{JTL}}$ in Fig. 7). The proposed differential Suzuki stack operates correctly with the coupling coefficient K from 0.7 to 1. Since SFQ splitter and JTL cell designs are unchanged, their operating margins are the same as in the RSFQ cell library [28].

IV. Comparison of Single-Ended and Differential Suzuki Stack Circuits

In this section, the proposed differential Suzuki stack circuit is compared to a single-ended (conventional) design. For a fair comparison, the same output voltage swing (i.e., ΔV_{out}) is considered. This means that the single-ended design should consist of $16 \times 2 = 32$ JJs connected in series and produce the output voltage of around 89.6 mV. The advantages and disadvantages of the differential Suzuki stack circuit are discussed in Sections IV-A and IV-B, respectively.

A. Advantages

1) Noise: The signal quality is improved because of the common-mode rejection property that is inherent in differential signaling [15]. The reduction of noise is an important aspect in high-speed digital link designs [16], [17], [18], [19].

2) Stability: The differential Suzuki stack circuit consists of 16 JJs connected in series in each branch, whereas the single-ended design has two times more number of JJs (i.e., 32 JJs in series). Stacking more number of JJs in series degrades the stability of the Suzuki stack circuit due to the process variations [14]. In addition, the bias margins are decreased with a greater number of JJs in series (see [14, Fig. 16], where the Suzuki stack circuits with 8, 16, 24, and 32 JJs are compared). The differential design, therefore, has better stability as compared with that of a single-ended design.

TABLE II
COMPARISON OF SINGLE-ENDED AND DIFFERENTIAL SUZUKI STACK DESIGNS

Parameter	Single-ended	Differential
Average output voltage	88.1 mV	89.6 mV
Power dissipation *	320.4 μW	319.9 μW
Fall time (90% to 10%)	68.5 ps	35.1 ps
Propagation delay	40.1 ps **	38.4 ps ***
Maximum frequency	3.91 GHz	4.67 GHz

* The switching activity factor of 0.5 is assumed. Includes only the power dissipation of the Suzuki stack circuit.
** Includes the JTL cell and the 4JL gate.
*** Includes SFQ splitter, positive-to-negative SFQ converter, JTL cells, and 4JL gate.

3) Power Dissipation: The bias current variation of a Suzuki stack circuit can be expressed as

$$\Delta I_{b1} = I_{b1}\{\text{in} = 0\} - I_{b1}\{\text{in} = 1\} \approx \frac{V_{\text{out}}}{R_b} \tag{2}$$

where $I_{b1}\{\text{in} = 0\}$ and $I_{b1}\{\text{in} = 1\}$ are the bias current values when the input is logic "0" and "1," respectively. Assuming equal ΔI_{b1} and I_{b1} for both the designs, the single-ended design should have $R_{b1} = 750 \times 2 = 1500\ \Omega$ and $V_{b1} = 0.5 \times 2 = 1$ V. Since most of the power is dissipated on the bias resistor R_{b1} [24], the power dissipation is approximately the same for both the designs. Particularly, the simulated power dissipation of differential design is within 0.16% of the single-ended design (see Table II). In addition, the power dissipation of CMOS amplifiers should be approximately the same because of similar output voltage swing of differential and single-ended Suzuki stack circuits (i.e., input voltage swing of the CMOS amplifier), which is initially assumed in Section IV.

4) Fall Time: The fall time of differential output voltage (ΔV_{out}) refers to a time taken for the amplitude of ΔV_{out} to decrease from 90% to 10% of the peak value. A shorter fall time allows the circuit to operate at a higher frequency making it an important design parameter. For the differential Suzuki stack design, the simulated fall time of ΔV_{out} is 35.1 ps, which is 1.95 times lower than that of a single-ended design (see Table II). Such behavior is caused by the smaller number of JJs connected in series in the differential Suzuki stack circuit. With smaller number of JJs connected in series (i.e., lower total parasitic capacitance), less time is required for the JJs to switch from the resistive state to the superconducting state [33].

5) Propagation Delay: One may argue that the additional stages of the SFQ splitter and the positive-to-negative SFQ converter in the differential Suzuki stack circuit could increase the overall propagation delay. However, in our case study, the overall propagation delay of the differential design is 4.24% lower than that of the single-ended design (see Table II). Similar to the fall time behavior, the smaller number of JJs in series (i.e., lower total parasitic series inductance) results in faster switching from the superconducting state to the resistive state [33]. Therefore, the lower switching time of differential Suzuki stack circuit compensates the additional propagation delay of the SFQ splitter and the positive-to-negative SFQ converter.

6) Maximum Frequency: In Fig. 6, the proposed differential Suzuki stack circuit is simulated at 2.5 GHz. The maximum operating frequency is 4.67 GHz, assuming that the SFQ input pulse arrives at the beginning of each clock cycle (i.e., best case scenario). The maximum frequency of the differential Suzuki stack circuit is 19.4% higher as compared to that of the single-ended design (see Table II). Such behavior is mainly caused by the difference in fall time values of output voltage that are listed in Table II.

7) Design Extension: Since a Suzuki stack circuit with positive and negative outputs has the same circuit parameters and margins, the existing designs of single-ended Suzuki stack circuits can be easily converted to produce the differential output. In addition, the circuit layout of a Suzuki stack circuit with negative output can have the same layout as the conventional one. Such a configuration is possible because in a Suzuki stack circuit with negative output, the current flowing through all the sections has the same magnitude in the absolute value and the opposite direction of current flow. Therefore, the output voltage swing can be doubled without degrading the performance and saving on R&D cost. Alternatively, the existing single-ended designs can be replaced with the differential design that has the same output voltage swing. Such a configuration could allow higher operating frequency because of the lower fall time (see Sections IV-A4 and IV-A6).

B. Disadvantages

1) Area: The total area of bias resistors (assuming that the resistance value is determined by changing only the length with a constant width similar to the Suzuki stack layout in [14, Fig. 17(a)], e.g., the area of a 750-Ω resistor is two times smaller than a 1500-Ω resistor) and JJs should be approximately similar in both the designs. Nevertheless, the differential Suzuki stack circuit consists of an additional SFQ splitter and the positive-to-negative SFQ converter, which makes its design slightly larger in area.

The differential Suzuki stack circuit requires an additional wire to the CMOS amplifier as compared to the conventional design. The 64-kB Josephson–CMOS hybrid memory [7] consists of 30 (single-ended) Suzuki stack circuits each connected to the CMOS comparator. The proposed differential Suzuki stack circuits would require additional 30 wires to be connected to CMOS circuits. In addition, if the CMOS differential amplifier is located at a higher temperature stage of the cryostat, the differential design will require an additional interconnect (cable) between temperature zones for the Suzuki stack with negative output (see Fig. 5).

2) Biasing Network: The proposed interface circuit requires both the positive and negative types of biasing networks, as shown in Fig. 5. Alternatively, a single-ended Suzuki stack circuit has only the positive biasing network, which makes the design less complex. Note that both the positive and negative biasing networks are commonly used in differential SFQ-to-dc converters and differential SQUID stack circuits [15].

V. CONCLUSION

In this article, a Suzuki stack circuit with a differential output is proposed. By designing the Suzuki stack circuit with the negative output voltage and the positive-to-negative SFQ converter, the output voltage swing can be doubled as compared to the

conventional (single-ended) designs without degrading the operating margins and having better immunity to noise. Alternatively, the proposed differential Suzuki stack circuit is compared to the single-ended design for the same output voltage swing. In the case of the same output voltage swing, the differential design can provide better immunity to noise and stability, approximately the same power dissipation (within 0.16%), and 19.4% higher operating frequency as compared to the single-ended Suzuki stack circuit. The drawbacks of the differential Suzuki stack circuit are slightly larger area, additional wiring to CMOS circuits, and more complex biasing network that needs both the positive and negative bias voltage sources.

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