Study of Vertical Ga_2O_3 FinFET Short Circuit Ruggedness using Robust TCAD Simulation

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Abstract

In this paper, the short circuit ruggedness of Gallium Oxide (Ga_2O_3) vertical FinFET is studied using Technology Computer-Aided-Design (TCAD) simulations. Ga_2O_3 is an emerging ultra-wide bandgap material and Ga_2O_3 vertical FinFET can achieve the normally-off operation for high voltage applications. Ga_2O_3 has a relatively low thermal conductivity and, thus, it is critical to explore the design space of Ga_2O_3 vertical FinFETs to achieve an acceptable short-circuit capability for power applications. In this study, appropriate TCAD models and parameters calibrated to experimental data are used. For the first time, the breakdown voltage simulation accuracy of Ga_2O_3 vertical FinFETs is studied systematically. It is found that a background carrier generation rate between 10^5 $cm^{-3}s^{-1}$ and 10^{12} $cm^{-3}s^{-1}$ is required in simulation to obtain correct results. The calibrated and robust setup is then used to study the short circuit withstand time (SCWT) of an 800 V-rated Ga_2O_3 vertical FinFET with different inter-fin architectures. It is found that, due to the high thermal resistance in Ga_2O_3, to achieve an SCWT > 1 μs, low gate overdrive is needed which increases $R_{on,sp}$ by 66% and that Ga_2O_3 might melt before the occurrence of thermal runaway. These results provide important guidance for developing rugged Ga_2O_3 power transistors.

1. Introduction

β-Gallium Oxide (β-Ga_2O_3) is a promising material to enable high breakdown and low loss power switching devices due to its ultra-wide bandgap (4.5 eV- 4.9 eV) and its ability to grow on a low-cost native substrate [1]-[4]. Since the Baliga figure of merit (BFOM) scales as the sixth power of the bandgap, its BFOM is expected to be almost 9 times that of GaN [1]. It also has well-controlled n-type doping in a wide range of 10^{15} cm^{-3} –10^{19} cm^{-3} [1][2]. However, it is difficult to form p-type doping in Ga_2O_3 [5] which poses limitations in the design of many power devices in Ga_2O_3.

To employ the Ga_2O_3 technology in power electronics systems, two fundamental devices, namely the diode and field-effect transistor (FET), must be realized. 1 kV vertical Ga_2O_3 field-plated Schottky barrier diode (SBD) has been achieved [6]-[8] and heterostructure p-n diodes were demonstrated [9][10]. SBDs have also been demonstrated to block high voltage at high temperatures up to 600 K [11]. The SBD development is expected to be successful with more sophistical edge termination techniques [2].

Due to the difficulty in p-type doping, depletion mode (threshold voltage, V_{th}, < 0 V) Ga_2O_3 FET is only possible if the traditional device architecture is used [12][13]. For fail-safe

operations, various schemes have been proposed to achieve enhancement mode devices (V_{th}, > 0 V) [14]-[20] and, among them, vertical Ga_2O_3 FinFET [19]-[22] is one of the most promising ones. Due to the work function difference between the gate metal and Ga_2O_3 channel, when the channel is narrow enough, vertical Ga_2O_3 FinFET becomes enhancement-mode even without p-type doping in the channel.

Since vertical Ga_2O_3 FinFET is still relatively immature, the experimental studies concentrate on $R_{on,sp}$, BV, $V_{th,}$ and trap densities. For example, in [19], an enhancement-mode vertical Ga_2O_3 FinFET has been achieved experimentally with V_{th} ~1.2-2.3V. In [20], the trap density at the interface was studied. Multi-fin enhancement mode Ga_2O_3 was then studied with improvement in sidewall trap density and high BV was achieved in [21]. To the best of our knowledge, since Ga_2O_3 is an emerging material, high-frequency studies and noise analysis such as in [23] for regular logic FinFET have not been performed experimentally.

Besides lacking p-type doping, another drawback of Ga_2O_3 in power application is that it has a relatively low thermal conductivity (k_T = 10–27 $Wm^{-1}K^{-1}$) compared to other materials, which poses an important engineering challenge [1][2]. Considerable works have studied the thermal performance of Ga_2O_3 devices [24][25]. Recently, a thermal resistance lower than the commercial SiC counterpart has been reported in packaged Ga_2O_3 SBDs [26].

The low k_T of Ga_2O_3 has also raised serious concerns about the electrothermal ruggedness of Ga_2O_3 devices. This ruggedness, e.g., short current or surge current, is essential for any power device in practical applications such as grids and automotive powertrains [27]. However, very few ruggedness studies have been reported for Ga_2O_3 devices, except for the surge current ruggedness of a Ga_2O_3 rectifier [28][30]. Despite a high surge current demonstrated in the packaged rectifier [28], the short-circuit capability of Ga_2O_3 transistors remains unknown due to the more complex device structures and higher electrothermal stress. The short-circuit condition involves abnormally high current at a blocking voltage close to the device rated voltage [29], while the surge-current condition is only at forward biases, rendering a much lower electric field stress.

For emerging materials and devices, Technology Computer-aided Design (TCAD) [31] is a very cost-effective tool to explore their design space and limitation in power circuit applications [9][10][17][32]-[37]. However, due to the ultra-wide bandgap and relative immaturity of Ga_2O_3, TCAD simulation of Ga_2O_3 devices is more difficult in terms of convergence, model formulation, and model selection. This is particularly true under extreme dynamic conditions, such as breakdown and short circuit ruggedness.

In this paper, the short circuit ruggedness of an 800 V-rated vertical Ga_2O_3 FinFET is studied using TCAD simulations with calibrated model parameters. Since the short-circuit simulation is performed at an 800 V bus voltage, the carrier dynamics at high voltage are vital. Thus, our simulation calibration relies on the breakdown voltage (BV) simulation. In addition to calibrating material parameters, the appropriate setup for BV extraction is derived to avoid numerical instabilities. The transistor is then designed using the BV obtained. Short circuit ruggedness through the extraction of short-circuit withstanding time (SCWT) is then simulated using mixed-mode simulation in TCAD for various device designs (e.g., inter-fin designs [38]) under the front-side junction cooling schemes.

2. Simulation Setup

2.1 Methodology

Ga_2O_3 is an emerging material. It does not have standardized TCAD models and parameters. To study its short circuit behavior, it also requires parameters calibrated to reliable high-temperature experimental data, which are not available. Therefore, a physical mobility model (PhuMob) is calibrated from 150 K to 400 K and verified to behave properly up to the melting point of Ga_2O_3 at 2200 K. BV simulation methodology is also studied systematically to make sure it is free of numerical artifacts and is verified with theoretical calculations. Finally, the short circuit simulations are performed until the maximum temperature reaches 2500 K. It is understood that beyond 2200 K, the result is no longer valid as Ga_2O_3 has melted. Therefore, the times for the maximum temperature to reach 1000 K and 2000 K are extracted and used for analysis. While the contact thermal resistance and metal thermal resistance are important in Ga_2O_3 [39][40], to study the "intrinsic" thermal limit of Ga_2O_3, all contacts are assumed to have zero thermal contact resistance and zero metal thermal resistance.

2.2 Parameters Calibrations and Device Design

There is no consensus on which model is the best to model Ga_2O_3 temperature-dependent mobility. For example, to model doping-dependent mobility, [33] uses the Arora model and [37] uses the Masetti model while [36] and [41] use Philips Unified Mobility (PhuMob) model [42]. To model the short circuit behavior of Ga_2O_3, it is best to have experimental data for calibration up to 2000 K. However, reliable high-temperature experimental data are not available. We adapt the approaches in [36] and [41] because PhuMob takes the screening of ionized impurities by charge carriers and temperature into account and it has been demonstrated that it can be extended to cryogenic temperatures in GaN [41] and Silicon [43]. Therefore, it is believed that PhuMob is suitable to model temperature-dependent mobility. Also note that in [41], it has been calibrated between 150 K and 400 K and demonstrated to match experimental diode IV with self-heating for Ga_2O_3. Thus, it is believed to be less prone to overfitting and can predict the high-temperature range well. Fig. 1 shows the electron mobility of the drift region as a function of temperature. It can be seen that it has a smooth trend up to 2000 K.

Incomplete ionization of the carriers is turned on using the parameters calibrated in [41]. Caughey-Thomas velocity saturation model is used with an electron saturation velocity of 2×10^7 cm/s, which is the peak velocity estimated using the *ab initio* method in [44]. Fermi-Dirac statistics is turned on. For convenience, the calibration works in [36] and [41] are summarized in Fig. 1 and Table I. Since the quality of the etched Fin is expected to be degraded compared to the bulk Ga_2O_3, in this study, μ_{max} and μ_{min} used for calibrating a junctionless FinFET in [36] are used in the Fin region and those for calibrating a Schottky Barrier Diode in [41] are used for the drift and drain regions which have higher mobility.

For the breakdown study, the van Overstraeten – de Man model is used for impact ionization with the parameters given in [45]. The device is assumed to be grown in the (100) direction and the corresponding parameters, *a* and *b,* are 0.79×10^6 V/cm and 2.92×10^7 V/cm, respectively. In [45], the corresponding critical electric field, E_c, is found to be 10.2 MV/cm based on certain assumptions. However, our self-consistent TCAD simulation shows that the corresponding E_c is about 8 MV/cm, which is thus used in the device design. The goal is to

design a device for an 800 V rating. By assuming a 50% margin, it is targeted to have a BV of 1200 V. Fig. 2 shows the device structure. In this study, it is assumed the substrate region is thin enough (20 μm) for the best scenario. This is possible as demonstrated in [46]. The gate work function is assumed to be 4.5 eV. Using the well-known equations for a non-punch-through design [47], the drift thickness, t_D, is

$$t_D = 2\,BV/E_C \qquad (1)$$

where BV is the desired breakdown voltage rating. It is found that t_D = 3 μm. The doping in the drift region, N_D, is given by:

$$N_D = \varepsilon\,E_C^2/(2qBV) \qquad (2)$$

where ε is the material permittivity and q is the elementary charge and it is found that N_D = 1.475×10^{17} cm^{-3}. Fig. 3 shows that the drift region is almost fully depleted when the peak electric field is near E_c. Therefore, the design is almost optimal.

A negative interface fixed charge of 4.9×10^{12} cm^{-2} is added to the oxide/Ga_2O_3 interface based on the calibration work in [36]. Moreover, self-heating is turned on in the short-circuit simulation (to be discussed) with thermal conductivity of 0.11 W/(cm·K) for the (100) direction [48].

The I_DV_G and I_DV_D curves, with self-heating of the structure in Fig. 2 are shown in Fig. 4. All contacts are assumed to have zero thermal contact and thermal resistance. The device has a threshold voltage, V_{TH}, of 4 V. Therefore, it is normally-off due to the good double gate control on the thin fin and the appropriate metal and channel work function difference. The extracted specific on-state resistance, $R_{ON,SP}$, is found to be 0.5 mΩ·cm^2 when V_G-V_{TH} = 5 V. This specific on-resistance is lower than the experimental demonstration [19] but is closer to the theoretical limit of Ga_2O_3 [1]. This suggests good room for performance advances in vertical Ga_2O_3 FinFET device technology.

3. Results and Discussions

3.1 Device Breakdown Simulations and Convergence

Ga_2O_3 is an ultra-wide bandgap material and the convergence is expected to be difficult. This is because of the very low intrinsic carrier density [1] which may result in numerical underflow during simulation. This is usually solved by adding background electron-hole pair generation to stabilize the system of linear equations. However, in this paper, we also find that the low intrinsic carrier concentration not only may hurt convergence but also may result in *wrong converged results*. This can lead to wrong conclusions in TCAD simulations.

We first study the BV of the structure in Fig. 2 with various background electron-hole pair generation rates. Simulation conditions are also modified. These include changing the mesh size (but not too coarse) in the drift region, the drain length, and also the mobility model and parameters in the channel region. Additionally, hole tunneling is also turned on to the channel from the gate with different tunneling masses but with a very low tunneling current due to the thick gate oxide. These modifications (dubbed "*weak parameters*") are expected to have minimal impact on the BV because the BV is determined by the drift layer length, drift

layer doping, and the models defined in the drift region. However, it is found that when the generation rate is small (<10^5 $cm^{-3}s^{-1}$), the BV 1) varies strongly with the weak parameters which should not have an impact on the BV, and 2) is different from the theoretical calculations in Section 2.2 if the simulation converges (as large as 2700 V) due to numerical instability.

Fig. 5 shows the BV curves of the structure in Fig. 2 under different generation rates and variations of the "weak parameters". It is found that generation rates between 10^5 $cm^{-3}s^{-1}$ and 10^{12} $cm^{-3}s^{-1}$ are required to give a correct result, i.e. BV~1200 V (corresponding to the expectation from Eqs. 1 and 2 and Fig. 3) and to have minor variation with the "weak parameters". When the generation rate is 0 cm^{-3} (red curves), a small variation in the weak parameters results in big variations in the BV. However, if the generation is too large (e.g. grey with 10^{18} cm^{-3}), the leakage is dominated by the generation but not the impact ionization initiated BV. Based on our previous simulation experience with other wide-bandgap and ultra-wide bandgap devices [34]-[36], the generation rate of 10^{12} $cm^{-3}s^{-1}$ is chosen in this study.

Fig. 6 shows the structures to be studied for short-circuit ruggedness based on the idea in the GaN FinFET inter-fin design study in [38]. There are 4 structures, namely, A) split-gate (SG), B) full-gate (FG), C) split-gate without inter-fin source (SGNS), and D) full-gate without inter-fin source (FGNS). For split-gate (SG), the gate electrode does not cover the inter-fin region, but the source electrode appears in the inter-fin region. For full-gate (FG), the gate electrode covers the inter-fin region as the source electrode. For the split-gate without an inter-fin source (SGNS), there is no source electrode in the inter-fin region, and similarly for the full-gate without an inter-fin source (FGNS).

To perform SC analysis, it is important to confirm that all structures have a larger BV than the V_{DD} to be applied in SC analysis. Fig. 7 shows the BV curves for the 4 structures with a background generation rate of 10^{12} $cm^{-3}s^{-1}$. It has been confirmed that this generation rate gives similar BV in each structure regardless of the "weak parameter" variations. It can be seen that they have almost the same BV, except for SGNS. This is because, for split-gate, the gate electrode creates a singular point at its end, resulting in a strong electric field (Fig. 8c). But, this electric field can be smoothed if there is an inter-fin source electrode with a small t_{SG} (separation between the gate and source electrode). Therefore, the inter-fin electrode (due to gate or source) avoids the strong electric field generated by the termination of the split gate. We also expect that the SGNS represents the worst case with the lowest BV because it has no inter-fin electrodes at all. Fig. 8 shows the electric field distribution of the four structures. Despite some splits having lower BV, they are all at least 200 V larger than the V_{DD} (800 V) to be used in the SC circuit simulations.

3.2 Short Circuit Ruggedness

TCAD mixed-mode simulation is then used to study the SC ruggedness of the devices with various inter-fin structures and t_{SG}. Fig. 9 shows the SC testing setup. The Ga_2O_3 vertical FinFET is simulated using the same set of models and parameters in Section 2.2 with self-heating and thermal dynamic models turned on. The width of the device in the third dimension is set up so that the total device area is 0.426 mm^2. V_{DD} is set to 800 V (i.e. at least 200 V lower than the BV found in Section 3.1) and the gate pulse increases from 0 V to V_G in 0.1 μs. V_G

varies from 5 V to 12 V in the study. The gate wire resistance is assumed to be 60 Ω and source/drain resistance and inductance are assumed to be 1 mΩ and 1 nH, respectively.

It is assumed that the source, gate, and drain contact have zero thermal contact and zero thermal metal resistance. This means the contacts are biased at 300 K. This emulates the best backside cooling condition through the drain contact as the drain contact covers the whole simulation domain at the bottom. For SG with small t_{SG}, FG, and FGNS, this also represents a perfect top-side cooling condition. Fig. 10 shows the change of drain current and the maximum temperature in the device as a function of the time when the gate pulse is applied at 0 s and raised to 9 V at 0.1 μs. It can be seen that all of them fail in less than 0.1 μs after the gate pulse is fully applied *even under a perfect double-side cooling condition*. Therefore, the short-circuit withstand time, SCWT, is less than < 0.1 μs. This is because of the low thermal conductivity of Ga_2O_3.

Fig. 11 shows the temperature distribution for selected structures at t = 0.1 μs (i.e. V_G just reaches 9 V). The heat generated in the drift region is confined at the center of the drift region and cannot be dissipated easily, resulting in catastrophic failure. It can also be seen that SGNS is the worst even though it has a similar electric field and current at the hotspot because it has the worst top-side cooling.

A lower V_G is then used and it is found that V_G needs to be as low as 5.7 V (i.e. only 1.7 V gate overdrive) to achieve an SCWT > 1 μs with T = 2000 K being defined as the failure point. Fig. 12 shows the change of drain current and the maximum temperature in the device as a function of time when V_G = 5.7 V. For the SG cases, it can be seen that smaller t_{SG} gives a longer SCWT because it is easier for the source electrode to help conduct the heat. SGNS is the worst because the source electrode is not in the inter-fin region to dissipate heat. This is the same for V_G = 9 V in Fig. 10.

However, it is surprising that the FG and FGNS have a much lower SCWT. This is consistent with the observation that FG and FGNS also have lower SCWT in the V_G = 9 V case as shown in Fig. 10. It was originally expected that the full gate structures have the best topside thermal conduction since the gate is very close to the drift region in the inter-fin region. It is believed that this is because the SCWT is no longer limited by self-heating but by electrostatics. As a result, this is more obvious when V_G is 5.7 V than 9 V. For full gate structures, when V_G increases, it causes the accumulation of electrons under the inter-fin region. This provides a conductive path and triggers impact ionization at an earlier time. Fig. 13 shows the impact ionization rate at t = 0.4 μs at the inter-fin region for FG, FGNS, SGNS, and SG. FG and FGNS have the impaction ionization spreading into the inter-fin region under the gate.

Therefore, SG with small t_{SG} has the highest SCWT.

From the SCWT perspective, even though the device is designed to have $R_{ON,SP}$ = 0.5 mΩ·cm^2 under 5 V gate overdrive (Fig. 4), it can only safely operate at 1.7 V gate overdrive with $R_{ON,SP}$ = 0.83 mΩ·cm^2.

To further understand the role of the low thermal conductivity of Ga_2O_3 in SWCT, GaN thermal conductivity is also used in the simulation with everything else the same. Fig. 14 shows the SCWT of SG with t_{SG} = 60 nm as a function of $R_{ON,SP}$ (which corresponds to different V_G) when the device has Ga_2O_3 or GaN thermal conductivities, which are 0.11 W/(cm·K) and 2.53

W/(cm·K), respectively. For SCWT > 1 ms, it is marked as 1 ms. It can be seen that, with GaN thermal conductivity, the device never fails except when V_G = 12 V, which corresponds to $R_{ON,SP}$ = 0.4 mΩ·cm^2.

It is also worth noting that based on the simulation, Ga_2O_3 FinFET will melt (reaches 2200 K) before the thermal runaway (current increases abruptly). This is because it has a higher bandgap (4.8 eV) than GaN (3.4 eV) and SiC (3.26 eV) while having a lower melting point (2200 K) than GaN (2773 K) and SiC (3003 K).

The study so far is to investigate the SCWT due to the limitations of Ga_2O_3's thermal conductivity and melting point in which perfect double-side cooling is assumed. In reality, the metal contact may fail (either melt or damaged) first if the top-side thermal contact is not perfect. We further investigate the SCWT without top-side cooling and define the SCWT as the time when the S and G maximum temperature reaches 900 K (~aluminum's melting point). As shown in Fig. 14, even with V_G = 5 V (overdrive being 1 V and $R_{ON,SP}$ = 1.17 mΩ·cm^2), the SCWT still cannot reach 1μs. In general, the source contains Al [20]. Therefore, a new alloy might be needed to avoid the SCWT being limited by the melting point of the contact. This is not an issue for the gate material as it contains only Au and Ni with high melting points.

To understand if the finding is valid for other gate lengths, L_G = 0.75 μm and L_G = 0.95 μm are also simulated. They are found to have the same V_{th} as L_G = 0.65 μm. Although they have different $R_{ON,SP}$ due to different channel lengths, they have the same SCWT to $R_{on,sp}$ relationship as shown in Fig. 15.

Conclusions

In this paper, we demonstrated the importance of selecting the correct models and setups to perform Ga_2O_3 vertical FinFET TCAD simulations, particularly under high voltage and high current. This is expected to be applicable to other ultra-wide bandgap device simulations. Particularly, one needs to be aware of the possibility of converging to wrong solutions if the setup is incorrect, particularly in BV simulation using impact ionization models. SCWT is simulated on an 800 V-rated Ga_2O_3 vertical FinFET. It is found that, due to the low thermal conductivity, the advantage of Ga_2O_3 is compromised. For the device designed, $R_{on,sp}$ is 66% more than it can achieve in order to achieve an SCWT > 1 μs. It is also found that the full gate (FG) structure has the worst SCWT due to electrostatics, but split-gate (SG) has the lowest BV. SG with inter-fin source and small t_{SG} is the best from the BV and SCWT perspectives. Based on the simulation, it is also found that Ga_2O_3 might also melt before the thermal runaway. These results present the first short circuit ruggedness studies of Ga_2O_3 vertical FinFETs and provide key guidance for their design and protections.

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Tables

	Si in Ga_2O_3 [41]	**Si in Ga_2O_3 [36]**	**Si in Ga_2O_3 [This Work]**
Device Type	Schottky Barrier Diode	FinFET	FinFET
μ_{max} ($cm^2/V{\cdot}s$)	123	18.45	18.45 (Fin) /123 (Rest)
μ_{min} ($cm^2/V{\cdot}s$)	80	12	12 (Fin) /80 (Rest)

θ	1.8	1.8	1.8
$N_{ref,1}$ (cm^{-3})	2×10^{17}	2×10^{17}	2×10^{17}
α_1	0.9	0.9	0.9

Table 1: Phumob parameters used in various TCAD simulations. The symbols are the same as those in Table 1 of [41]. θ is the exponent of temperature dependence due to lattice scattering.

Figures

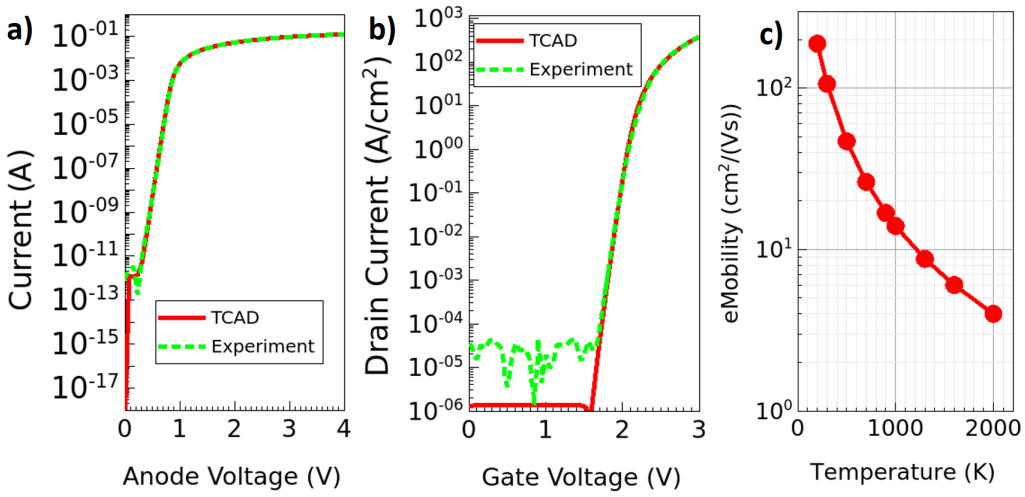

Figure 1. Comparison of TCAD simulation and experimental results for Ga_2O_3 Schottky Barrier Diode in [41] (a) and junctionless FinFET in [19] (b). The corresponding PhuMob parameters are shown in Table I. (c) shows the electron mobility in the drift region as a function of temperature when the doping is 1.475×10^{17} cm^{-3}.

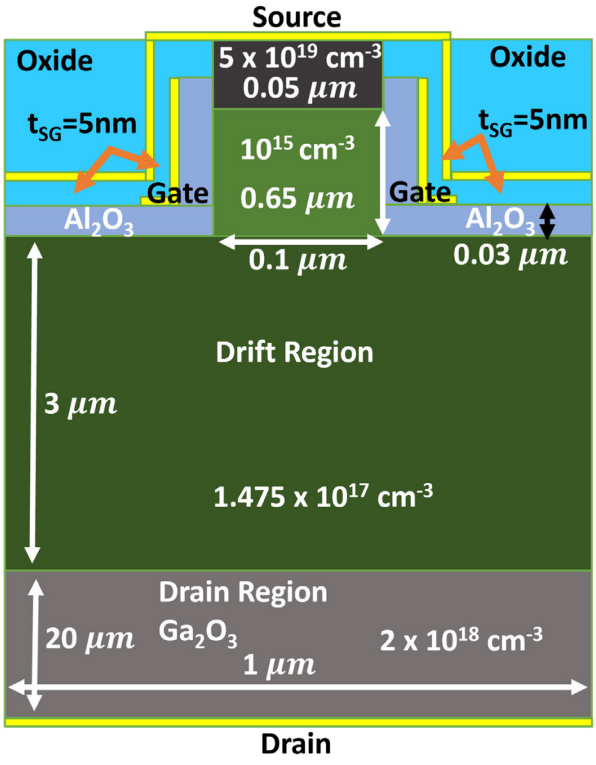

Figure 2. Structure of the junctionless FinFET studied in this paper (not to scale for clarity).

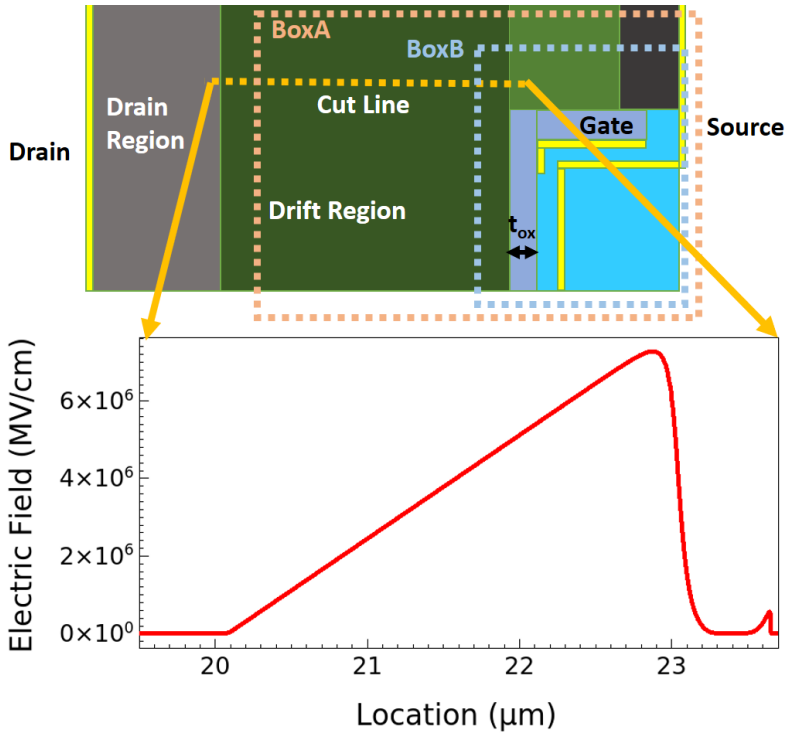

Figure 3. Top: Right half of the structure in Fig. 2 rotated by 90 degrees clockwise. Bottom: Electric field distribution along the "Cut Line" at ~1200 V with background electron-hole pair generation 10^{12} $cm^{-3}s^{-1}$. Location at 20 μm is the drift/drain interface.

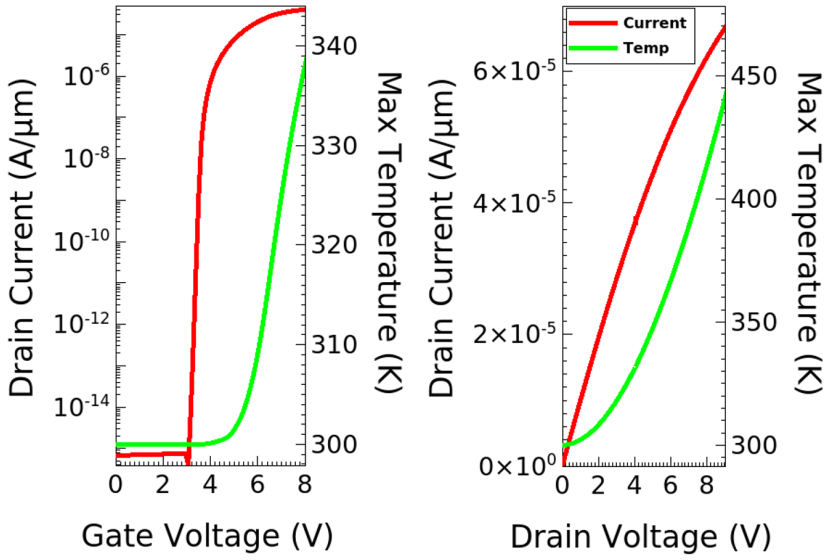

Figure 4. I_D-V_G with $V_D = 5$ V and I_D-V_D with $V_G = 9$ V for the structure in Fig. 2. Maximum temperature in the device is also shown.

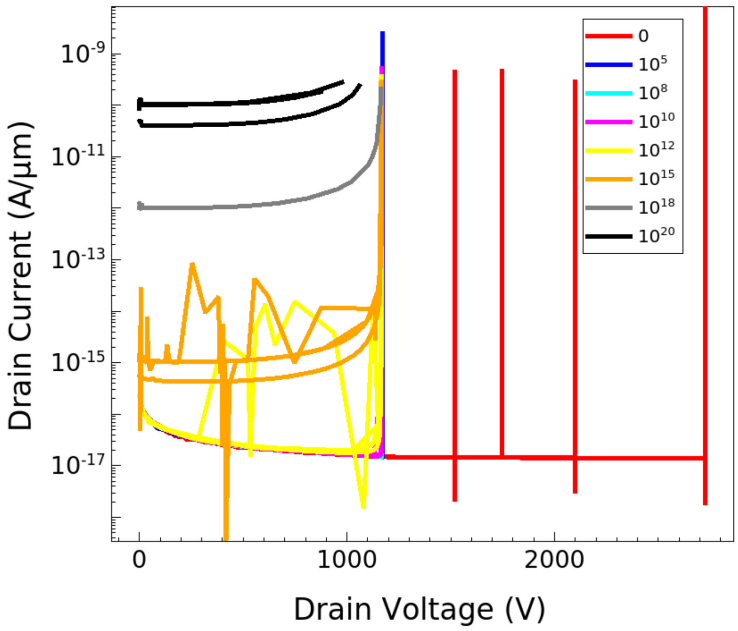

Figure 5. BV curves of the structure in Fig. 2 under different background carrier generation rates. Each color group has the same background generation rate and within the group, each curve represents the device with different "weak parameters", i.e, drift mesh, drain length, channel mobility model and parameter, and channel hole tunneling mass.

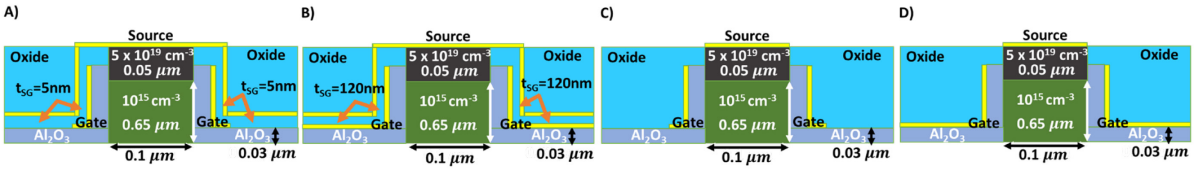

Figure 6. The Fin region designs of the device studied in this paper. A) split-gate (SG), B) full-gate (FG), C) split-gate without inter-fin source (SGNS), and D) full-gate without inter-fin source (FGNS). t_{SG} is varied in the SC study.

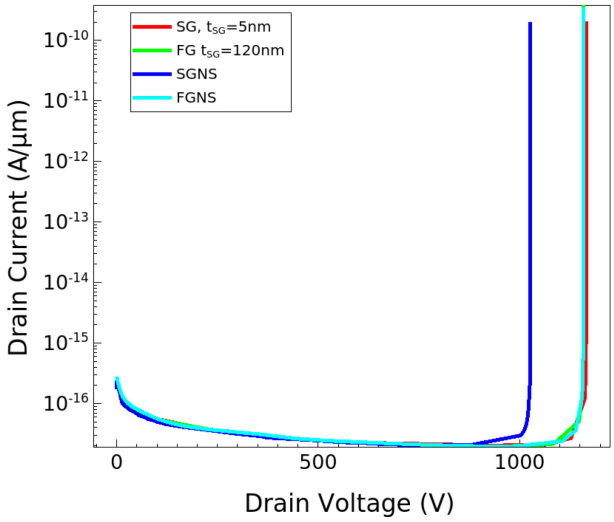

Figure 7. BV curves of the structures in Fig. 6 with background generation of 10^{12} $cm^{-3}s^{-1}$. Note that the drain current decreases at the beginning due to the displacement current as this is a transient simulation.

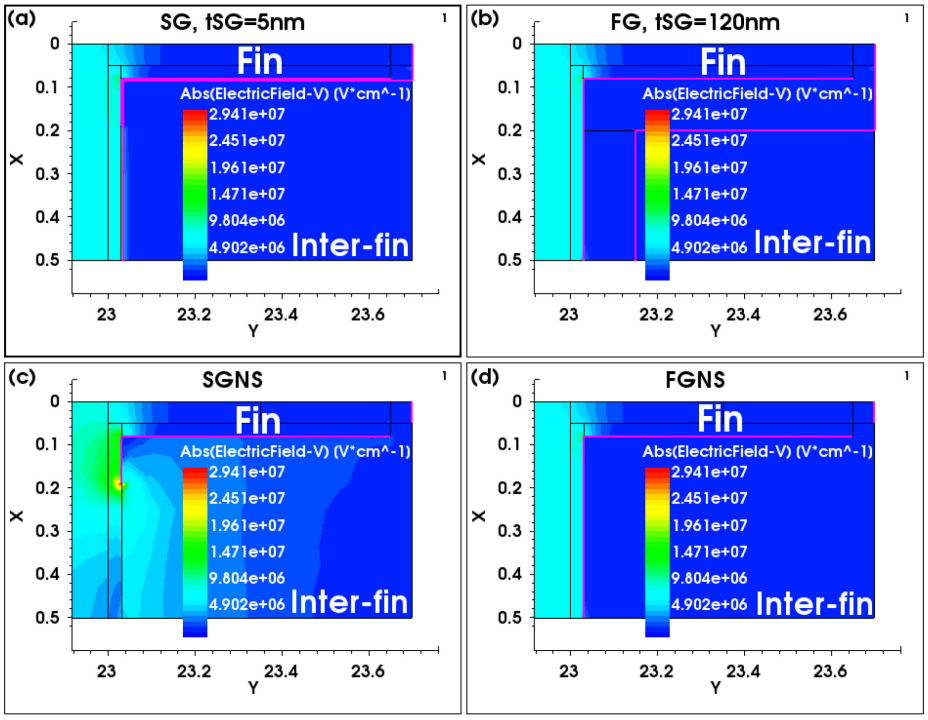

Figure 8. Electric field distribution of the structures in Fig. 7 at 1000 V around the fin and inter-fin regions. *Note that only half of the structure is shown and the structure is rotated 90º clockwise compared to the structure in Fig. 6*. The pink lines are the gate and source electrodes. The region shown is also "BoxB" in Fig. 3.

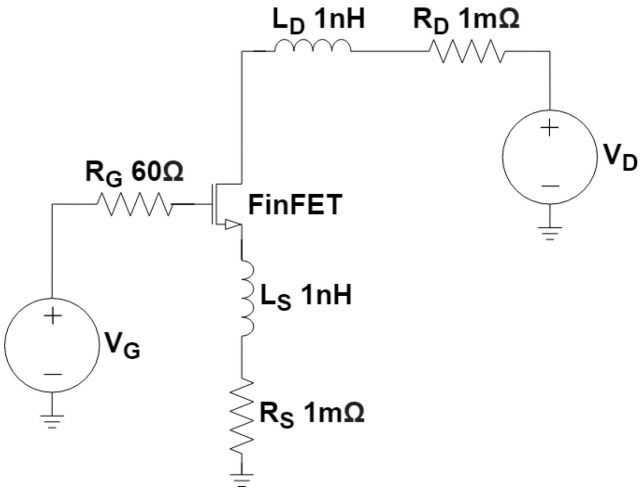

Figure 9. SC testing setup.

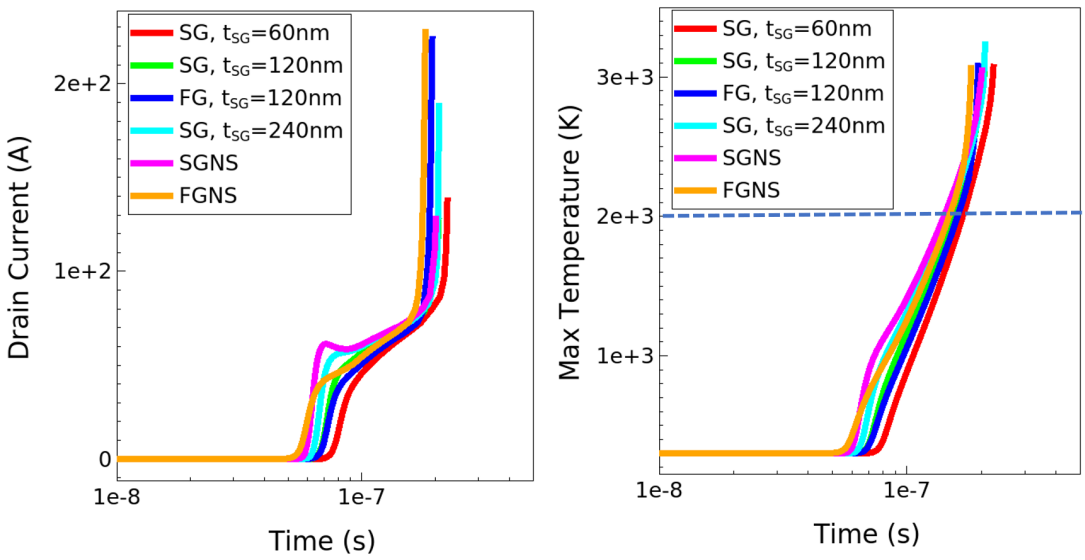

Figure 10. I_D and maximum device temperature, T_{max}, as a function of time in the SC simulations for various devices when V_G = 9 V. Note that the melting point of Ga_2O_3 is 2200 K. Therefore, only the simulations below 2200 K are considered to be valid.

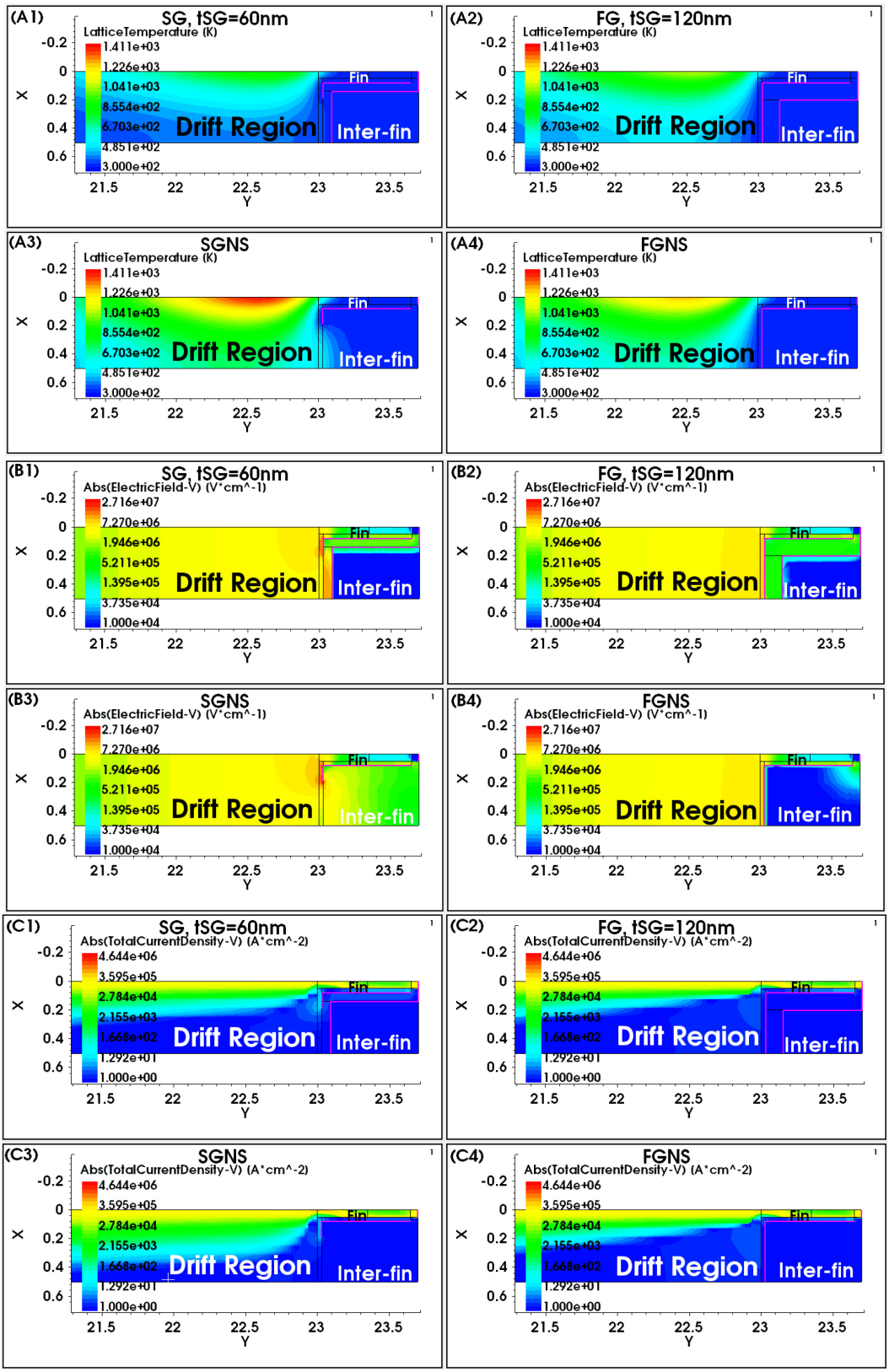

Figure 11. Temperature (A1-A4), electric field (B1-B4), and total current (C1-C4) distributions of selected structures at t = 0.1 μs in the SC simulation with V_G = 9 V. The region showed corresponds to "BoxA" in Fig. 3.

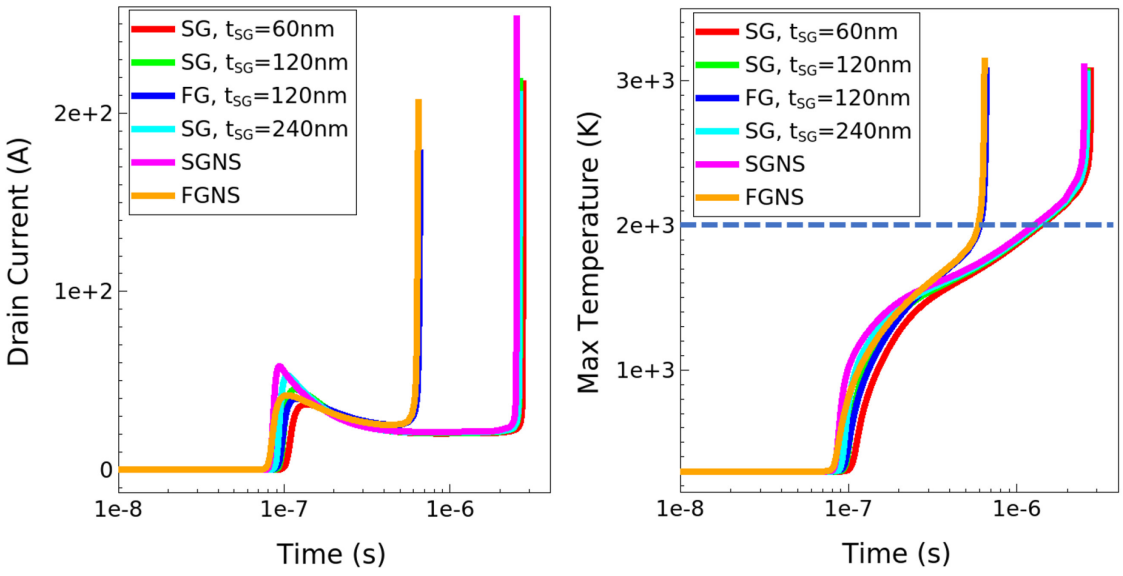

Figure 12. I_D and maximum device temperature, T_{max}, as a function of time in the SC simulations for various devices when V_G = 5.7 V.

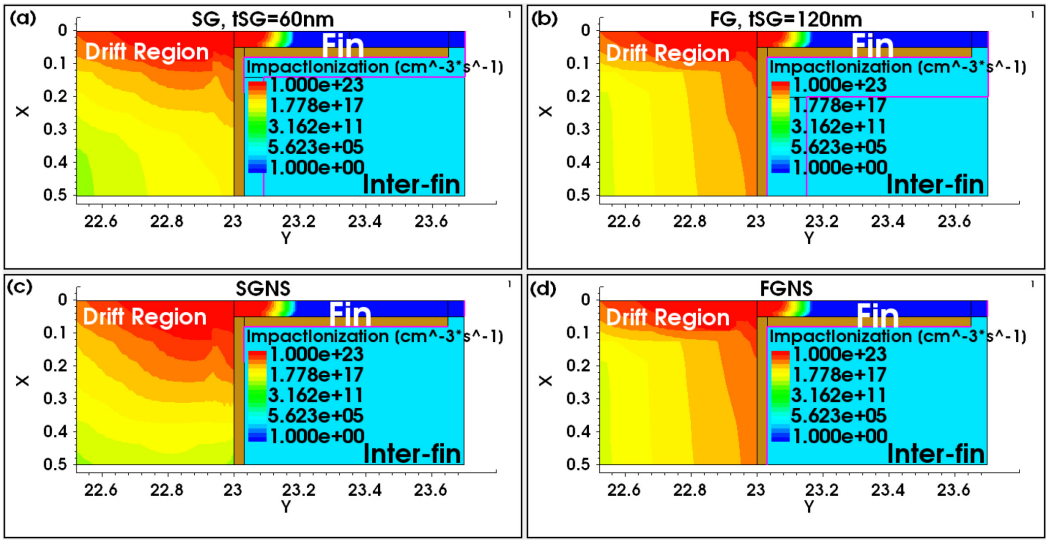

Figure 13. Impact ionization of selected structures at t = 0.4 μs in the SC simulation with V_G = 5.7 V. The region showed corresponds to "BoxB" in Fig. 3.

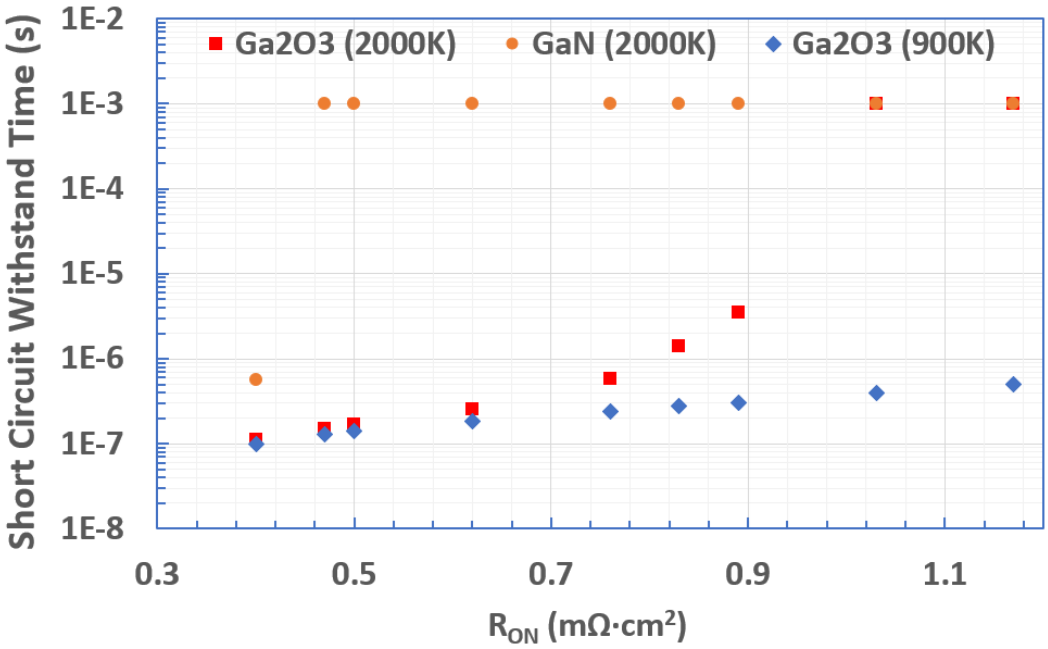

Figure 14. SCWT of SG, t_{SG} = 60 nm as a function of $R_{ON,SP}$ for thermal conductivity of 0.11 W/(cm·K) (Ga_2O_3) and 2.53 W/(cm·K) (GaN). L_G = 0.65µm. Two definitions of SCWT are used, namely the time when the maximum temperature in Ga_2O_3 reaches 2000K (with top-side cooling) and the time when the peak temperature at source and gate contacts reaches 900K (when there is no top-side cooling).

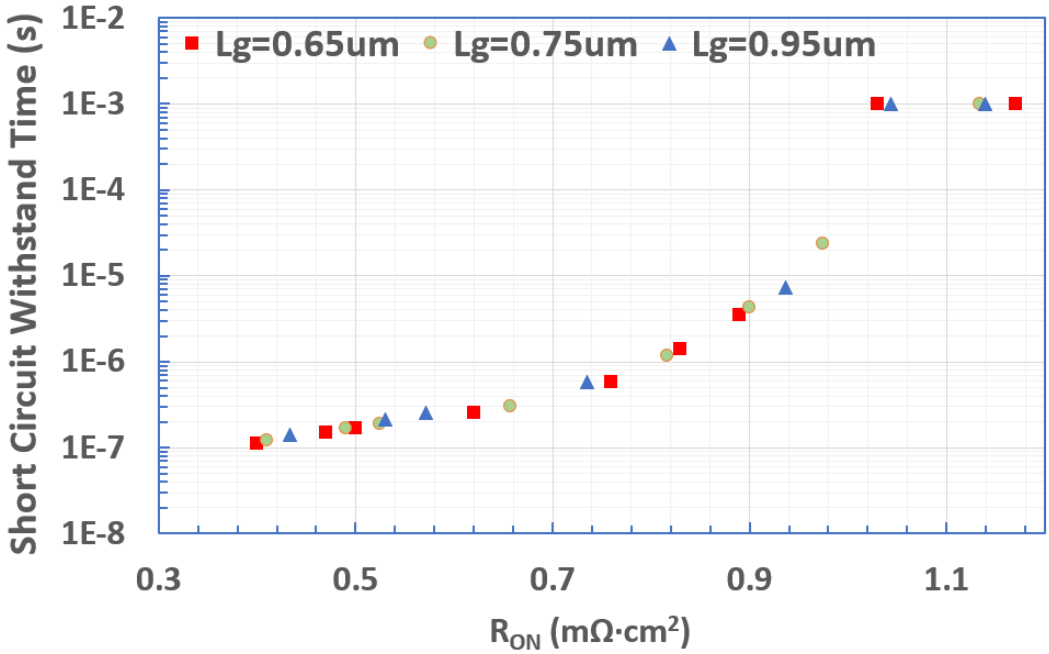

Figure 15. SCWT of SG, t_{SG} = 60 nm as a function of $R_{ON,SP}$ for various L_G using Ga_2O_3 thermal conductivity of 0.11 W/(cm·K). SCWT is defined as the time when the maximum temperature in Ga_2O_3 reaches 2000K (with top-side cooling).