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Graphene nanopattern as a universal epitaxy platform for single-crystal membrane production and defect reduction

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Heterogeneous integration of single-crystal materials offers great opportunities for advanced device platforms and functional systems[1]. Although substantial efforts have been made to co-integrate active device layers by heteroepitaxy, the mismatch in lattice polarity and lattice constants has been limiting the quality of the grown materials[2]. Layer transfer methods as an alternative approach, on the other hand, suffer from the limited availability of transferrable materials and transfer-process-related obstacles[3]. Here, we introduce graphene nanopatterns as an advanced heterointegration platform that allows the creation of a broad spectrum of freestanding single-crystalline membranes with substantially reduced defects, ranging from non-polar materials to polar materials and from low-bandgap to high-bandgap semiconductors. Additionally, we unveil unique mechanisms to substantially reduce crystallographic defects such as misfit dislocations, threading dislocations and antiphase boundaries in lattice- and polarity-mismatched heteroepitaxial systems, owing to the flexibility and chemical inertness of graphene nanopatterns. More importantly, we develop a comprehensive mechanics theory to precisely guide cracks through the graphene layer, and demonstrate the successful exfoliation of any epitaxial overlayers grown on the graphene nanopatterns. Thus, this approach has the potential to revolutionize the heterogeneous integration of dissimilar materials by widening the choice of materials and offering flexibility in designing heterointegrated systems.

With the advancement of current electronic and photonic devices, demands for the heterogeneous integration of dissimilar materials are continuously increasing to realize multifunctional chips on a single platform. To date, the heterointegration of single-crystalline materials has been carried out either by monolithic approaches using heteroepitaxy or by the transfer of semiconductor membranes from foreign substrates. For heteroepitaxy, elemental semiconductors such as Si and Ge have been widely utilized as epitaxial templates for growing compound semiconductors owing to their substantially lower costs and compatibility with mature platforms. However, heteroepitaxy cannot prevent the formation of crystalline defects such as dislocations and antiphase boundaries (APBs), which severely deteriorate the device performance[4]. Although various approaches have been proposed to mitigate this issue, such as employing metamorphic buffer layers or dislocation filtering structures, these methods cannot completely eliminate such epitaxial defects[5].

On the other hand, layer transfer techniques can be employed to integrate dissimilar materials without being restricted to lattice-matching requirements[3,6]. For this, active device layers are chemically, mechanically or optically released from the substrate and stacked onto a foreign substrate of interest. However, the applicability of these methods is limited by many technical challenges, such as poor controllability, low throughput and damage to the substrate[7–11]. Recently, a two-dimensional material-based layer transfer technique combined with remote epitaxy has been introduced as a promising method to overcome these issues[12–14]. Remote epitaxy allows direct growth on graphene-coated wafers[15], and the epitaxial layers on graphene can be instantaneously and precisely exfoliated off of the substrate from the weak graphene interface[16,17]. Despite such advantages, remote epitaxy can be accomplished only for compound semiconductors[15], and thus, cheap elemental materials such as Si and Ge cannot be utilized as epitaxial layers or growth templates in remote epitaxy[18].

Here we demonstrate a universal solution that can substantially reduce crystallographic defects in heteroepitaxial layers and allow fast mechanical layer release. This is realized by the epitaxy

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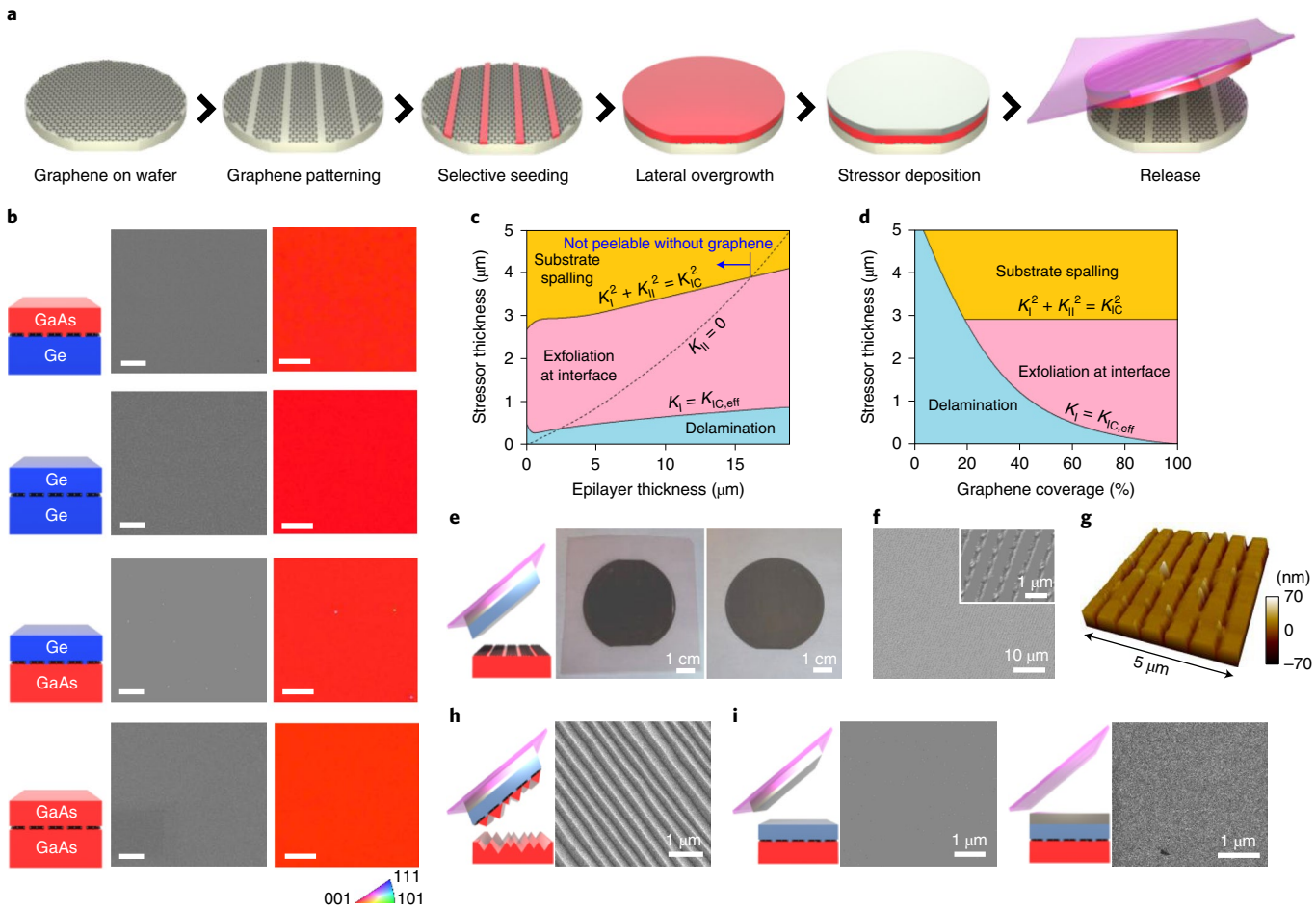

Fig. 1 | Graphene nanopattern for single-crystal membrane growth and release. a, Schematic of epitaxy on nanopatterned graphene and layer release. **b**, Plan-view SEM images (left) and EBSD maps (right) of GaAs and Ge grown on GaAs and Ge substrates, showing planarized single-crystalline thin films. Scale bars, 2 μm. **c**, Three modes of peeling as a function of stressor thickness and epilayer thickness at the Ni stress level of 600 MPa and graphene coverage of 70% on the Ge substrate. The dashed line represents the natural spalling depth without graphene. **d**, Effect of graphene coverage on the peeling modes at the stressor stress of 600 MPa and epilayer thickness of 1 μm. **e**, Photograph of an exfoliated GaAs film (left) and remaining two-inch Ge wafer (right). **f**,**g**, Plan-view SEM images (**f**) and AFM image (**g**) of the substrate after peeling. **h**, Plan-view SEM image of GaAs substrate in the spalling regime. **i**, Plan-view SEM images of the sample surfaces in the delamination regime, showing delamination at the Ni/epilayer interface (left) and tape/Ni interface (right).

on nanopatterned graphene (EPG) technique, where we perform lateral overgrowth on wafers coated with patterned graphene. The EPG technique provides the following unique features: (1) epilayers can be readily released from the wafer by simple mechanical exfoliation due to reduced interface toughness with graphene nanopatterns; (2) elemental materials can not only be utilized as substrates but be made as freestanding membranes due to selective nucleation; (3) APB-free growth of compound semiconductors is permitted on elemental semiconductor substrates due to the blockage of step edges by graphene; and (4) dislocations can be substantially reduced in lattice-mismatched heteroepitaxy due to lateral relaxation by the flexibility and chemical inertness of graphene.

Figure 1a shows the schematic of the process flow for epitaxy on graphene nanopatterns and the release of epilayers. We first utilize graphene-coated Ge(100) substrates as a growth template, on which Ge and GaAs (that are quasi-lattice-matched) are grown through graphene stripes. Graphene is first grown on an on-axis Ge substrate, followed by lithography and dry etching (Methods and Supplementary Figs. 1 and 2 provide the detailed processes). The growth of Ge and GaAs on GaAs wafers through patterned graphene is also studied. The scanning electron microscopy (SEM) images (Fig. 1b) show that Ge and GaAs films grown by metal–organic chemical vapour deposition (MOCVD) are fully planarized after growing a nominally 1-μm-thick film (Methods provides the detailed growth processes). The electron backscatter diffraction (EBSD) maps and X-ray diffraction characterizations reveal that the entire film is single-crystalline (Fig. 1b and Supplementary Fig. 3), due to the selectivity for the exposed region over the graphene-coated region (Supplementary Fig. 4 shows the density of nuclei). The merging and planarization of the film from the patterns are governed by the pattern geometry and crystal-orientation-dependent growth rates (Supplementary Fig. 5)[19].

We developed analytical solutions from conventional spalling theory to estimate the criteria for exfoliation at the graphene interfaces. In principle, the generation and propagation of cracks through a medium are governed by stress intensity factors, K_I (opening mode) and K_{II} (shear mode), exerted by the stressor layer, and fracture toughness, K_{IC}, of the spalled medium[20] (Supplementary Section 1 provides the detailed theory). When graphene nanopatterns are introduced, the presence of graphene effectively weakens the interface because the bonding strength of the graphene-covered surface is marginal[21,22]. For a graphene coverage percentage of x, the effective fracture toughness at the interface becomes

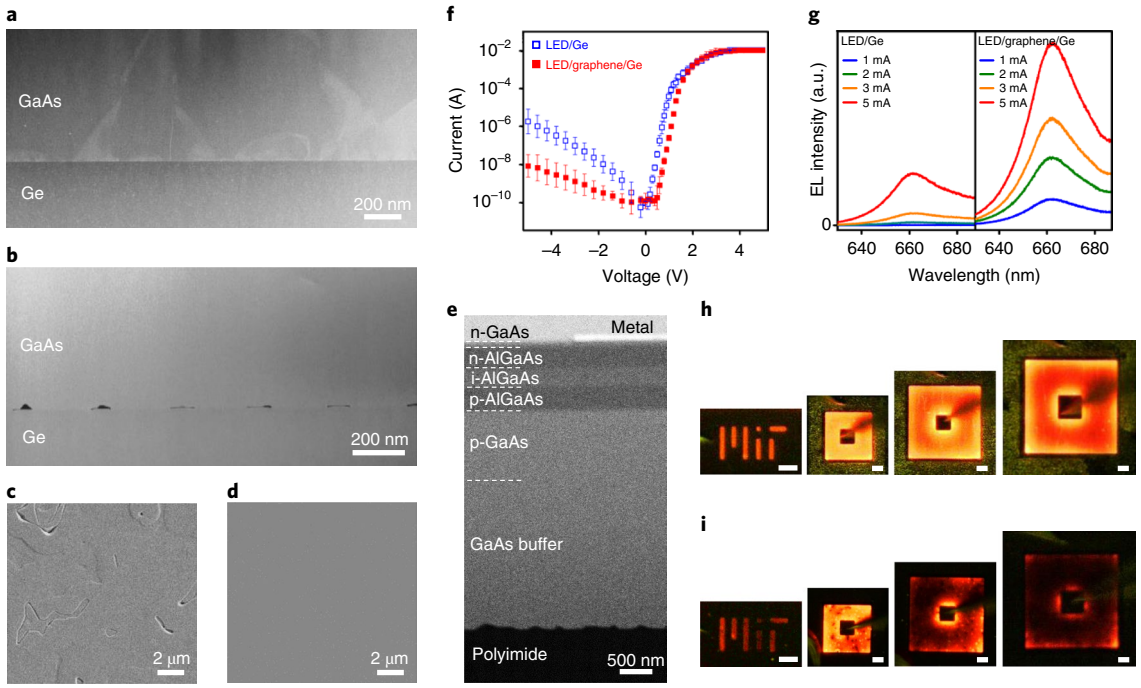

Fig. 2 | APB elimination by graphene nanopatterns. a,**b**, Cross-sectional STEM images of GaAs directly grown on Ge (**a**) and nanopatterned graphene-coated Ge (**b**). **c**,**d**, Plan-view SEM images of AlGaAs red LEDs grown on bare Ge (**c**) and nanopatterned graphene-coated Ge (**d**). **e**, Cross-sectional SEM image of LED fabricated by exfoliating the LED structure from the substrate and transferring onto the polyimide/silicon substrate. **f**, *I*–*V* curves of the fabricated LEDs on Ge with and without nanopatterned graphene. The error bars represent standard deviation after log transformation. **g**, Comparison of EL spectra of LEDs on Ge without (left) and with (right) nanopatterned graphene under various injection currents. **h**,**i**, Microscopic photographs of EL from red LEDs with different sizes and geometries on nanopatterned graphene-coated Ge (**h**) and bare Ge (**i**). Injection currents are 3, 3, 5 and 7 mA (from left to right). Scale bars, 10 μm.

$$K_{IC,eff} = (1 - x)K_{IC}.$$

As the thickness of the epilayer deviates from the spalling depth ($K_{II} \neq 0$), the condition for spalling changes to

$$K_I^2 + K_{II}^2 > K_{IC}^2.$$

On the other hand, the delamination of a stressor layer from the surface of the epilayer occurs when the energy release rate provided by the stressor is not sufficient for crack propagation, expressed as

$$K_I < K_{IC,eff}.$$

Outside these spalling and delamination regimes, exfoliation occurs at the graphene interface (Supplementary Section 1 and Supplementary Figs. 6–9 provide more information).

The exfoliation criteria we developed (Fig. 1c,d) agree well with our experimental results. As shown in the photograph and SEM images (Fig. 1e,f and Supplementary Figs. 10 and 11), the entire area of the 1-μm-thick epilayer can be exfoliated off of the wafer. The surface morphology of the substrate following exfoliation is flat on the graphene-covered regions, whereas the exposed regions show undulation with a height fluctuation of tens of nanometres (Fig. 1g and Supplementary Fig. 12). When the accumulated strain energy within the Ni stressor layer is high ($K_I^2 + K_{II}^2 > K_{IC}^2$), the substrate spalls and reveals its zig-zag {110} cleavage planes of GaAs and a relatively planar (100) plane for Ge (Fig. 1h and Supplementary Fig. 11c)[20,21]. On the other hand, when the stress is too low ($K_I < K_{IC,eff}$), then cracks cannot propagate, resulting in the delamination of the Ni layer or the handling tape (Fig. 1i). The same principle can be applied to produce freestanding membranes for different materials, too (Supplementary Fig. 13). This is in contrast to the conventional controlled spalling method, wherein the spalling depth cannot be reliably controlled and the spalled surface is roughened[7,8].

We also show that the EPG technique can eliminate the formation of APBs in III–V epilayers. The formation of APBs is unavoidable in conventional III–V epitaxy on elemental substrates of on-axis (100) orientation due to the presence of monoatomic steps on the surface[23]. Thus, APBs are clearly observed when GaAs is directly grown on Ge(100) (Fig. 2a). However, our EPG shows the complete elimination of APBs when the alignment of graphene stripes is along the <110> direction of the Ge surface. As shown in Figs. 1b and 2b, the GaAs film grown on graphene stripes aligned to the <110> direction exhibits no APB. The enhancement in crystal quality by APB elimination is also confirmed by X-ray diffraction characterizations (Supplementary Fig. 14). Interestingly, APBs still appear for GaAs on graphene patterned along the <100> direction (Supplementary Fig. 15). We speculate that this is because step edges tend to form along the <110> direction due to surface reconstruction[24], and such <110> steps can be periodically covered by graphene patterns along the <110> direction. For APBs to form from graphene nanopatterns, more than two step edges need to coexist on the exposed region between two graphene stripes, which is unlikely to occur in our pattern dimensions[25].

The impact of APB elimination is confirmed by comparing the optoelectronic and electronic performances of III–V devices. AlGaAs-based red light-emitting diodes (LEDs) grown on patterned graphene are APB-free, whereas those directly grown on Ge exhibit APBs in their microstructures (Fig. 2c,d). When we fabricated these LED devices (Methods and Fig. 2e), we observed a higher reverse-bias dark current and a higher forward-bias recombination current for LEDs with APBs directly grown on Ge (Fig. 2f), substantiating the superior material quality of APB-free LEDs grown on patterned graphene. This is also substantiated by electroluminescence

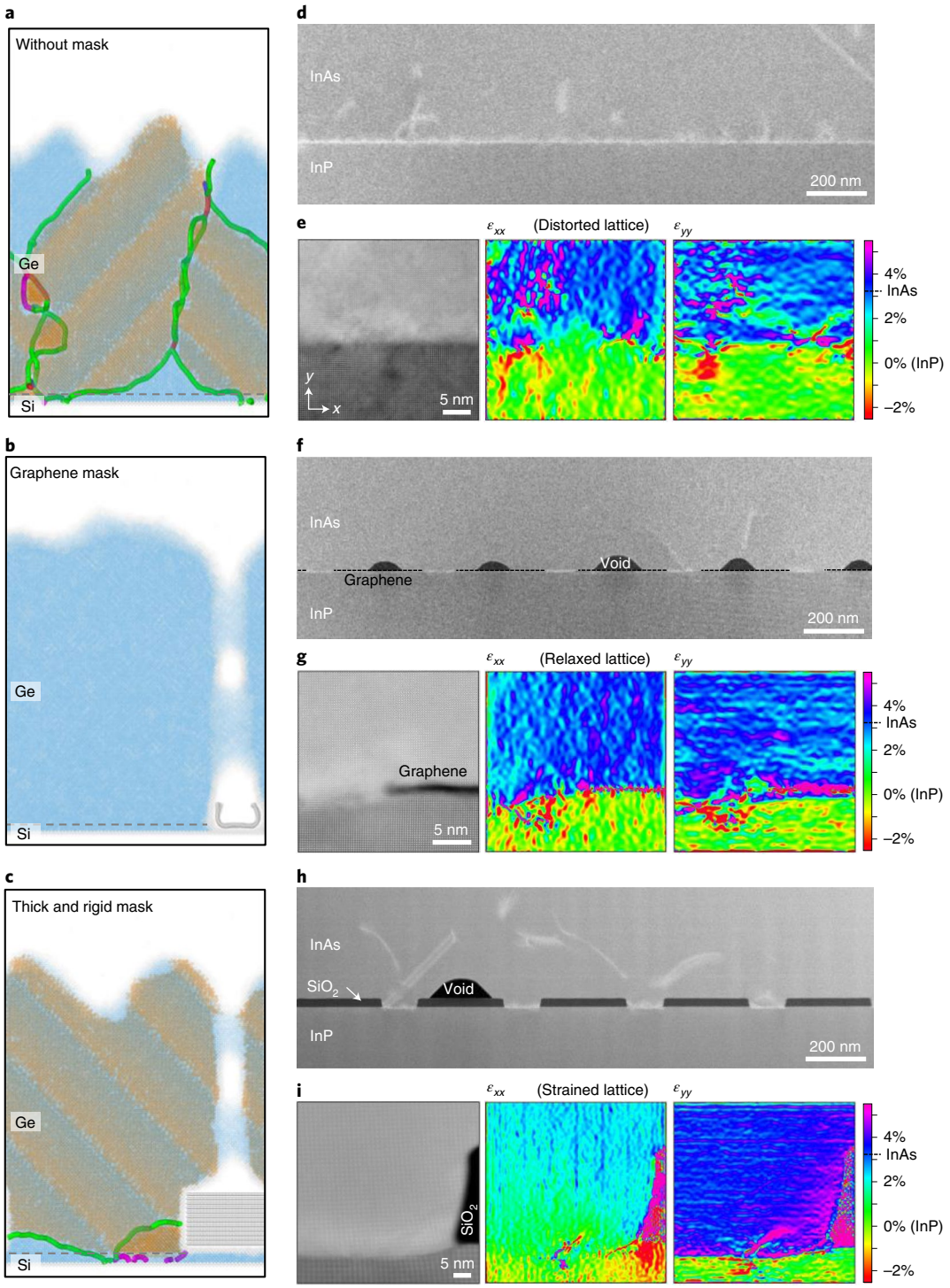

Fig. 3 | Defect reduction in lattice-mismatched heteroepitaxy by graphene nanopatterns. a–c, MD simulations of heteroepitaxy without graphene (**a**), on thin and flexible graphene mask (**b**) and on thick and rigid mask (**c**). Dislocations are coloured according to their Burgers vector: blue for 1/2 <110>, green for 1/6 <112>, purple for 1/6 <110> and cyan for 1/3 <111>. Atoms are coloured as blue and transparent for the perfect diamond cubic structure and orange and opaque for stacking faults. The carbon atoms are coloured grey and the epilayer/substrate interfaces are indicated as dashed lines. **d**, Low-magnification STEM image of InAs directly grown on InP without a mask. **e**, High-resolution STEM image (left) and corresponding GPA maps showing in-plane (centre) and out-of-plane (right) strain. **f**, Low-magnification STEM image of InAs grown on graphene pattern. **g**, High-resolution STEM image and corresponding GPA maps at the edge of graphene, showing relaxed InAs film with slightly deformed graphene. **h**,**i**, Same set of data for InAs grown on SiO_2 pattern, showing severe strain at the interface and at the mask edge. Enlarged atomic-resolution STEM image of **i** is shown in Supplementary Fig. 23.

(EL) measurements, which indicate a significantly brighter EL and efficient current spreading in LEDs grown on patterned graphene compared with LEDs without graphene (Fig. 2g–i).

We next show the defect reduction and strain relaxation in lattice-mismatched heteroepitaxial systems, which is conducted by theoretically and experimentally comparing heteroepitaxy on

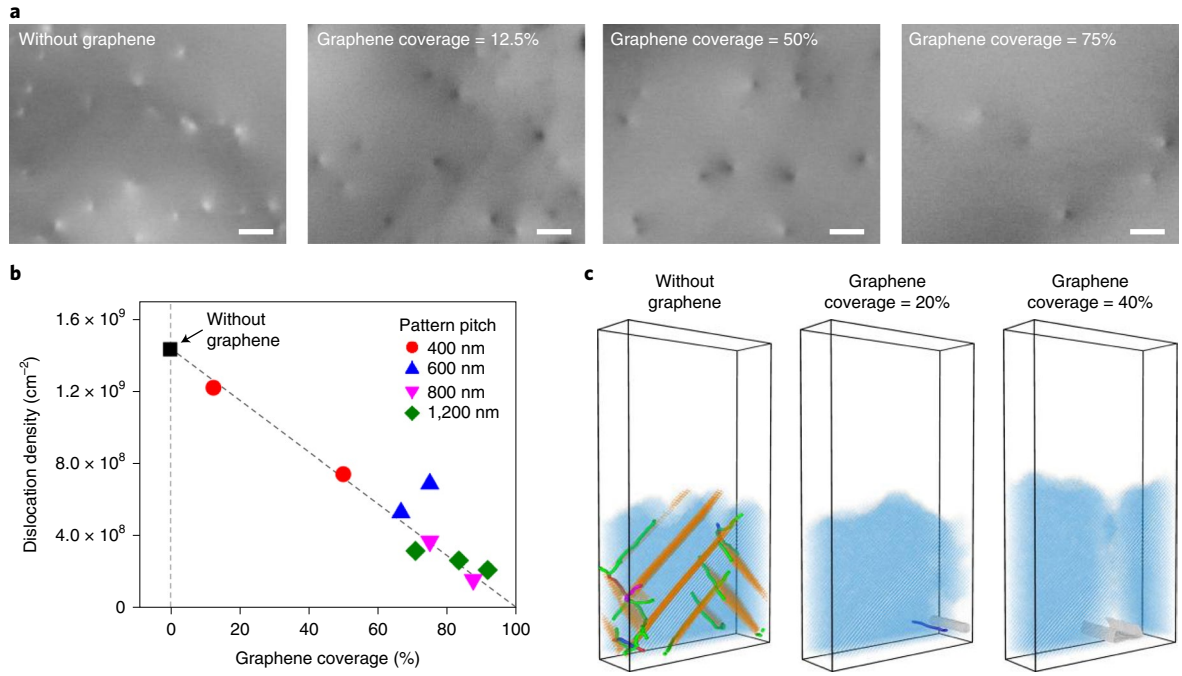

Fig. 4 | Effect of graphene coverage. a, ECCI images of InAs grown on nanopatterned graphene-coated GaAs with different graphene coverages. Scale bars, 200 nm. **b**, Surface dislocation density as a function of graphene coverage measured by ECCI. **c**, MD simulations of heteroepitaxy of Ge on Si(100) with different mask widths covering 0%, 20% and 40% of the surface, showing a decrease in defects by increased graphene coverage. The colour coding is the same as that in Fig. 3.

patterned graphene with direct heteroepitaxy and SiO_2 mask-based conventional selective-area epitaxy. In three-dimensional molecular dynamics (MD) simulation models, we studied the epitaxy of Ge on Si(100) as a representative case of ~4% lattice-mismatched systems. Three cases are investigated: direct epitaxy without masks, epitaxy with thin and flexible masks (analogous to graphene), and epitaxy with thick and rigid masks (analogous to SiO_2) (Methods provides the detailed MD simulation setup). Figure 3a shows the direct heteroepitaxy case without masks, in which multiple misfit and threading dislocations are formed due to substantial lattice mismatch, along with stacking faults. In the presence of flexible monolayer graphene masks, the formation of dislocations and stacking faults is effectively suppressed (Fig. 3b). The deformation of graphene is clearly observed by laterally accommodating the misfit strain. On the other hand, rigid patterns exhibit strain buildup at the edges of the mask as it cannot dynamically accommodate misfit strain at the edges, resulting in misfit dislocations, threading dislocations and stacking faults (Fig. 3c and Supplementary Fig. 16).

Experimentally, we study the heteroepitaxy of InAs on InP substrates with 3.2% lattice mismatch as a model system. Heteroepitaxy is performed on both monolayer graphene and 30-nm-thick SiO_2 masks with the same mask width and periodicity. Compared with the case of the direct growth of 1-μm-thick InAs on InP, a substantial reduction in dislocations is observed for 1-μm-thick InAs grown on graphene patterns, as shown in the scanning transmission electron microscopy (STEM) images (Fig. 3d,f). Geometrical phase analysis (GPA) at the interfaces shows that the lattice near the interface is distorted in direct heteroepitaxy (Fig. 3e), whereas the strain is mostly relaxed near the edge of graphene (Fig. 3g). The high-resolution STEM images and GPA maps (Fig. 3g and Supplementary Fig. 17) clearly show the slight bending of graphene near the edge and complete relaxation of strain in the film above graphene, which substantiates graphene's unique effect on dislocation reduction by its bendability and chemical inertness[26,27]. On the other hand, SiO_2 patterns are less effective than graphene patterns in dislocation reduction (Fig. 3h), as predicted by our simulations. The epilayer is only slightly relaxed near the edges of the SiO_2 mask (Fig. 3i) due to the rigidity and thickness of SiO_2, inducing localized strain (denoted by an arrow in Supplementary Fig. 17). Therefore, these findings clarify that the deformable and slippery nature of graphene provides an additional path for strain relaxation and enables the reduction in dislocations, whereas nucleation and threading of new dislocations are observed at the edges of SiO_2 masks. It should be noted that the effective elimination of APBs by the EPG technique is also confirmed for a lattice-mismatched heteroepitaxy system such as InGaAs on graphene-coated Ge substrates (Supplementary Fig. 18). In addition, heteroepitaxial films on patterned graphene are successfully released from the substrates as in the case of GaAs and Ge material systems.

We note that air voids are occasionally formed during lateral overgrowth on graphene or SiO_2 masks, as shown in the cross-sectional STEM images in Figs. 2b and 3f,h and Supplementary Figs. 19 and 20. This phenomenon is well understood in the epitaxial lateral overgrowth of III–V materials[28–31], and the formation of voids can be controlled or eliminated by tuning the mask geometry or growth conditions[29,30,32]. When laterally grown layers are merged, threading dislocations may be generated at the coalescence boundaries[32,33], which is also observed in our EPG approach (Supplementary Fig. 19). Although such threading dislocations initiated at the coalescence boundaries adversely affect the crystal quality of epilayers, we emphasize here that the overall crystal quality is improved by the EPG technique due to the roles of graphene revealed above.

The impact of the EPG technique on highly mismatched systems is studied by growing InAs on GaAs substrates, exhibiting 7.2% lattice mismatch, with graphene patterns having various pitches and opening widths. As shown in the electron-channelling contrast images (ECCI) of InAs epilayers of the same thicknesses of 1 μm (Fig. 4a and Supplementary Fig. 21), the dislocation density progressively reduces on the surface as the graphene coverage increases. The monotonic decrease in dislocation density is

observed by plotting the density as a function of graphene coverage from 0% to 92%. This proves that the impact of graphene coverage is substantial as it shows an order of magnitude reduction in dislocations by simply varying the coverage (Fig. 4b). MD simulations also predict a reduction in dislocations and stacking faults by increased graphene coverage (Fig. 4c and Supplementary Fig. 22), in agreement with experimental results. It should be highlighted that this technique provides unique solutions for obtaining heteroepitaxial films with significantly reduced dislocation densities that can be mechanically released from the substrate.

In conclusion, we demonstrate graphene nanopatterns as a universal platform for the epitaxy of single-crystal films, where both elemental and compound semiconductors can be used for the substrates as well as epilayers. The three modes of peeling—spalling, exfoliation and delamination—are theoretically proposed and experimentally demonstrated, proving that the grown films can be readily exfoliated with good controllability regardless of film thickness due to the weak interfaces intentionally formed by graphene stripes. Moreover, APBs completely disappear when III–V films are grown on elemental substrates with graphene stripes, resulting in high-quality III–V optoelectronic devices that can be made freestanding and transferred onto foreign platforms for heterointegration. Our theoretical analysis of dislocation reduction by the dangling-bond-free and ultrathin graphene in lattice-mismatched heteroepitaxy supports the experimental results. Overall, we provide a new pathway for the production of various high-quality and single-crystal membranes, overcoming polarity and lattice-matching constraints that have been a critical obstacle for heterointegrated multifunctional systems.

Online content

Any methods, additional references, Nature Research reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41565-022-01200-6.

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Methods

Graphene formation. For Ge substrates, graphene is directly grown on Ge(100) by chemical vapour deposition (CVD) (TCVD-50B, Graphene Square) at atmospheric pressure. Ge(100) wafers are first cleaned in a diluted HCl solution (10% HCl in water) for 3 min, followed by water rinsing and nitrogen blow-drying. After loading the Ge substrates into the CVD system, the CVD tube is first purged with Ar for 30 min at room temperature, followed by ramping the temperature up to 910 °C that takes 30 min. At 910 °C, graphene is grown by flowing H_2 at 730 s.c.c.m. and CH_4 at 200 s.c.c.m. for 60 min. After the growth, the tube is cooled down to room temperature by flowing Ar at 140 s.c.c.m. The graphene thickness obtained is between monolayer and bilayer.

For III–V substrates, graphene is first formed on a copper foil by CVD, followed by a standard wet-transfer process to transfer graphene onto the III–V substrate. Details on graphene growth and transfer can be found elsewhere[18]. GaAs substrates are deoxidized by diluted HCl and InP substrates by 5:1 buffered oxide etchant (J.T.Baker), and both are cleaned with water right before scooping the graphene. Because the remote epitaxy of III–V requires dry-transferred graphene and does not work on wet-transferred graphene due to interfacial oxidation, employing wet-transferred graphene in this study ensures that the growth of single-crystalline membranes is the result of purely lateral overgrowth, not by a mixed growth mode with a portion of remote epitaxy[34].

Graphene patterning. After graphene formation, graphene is patterned at the nanoscale by various types of lithographic method, including electron-beam lithography, interference lithography and stepper lithography. The electron-beam lithography technique is mainly used to study epitaxial film growth and exfoliation behaviour depending on the pattern geometries. A 200-nm-thick polymethyl methacrylate resist layer is spin coated on graphene and baked at 180 °C for 2 min, followed by exposure using an Elionix ELS-F125 electron-beam lithography system. The exposed samples are then developed in methyl isobutyl ketone:isopropanol = 1:3 for 60 s and washed out in pure isopropanol. The developed polymethyl methacrylate patterns are transferred to graphene by reactive ion etching via Plasma-Therm 790 with O_2 (20 s, 6 mtorr, 90 W), followed by rinsing the overlying polymethyl methacrylate layer in acetone to finish the graphene-patterning process. For large-area thin-film growths and LED device fabrication, interference lithography or stepper lithography is employed to produce millimetre- to centimetre-scale patterns. Nanoscale gratings are interferometrically or photolithographically patterned utilizing the interference pattern of 325 nm HeCd laser generated by a Lloyd's-mirror-based interference lithography system or exposing to a GCA AS200 i-line stepper, respectively. For both processes, a 100-nm-thick positive photoresist (Futurrex PR1-100A1) is first spin coated on graphene and baked at 120 °C for 2 min. After exposure, the samples are developed in Futurrex RD6 diluted at 3:1 with deionized water for 15 s and rinsed in pure deionized water. The rest of the process is the same as electron-beam lithography.

Epitaxy. Ge, GaAs and InAs epitaxy are conducted in a close-coupled showerhead metal–organic chemical vapour deposition reactor using arsine, trimethylgallium, trimethylaluminum, trimethylindium and germane as the sources of As, Ga, Al, In and Ge, respectively. Disilane and dimethylzinc are used as Si and Zn dopants, respectively. The reactor pressure is maintained at 100 torr during the growth, and nitrogen is used as a carrier gas. Ge growth is conducted at 650 °C at a growth rate of ~30 nm min^{-1}. GaAs growth is conducted at 650 °C at a growth rate of ~33 nm min^{-1} and a V/III flow rate ratio of ~45. InAs growth is conducted at 650 °C at a growth rate of ~23 nm min^{-1} and a V/III flow rate ratio of ~65. For the growth on GaAs and InP substrates, arsine and phosphine are respectively flown during the temperature ramp up from 300 °C to the growth temperature to prevent substrate desorption before the growth. Similarly, after the growth of GaAs and InAs films, arsine is flown during the temperature ramp down to 300 °C. For the growth of red LED structures, a 2-μm-thick GaAs buffer is first grown at 650 °C, followed by a 700-nm-thick p-GaAs bottom contact layer, 350-nm-thick p-$Al_{0.65}Ga_{0.35}As$ barrier, 300-nm-thick $Al_{0.35}Ga_{0.65}As$ emitter, 350-nm-thick n-$Al_{0.65}Ga_{0.35}As$ barrier and 100-nm-thick n-GaAs top contact layer at 700 °C. Although p-GaAs is more commonly used as the top contact layer, we employed n-GaAs as a thin top contact layer and p-GaAs as a thick bottom contact layer, because we did not employ an additional current-spreading scheme and both holes and electrons are laterally injected.

Two-dimensional material-based layer transfer and device fabrication. The grown films are exfoliated by first depositing a 30-nm-thick Ti adhesion layer by electron-beam evaporation, with a deposition rate of ~0.1 nm s^{-1}. Next, a Ni stressor layer is deposited by direct-current (d.c.) sputtering in the same chamber with a d.c. power of 500 W and constant Ar flow of 6 s.c.c.m. The stress level of Ni is controlled by the chamber pressure during sputtering, which typically ranged around 1.1–1.8 mtorr, with a higher pressure resulting in a higher stress level. After the deposition of metal, a thermally releasable tape (TRT; Revalpha; release temperature, ~150 °C; Semiconductor Equipment) is attached to the metal by gently rubbing with a cotton swab. The tape edge is then lifted up by holding with a tweezer, which initiates cracks from the sample edge. The cracks propagate as the tape is further lifted up, and mechanical exfoliation finishes when the entire TRT/stressor/epilayer stack is detached from the substrate.

The exfoliated AlGaAs LED layer on TRT is transferred on a Si wafer by treating with oxygen plasma (Anatech Barrel Plasma System), spin coating 1 vol% aqueous solution of (3-aminopropyl)triethoxysilane (Sigma-Aldrich) at a speed of 3,000 rpm for 30 s, and baking at 110 °C for 1 min on both LED and receiver substrate surfaces. The substrate is subsequently spin coated with a polyimide precursor (PI-2545; HD Microsystems) at a speed of 3,000 rpm for 30 s, baked at 110 °C for 30 s, bonded with the LED film on TRT and pressed in a steel vise (Toolmaker's vise, Tormach), and further baked at 180 °C for 10 min before TRT is removed. Final curing in a 250 °C convection oven completed the transfer process. Wet etching in $FeCl_3$ solution (MG Chemicals) and 5:1 buffered oxide etchant removed the Ti/Ni layers.

LED mesa structures are fabricated by photolithography and reactive ion etching (PlasmaPro 100 Cobra 300 System, Oxford Instruments) in Cl_2 gas. Both top and bottom metal contact pads are formed by photolithography, electron-beam evaporation of Cr/Au (~15/100 nm) and metal lift-off.

Characterizations. Cross-sectional STEM specimens were prepared with conventional focused-ion-beam lift-out technique using Helios NanoLab 600. Argon-ion milling under 900 and 500 eV was used to clean the surface amorphous layer and minimize subsurface damage. STEM images were collected using a probe-aberration-corrected Thermo Fisher Scientific Themis Z STEM operated at 300 kV and a convergence semi-angle of 20 mrad. Strain mapping of the film with respect to the substrate was conducted using GPA[35] based on atomic-resolution images.

Atomic force microscopy (AFM) measurements were conducted using an AFM probe with a silicon tip (PPP-NCHR, Nanosensors) in the non-contact mode (Park NX10, Park Systems).

SEM and EBSD characterizations were conducted using a Zeiss Merlin high-resolution SEM system. SEM images were measured using a beam acceleration voltage of 3 kV and current of 0.1 nA, and the EBSD maps were measured using an EBSD detector with a beam acceleration voltage of 15 kV and current of 3 nA.

Raman and EL spectra were measured using a Renishaw Invia Reflex Micro Raman system with a charge-coupled device detector, and the current–voltage (I–V) characteristics were measured using a Signatone probe station equipped with a semiconductor parameter analyser (Agilent 4156C, Keysight Technologies) and a camera system connected with an optical microscope for collecting the images.

MD simulations. MD simulations were carried out via the Large-scale Atomic/Molecular Massively Parallel Simulator (LAMMPS)[36,37] package with the equations of motion integrated using the velocity Verlet algorithm under a time step of 1 fs. To mimic the behaviour of Ge–Si systems, Stillinger–Weber potential parameterized elsewhere[38] was employed. The interaction of carbon atoms within a graphene layer is also described by the Stillinger–Weber potential, which has been parameterized elsewhere[39]. The interaction between graphene and Si–Ge is a hard sphere only for simplicity since the weak van der Waals attraction is negligible at high temperatures. For convenience, the C–Si and C–Ge interactions are also modelled using the Stillinger–Weber formulation with only the two-body term (effectively a tailed Lennard–Jones 12-6 potential) with the following identical parameters: $\varepsilon = 0.04$ eV, $\sigma = 0.35$ nm, $p = 12$, $q = 6$, $a = 1.12$, $A = 1$ and $B = 1$. Our MD simulations consist of a 1.2-nm-thick Si(100) substrate with cross-sectional dimensions of 20.2 (x) × 6.0 (y) nm^2. To mimic the rigid SiO_2 mask, multiple layers of graphene are introduced without permitting the carbon atoms to move. The simulation box in the z direction is 43.6 nm. The lattice constant of Si was chosen to be 0.545 nm (lattice constant at the growth temperature used here). The bottom layer of the Si substrate was fixed. The growth temperature was set to 2,100 K to facilitate the formation of the diamond cubic structure under the extremely high deposition rate, which is typical for MD simulations. A lower growth temperature leads to amorphous Ge film formation. Si and Ge crystals are stable under this temperature (as shown in Supplementary Videos 1–3), which is attributed to the deficiency of the potential used here[38]. The temperature is controlled using a Nose–Hoover thermostat[40]. We note that the Ge/Si/C system instead of the experimentally employed In/As/P/C system can eliminate the complexity such as non-stoichiometry, and still effectively represent the lattice-mismatched epitaxy environments with graphene nanopatterns. To model the flexible graphene mask, there is an external force of 0.015 eV $Å^{-1}$ applied on each carbon atom (excluding about 1 nm width on both edges) towards the Si substrate to prevent the graphene mask from leaving the substrate. Ge atoms are randomly introduced at the top of the simulation box periodically with a downward velocity. For all the MD simulations presented here, the growth rates are identical, which is roughly 0.1 nm ns^{-1}. Periodic boundary conditions were applied in all the three directions of the simulation box. Therefore, both flexible mask and rigid mask represent infinitely long stripes with equal spacing on the silicon substrate. A wall was imposed on top of the simulation box to prevent atoms from depositing to the backside of the substrate. The interaction is a Lennard–Jones 9-3 potential ($\varepsilon = 0.01$ eV, $\sigma = 0.10$ nm, $\sigma_{cutoff} = 0.25$ nm). The OVITO visualization software[41] was used to generate the simulation snapshots.

Data availability

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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Author contributions

J.K. and S.-H.B. conceived the idea. H.K., S.L. and J.S. designed and coordinated the experiments. M.A., Y.Z. and Y.S. conducted the theoretical studies and simulations of epitaxy. Epitaxial growth was performed by H.K., K. Lu and Y.B. Graphene growth and transfer were performed by H.K., S.L., K. Lu, N.M.H., K.S.K., H.S., H.S.K., S.-I.K., J.-H.L. and J.-H.A. Patterning, exfoliation and device fabrication were performed by S.L., J.S., H.K., K. Lu, B.-I.P., C.C., H.Y., Y.M. and S.S. Exfoliation theory is developed by H.K., S.L., N.M.H., K. Lee, S.-H.B. and J.K. STEM measurements and GPA analysis were conducted by M.Z. and J.H. Material characterizations were conducted by H.K., S.L., N.M.H., K. Lu, C.S.C., J.M.S., H.Y., Y.M. and S.S. Optoelectronic characterizations were conducted by H.K. and J.S. The manuscript was written by H.K., Y.S. and J.K. with input from all the authors. All the authors contributed to the analysis and discussion of the results leading to the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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