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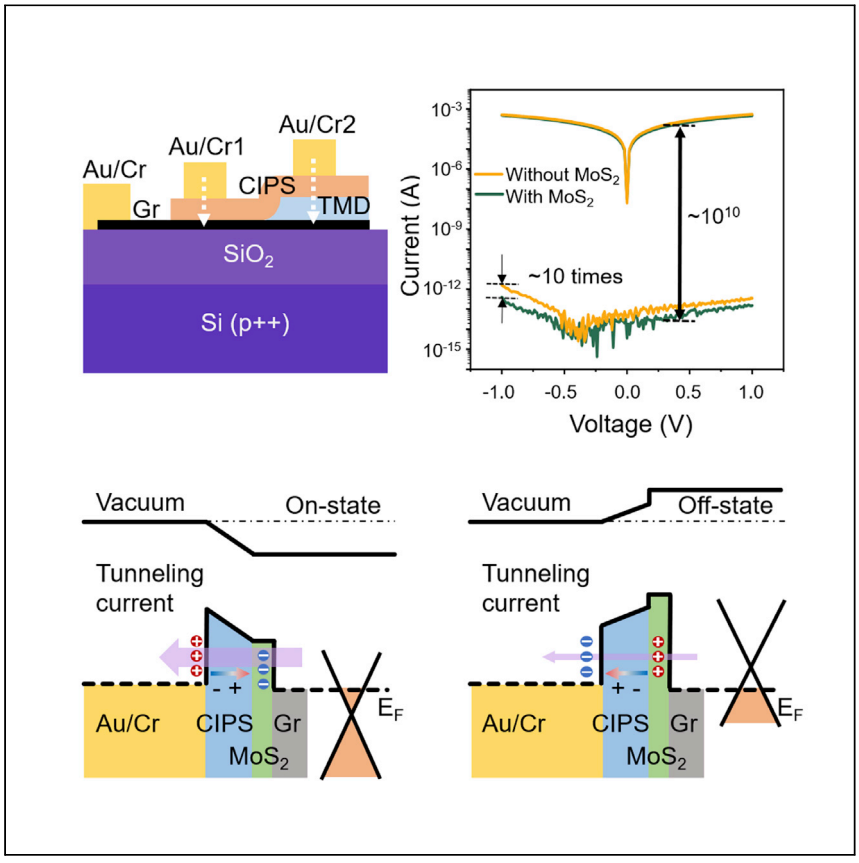
Extraordinary tunnel electroresistance in layer-by-layer engineered van der Waals ferroelectric tunnel junctions



Conventional ferroelectric tunnel junctions (FTJs) comprising metal/oxide heterostructures suffer from a relatively low tunneling electroresistance (TER; usually $<10^6$) due to the unavoidable defect states and interfacial states. Here, we constructed van der Waals FTJs consisting of 2D ferroelectrics $CuInP_2S_6$ and 2D electronic materials (e.g., graphene and MoS_2) and demonstrated a record-high TER of $>10^{10}$ at room temperature. We also demonstrated an unprecedented layer-by-layer engineering of giant TER, largely strengthening the ability to manipulate electrons' tunneling behaviors for advanced tunneling devices.

Benchmark
First qualification/assessment of material properties and/or performance

Qinqin Wang, Ti Xie, Nicholas A. Blumenschein, ..., Jian-Ping Wang, Adam L. Friedman, Cheng Gong

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Highlights

Demonstrated van der Waals (vdW) ferroelectric tunnel junctions (FTJs)

Achieved layer-by-layer engineering of tunneling electroresistance (TER) of $>10^{10}$

Enhanced TER by 10× via adding monolayer MoS_2 or WSe_2 into Cr/$CuInP_2S_6$/graphene FTJs

Demonstrated the gate tunability of the on-state tunneling current in vdW FTJs

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Extraordinary tunnel electroresistance in layer-by-layer engineered van der Waals ferroelectric tunnel junctions

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SUMMARY

The ability to engineer potential profiles of multilayered materials is critical for designing high-performance tunneling devices such as ferroelectric tunnel junctions (FTJs). FTJs comprise asymmetric electrodes and a ferroelectric spacer, promising semiconductor-platform-compatible logic and memory devices. However, traditional FTJs consist of metal/oxide/metal multilayered structures with unavoidable defects and interfacial trap states, which often cause compromised tunneling electroresistance (TER). Here, we constructed van der Waals (vdW) FTJs by a layered ferroelectric $CuInP_2S_6$ (CIPS) and graphene. Owing to the gigantic ferroelectric modulation of the chemical potentials in graphene by as large as ~1 eV, we demonstrated a giant TER of 10^9. While inserting just a monolayer MoS_2 between CIPS/graphene, the off state is further suppressed, leading to $>10^{10}$ TER. Our discovery opens a new solid-state paradigm where potential profiles can be unprecedentedly engineered in a layer-by-layer fashion, fundamentally strengthening the ability to manipulate electrons' tunneling behaviors and design advanced tunneling devices.

INTRODUCTION

Among all the bizarre phenomena governed by quantum mechanics, the tunneling behavior is clearly beyond any classical theory's comprehension when it comes to the penetration of matter waves and the transmission of particles through a high potential barrier—that is, the classically forbidden region.[1–3] Fundamentally differing from diffusive transport, electrons' quantum tunneling through the classically forbidden region leads to a wide spectrum of remarkable phenomena such as Klein tunneling and pivotal devices such as magnetic and ferroelectric tunnel junctions. Quantum tunneling efficiency sensitively depends on the details of the potential barriers including heights and widths.[4,5] Given such a dependence is an exponential function, the tunneling can be turned on and off with stark contrast, thereby leading to the development of a broad range of important devices such as nonvolatile memories and steep-slope tunneling field-effect transistors.[6–9]

When ferroelectric layers are implemented between a pair of asymmetric electrodes, the tunneling transmission can be toggled with ferroelectric polarizations because the relative potential files are altered by the opposite electric dipoles, leading to a

PROGRESS AND POTENTIAL

Ferroelectric tunnel junctions (FTJs) promise electrically switchable memories, sensors, and logic devices. However, traditional FTJs comprising metal/oxide heterostructures only exhibit modest tunneling electroresistance (TER; usually $<10^6$), which is limited by defect states and interface trap states. Here, we demonstrated an emerging class of FTJs by employing 2D van der Waals (vdW) ferroelectrics and 2D electronic materials (e.g., graphene and MoS_2). A giant TER of $>10^{10}$ is achieved due to the gigantic ferroelectric modulation of band alignments of vdW stacks. In our FTJ multilayered structures, inserting a monolayer MoS_2 or WSe_2 in between ferroelectrics/graphene effectively enhances TER by ten times. Our discovery of the giant TER in vdW FTJs opens up a new solid-state paradigm in which electrons' potential profiles can be tailored in an unprecedented layer-by-layer fashion, enhancing the ability to control electrons' tunneling behaviors for emerging tunneling devices.

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tunneling resistance contrast defined as tunneling electroresistance (TER) of a ferroelectric tunnel junction (FTJ).[6,10–12] However, in practical multilayered material systems such as metal-oxide-metal trilayer structures, defect states and interfacial trap states are inevitable, sometimes entangled with metal-induced gap states[13] and the associated Fermi-level pinning. The defect states complicate the intermediate tunneling channels and thus tend to deteriorate the TER, and Fermi-level pinning sets roadblocks for the efficient ferroelectric alternation of the relative potential profiles, suppressing the TER.[14–16]

The recently emerged two-dimensional (2D) layered van der Waals (vdW) materials, and in particular the vdW ferroelectrics (e.g., $CuInP_2S_6$ [CIPS] and In_2Se_3),[17,18] promise a giant TER owing to the negligible defects, absence of interfacial states in vdW heterojunctions, and the easy tunability of the chemical potentials of 2D materials.[19–24] The high crystallinity of 2D vdW materials retains at the atomic level and even at the wafer scale, which holds unprecedented prospects for next-generation high-performance, energy-efficient FTJs considering that the ultrathin, defect-free ferroelectrics can allow low-voltage writing operations. Here, we constructed the vdW heterostructure-based FTJs primarily consisting of 2D ferroelectric CIPS and 2D electronic materials (i.e., graphene, MoS_2, and WSe_2) and demonstrated a record-high TER of $>10^{10}$ at room temperature. This giant TER arises from the gigantic ferroelectric modulation of the tunneling barrier height and the band positions of 2D electronic materials. Remarkably, we achieved an order-of-magnitude-enhanced TER in Cr/CIPS/graphene (CrCG) tunnel junctions by simply adding a monolayer MoS_2 or WSe_2 in between CIPS and graphene. Our discovery of the giant TER in vdW FTJs and the demonstration of the effectiveness of the layer-by-layer engineering of FTJs open the door to an emerging class of vdW heterostructures for studying fundamental tunneling physics and exploring tunneling devices such as nonvolatile memories, logics, and logic-in-memory technologies.

RESULTS AND DISCUSSION

Device structures and band diagrams for CrCG FTJs

Figures 1A and 1B illustrate the Au/Cr/CIPS/graphene multilayer stack of FTJ with CIPS polarized oppositely. Under opposite polarizations, the positions of Cu^+ ions (red balls) differ in vertical positions: for the on state, Cu^+ ions are pushed by the positive electric field toward the CIPS/graphene interface, and for the off state, Cu^+ ions are dragged away from the CIPS/graphene interface. Figure 1C shows a representative optical image of the core heterostructure of CIPS/graphene fabricated by mechanical exfoliation and dry-transfer process. The thin graphene flake is covered by a CIPS flake with two regions of different thicknesses. Specifically, Figure 1F shows the Raman spectra of the exfoliated CIPS and graphene thin flakes, measured by an excitation laser of 532 nm wavelength at room temperature. The intensities of the 2D band (2,685 cm^{-1}) and the G band (1,580 cm^{-1}) of the graphene flake are comparable, suggesting that the graphene consists of two atomic layers.[25] As for CIPS, the vibration of anion ($P_2S_6^{4-}$) corresponds to the peak at ~100 cm^{-1}, and the S-P-S vibration corresponds to the peak at 262 cm^{-1}.[26] Cu^+ ions and P-P stretching are responsible for the peaks located at 316 and 373 cm^{-1}, respectively.[26–28] These well-defined Raman peaks agree with the previous work on high-quality CIPS crystals, indicating the high crystalline quality of our CIPS flake with low defect density, which is critical for achieving a very large TER. The thickness of the CIPS flake of the thinner region in Figure 1C is ~3.5 nm, as estimated by optical contrast first and confirmed by atomic force microscopy (AFM) measurement (Figure S1).

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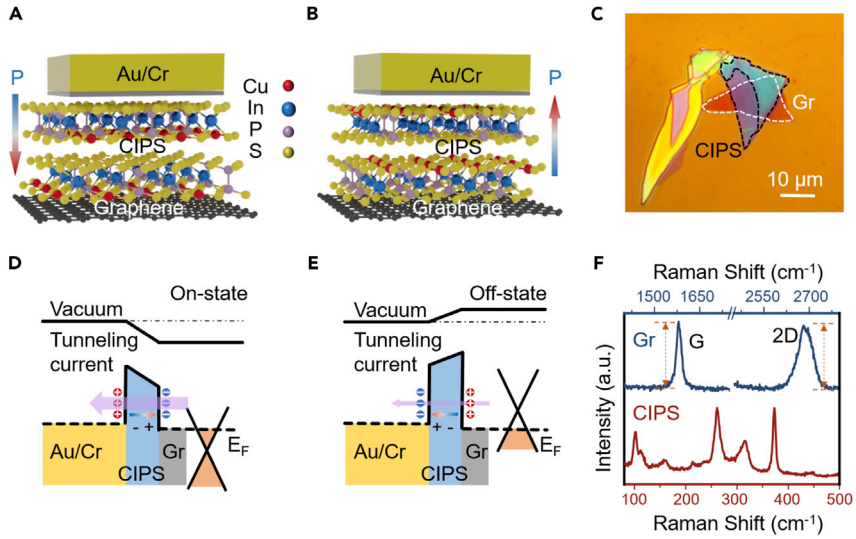

Figure 1. The device structures and band diagrams for the on state and off state of the CrCG tunneling device

(A) Schematic of the CrCG tunneling device in on state.

(B) Schematic of the CrCG tunneling device in off state. The built-in polarization fields in the CIPS are indicated by the blue-to-red arrows.

(C) Optical image of the fabricated CIPS/graphene heterostructure on a 260-nm-thick SiO_2/Si chip. The thin graphene and CIPS flakes are circled by white and black dashed lines, respectively. Scale bar, 10 μm.

(D) Band diagram for the on-state FTJ.

(E) Band diagram for the off-state FTJ. The built-in polarization fields in the CIPS are indicated by the blue-to-red arrows, and the tunneling currents are indicated by the purple arrows.

(F) Corresponding Raman spectra of graphene (blue) and CIPS (red) of the heterostructure shown in (C), indicating the high crystalline quality of these vdW flakes. The comparable peak intensities of the 2D and G peaks in graphene suggest it is a bilayer graphene.[25] The CIPS thickness is estimated to be 3.5 nm by atomic force microscopy (AFM) measurement, as shown in Figure S1. The thinness of the CIPS flake agrees with its shallow optical contrast[6] and sizable on-state tunneling current.

The ferroelectric polarization with built-in electric field can cause the effective modulation of the energy levels in graphene and the height of the tunneling barrier. Specifically, the positive polarization (pointing through CIPS toward the CIPS/graphene interface) causes the lowering of energy levels in both CIPS and graphene along the CIPS-graphene direction, as illustrated in Figure 1D. Conversely, the negative polarization gradually lifts up the energy levels of CIPS and graphene along the CIPS-graphene direction, as illustrated by Figure 1E. There is a fundamental difference between the vdW heterostructure and the oxide/metal heterostructures in traditional FTJs. It has been well known that the metal/insulator heterojunctions easily produce mid-gap states due to the evanescent wavefunction of metals decaying into the insulators, which produces the gap states that potentially pin the Fermi level.[13] The mid-gap states themselves complicate the tunneling channels that often cause the compromised TER, and Fermi-level pinning largely undermines the effectiveness of the ferroelectric modulation of the band alignments across the stacks. In stark contrast, CIPS/graphene heterojunctions are free from defects and Fermi-level pinning and can thus allow the effective ferroelectric modulation of chemical potentials in graphene by as large as ~1 eV (see density functional theory [DFT] calculation results in Note S1 and Figures S2 and S3)[6] and thus the effective ferroelectric toggling between two contrasting band alignments (Figures 1D and 1E), potentially leading to a giant TER.

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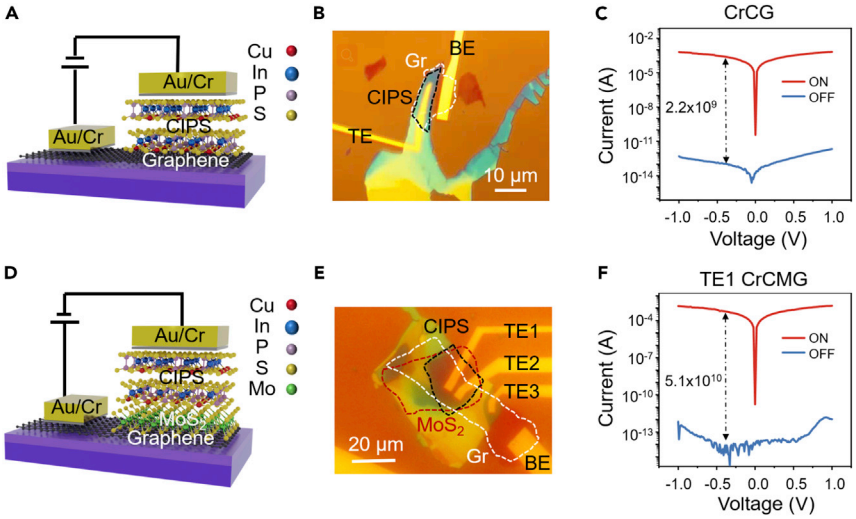

Figure 2. The device structures and current-voltage characteristics of the CrCG and CrCMG tunneling devices

(A) Schematic of the CrCG tunneling device. The ultrathin CIPS flake serves as the tunneling layer here.

(B) Optical image of a CrCG tunneling device with a top electrode (TE) and bottom electrode (BE). Areas of graphene and CIPS are circled by white and black dashed lines, respectively. Scale bar, 10 μm.

(C) Current-voltage characteristics of the on (red) and off (blue) states of the CrCG tunneling device. TER is measured using −0.4 V reading voltage.

(D) Schematic of the CrCMG tunneling device.

(E) Optical image of the CrCMG tunneling device, showing three subdevices with three different TEs, TE1 (CrCMG), TE2 (CrCMG), and TE3 (CrCG), sharing the common BE. Areas of graphene, MoS_2, and CIPS are circled by white, red, and black dashed lines, respectively. Scale bar, 20 μm.

(F) Current-voltage characteristics of the CrCMG tunneling device with TE1. TER is measured using −0.4 V reading voltage.

Device structures and electrical characteristics of CrCG and Cr/CIPS/MoS_2/graphene (CrCMG) FTJs

We fabricated and electrically characterized CrCG tunneling devices. Figure 2A is the schematic of the CrCG tunneling device structure, where a thin CIPS flake serves as the tunneling layer and the bottom and top electrodes are graphene and Cr, respectively. Figure 2B shows a representative optical image of the CrCG tunneling device. As discussed in detail later, we apply a pulse voltage to flip the ferroelectric polarization. After the writing operation, we sweep the voltage and measure the tunneling current. Both on- and off-state current-voltage characteristics displayed in Figure 2C have typical tunneling features with a slight asymmetry between positive and negative bias voltages, which is caused by the asymmetric device structure (i.e., top and bottom electrodes adopt different metals). Under the −0.4 V reading voltage, the on-state current and off-state current of this device are 2.5×10^{-4} and 1.1×10^{-13} A, respectively, leading to a gigantic on/off ratio of 2.2×10^{9}, which is three orders of magnitude higher than the maximum TER reported in conventional FTJs (primarily using oxide ferroelectrics).[6,29,30] To the best of our knowledge, this is the record-high TER in FTJs at room temperature reported to date.

The vdW heterojunctions not only provide unique platforms that could enable a giant TER but also open up unprecedented opportunities to engineer band alignment in a layer-by-layer fashion. Here, we inserted monolayer transition metal

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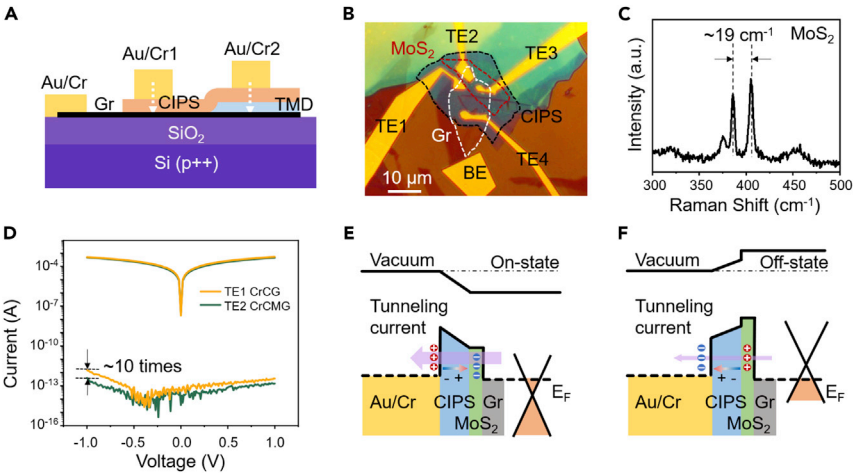

Figure 3. Layer engineering of the TER in CrCG tunneling device by inserting a monolayer MoS_2 in between CIPS/graphene

(A) Schematic of the device structure. Au/Cr1 and Au/Cr2 refer to TE1 (CrCG) and TE2 (CrCMG) in the optical image in (B).

(B) Optical image of the CrCG and CrCMG tunnel junctions. There is a monolayer MoS_2 flake under the TEs labeled with TE2 and TE3, while the graphene directly contacts the top CIPS under the TEs labeled with TE1 and TE4. Graphene, MoS_2, and CIPS are circled by white, red, and black dashed lines, respectively. Scale bar, 10 μm.

(C) Raman spectrum of the MoS_2 in the device shown in (B). The distance between two peaks is ~19 cm^{-1}, demonstrating that the MoS_2 flake is monolayer.[31,32]

(D) Current-voltage characteristics of the CrCG and CrCMG tunnel junctions. The largest difference between the two off-state currents is around 10 times.

(E) Band diagram for the CrCMG tunnel junction in on state.

(F) Band diagram of the CrCMG tunnel junction in off state. In (E) and (F), the built-in polarization fields in the CIPS are indicated by the blue-to-red arrows, and the tunneling currents are indicated by the purple arrows. The difference between the vacuum levels of MoS_2 and graphene is not the focus and thus is not specified in the illustrations in (E) and (F).

dichalcogenides (TMDs) in these tunnel junctions to further tune the band alignments. Figure 2D shows the schematic of the CrCMG tunneling device, and Figure 2E shows the optical image of a fabricated CrCMG device. Remarkably, in the CrCMG device, we observed an even higher TER of 5.1×10^{10} (Figure 2F). This device exhibits a very low off-state current of 1.1×10^{-14} A, while it can reach a 5.6×10^{-4} A on-state current, measured by the reading voltage of −0.4 V. Compared with the CrCG results shown in Figure 2C, it appears that the monolayer MoS_2 promotes the tunneling device with one-order-of-magnitude-higher TER.

Layer engineering of the TER in vdW FTJs

The giant TER of $>10^{10}$ achieved in CrCMG tunnel junctions is remarkable not only because of the giant TER itself but also because it indicates a promising prospect of layer-by-layer engineering of the band alignments and thus the resultant fine design and engineering of TER. To confirm that our experimentally observed one-order-of-magnitude enhancement in the CrCMG device with respect to the CrCG device is not because of sample variance but indeed is caused by the presence of the monolayer MoS_2, we designed the control experiments based on two directly comparative devices, between which the only difference is the monolayer MoS_2. As shown in Figure 3A, the CrCG and CrCMG devices share the same graphene flake and the same uniform CIPS flake (see Figure S4 for details of the fabrication process). By doing so, the thickness of graphene (and also CIPS) in these two types of devices is identical. Figure 3B presents the optical image of the fabricated devices. There are four

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devices on this chip, sharing the same bottom electrode labeled as BE, and there is a monolayer MoS_2 flake under the top electrodes labeled with top electrode 2 (TE2) and TE3 while the graphene directly contacts the top CIPS under the TEs labeled with TE1 and TE4. As shown in Figure 3C, the Raman E_{2g} and A_{1g} peaks of MoS_2 are located at 385 and 404 cm^{-1}, respectively, with the peak frequency separation 19 cm^{-1}, confirming it is a monolayer MoS_2.[31,32]

Figure 3D shows the current-voltage characteristics of the CrCG and CrCMG tunnel junctions. The on-state currents of these two devices are similar, while the CrCMG tunnel junction exhibits a one-order-of-magnitude-lower off-state current than the CrCG tunnel junction, which causes a higher TER in the CrCMG tunnel junction. Band diagrams of the on and off states of the CrCMG tunnel junction are shown schematically in Figures 3E and 3F (see Note S2 and Figures S5–S7 for additional details), based on the calculated band alignment of CIPS/MoS_2 by DFT. As shown in Figure 3E, for the on state, the conduction band minimum (CBM) of MoS_2 is close to the CBM of CIPS. The positive polarization in the on state tends to n-type dope MoS_2. Given that freshly exfoliated MoS_2 typically exhibits n-type behavior, the positive polarization will keep MoS_2 n-type doped. Therefore, in this on state, the monolayer MoS_2 serves as a thin conductive material in this structure and will not have obvious effects on the on-state tunneling currents. In stark contrast, for the off state, the CBM of MoS_2 is lifted higher than the CBM of CIPS. In other words, the negative polarization tends to deplete the originally n-type doped MoS_2, making it more intrinsic (i.e., more insulating). In this scenario, the MoS_2 serves as an insulating layer to effectively increase the width of the barrier. The band diagram in Figure 3F implies that the presence of MoS_2 with higher CBM than the CBM of CIPS increases the tunneling barrier height as well. Thus, in the off state, the monolayer MoS_2 will effectively block the electron tunneling, leading to the further suppressed off-state current.

The effective suppression of the off-state current by one order of magnitude through adding a monolayer MoS_2 highlights the effective strategy of layer-by-layer engineering of the potential profiles in the tunneling pathway. As an important control experiment, we decide to insert a monolayer WSe_2 in the CrCG device. The reason for choosing WSe_2 is because of its contrasting property from MoS_2: the as-exfoliated MoS_2 is typically n-type doped, while the as-exfoliated WSe_2 is typically p-type doped. The p-type doped WSe_2 has a large work function, and its valence band can directly serve to receive the electrons that tunnel through CIPS. In other words, WSe_2 in the p-type doping region can serve as the conductive electrode to receive the tunneling electrons. Note that the relatively flat band of the covalently bonded semiconductor WSe_2 has a much larger density of states than graphene, thereby potentially allowing a higher tunneling transmission than graphene.

To confirm this scenario, we fabricated the devices in a directly comparative manner. Figure 4A shows the optical image of the Cr/CIPS/WSe_2/graphene (CrCWG) tunneling device, in which the regions surrounded by the blue and white dashed lines represent the monolayer WSe_2 and the few-layer graphene underneath, respectively. Device 1 under TE1 is the CrCWG structure, while device 2 under TE2 is the CrCG structure. Again, between these two devices, the only difference is the presence and the absence of the monolayer WSe_2. Figure 4B shows the well-defined Raman peaks of WSe_2 (e.g., the E_{2g} mode of WSe_2 at 244 cm^{-1}), and the strong photoluminescence peak at the energy ~1.66 eV demonstrates the monolayer nature of the WSe_2 flake.[33,34]

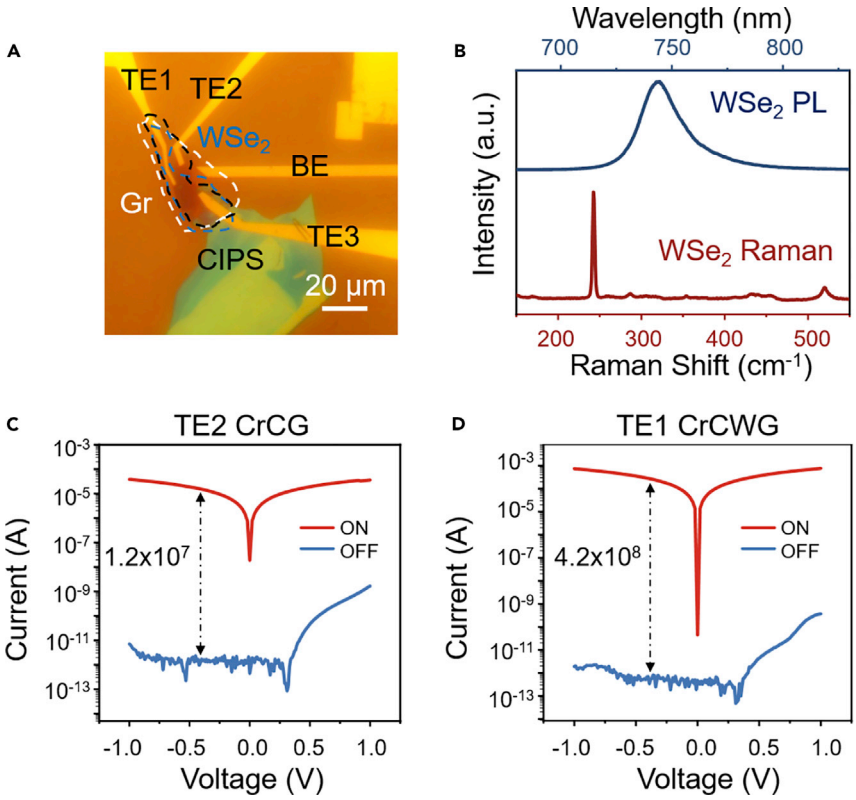

Figure 4. Layer engineering of the TER in CrCG tunneling device by inserting a monolayer WSe_2 in between CIPS/graphene

(A) Optical image of the CrCWG tunneling device. There is a monolayer WSe_2 flake under the TEs labeled with TE1 and TE3, while the graphene directly contacts the top CIPS under the TE labeled with TE2. Graphene, WSe_2, and CIPS are circled by white, blue, and black dashed lines, respectively. Scale bar, 20 μm.

(B) Raman and photoluminescence (PL) spectra of the monolayer WSe_2.

(C) Current-voltage characteristics of the CrCG tunneling device with TE2, showing an on/off ratio of 1.2×10^7 at −0.4 V reading voltage.

(D) Current-voltage characteristics of the CrCWG tunneling device with TE1, showing an on/off ratio of 4.2×10^8 at −0.4 V reading voltage.

Indeed, we experimentally observed the one-order-of-magnitude-enhanced TER with the one-order-of-magnitude-enhanced on-state current in the CrCWG device with respect to the CrCG device. Figure 4C shows the current-voltage characteristics of the CrCG tunneling structure with TE2, exhibiting a low off-state current of 1.2×10^{-12} A and a high on-state current of 1.5×10^{-5} A with a reading voltage of −0.4 V, leading to the TER of 1.2×10^7. In the device with TE1, which has an additional WSe_2 layer in the structure, using the same reading voltage with the TE1 device, the off-state current can be as low as 6.7×10^{-13} A, and the on-state current can reach 2.8×10^{-4} A, an order of magnitude higher than the on-state current of the CrCG device (Figure 4D). Thus, a higher TER of 4.2×10^8 is achieved with respect to the TER of 1.2×10^7 in the CrCG device. These results clearly show that the insertion of monolayer TMDs can enhance the TER effectively. Interestingly, as discussed, the inserted MoS_2 enhances the TER primarily by suppressing the off-state current, while the inserted WSe_2 enhances the TER primarily by enhancing the on-state current. Such layer-by-layer engineering of the potential profiles opens up the new avenues to study the fundamental tunneling physics and explore novel tunneling devices for memories and logic applications.

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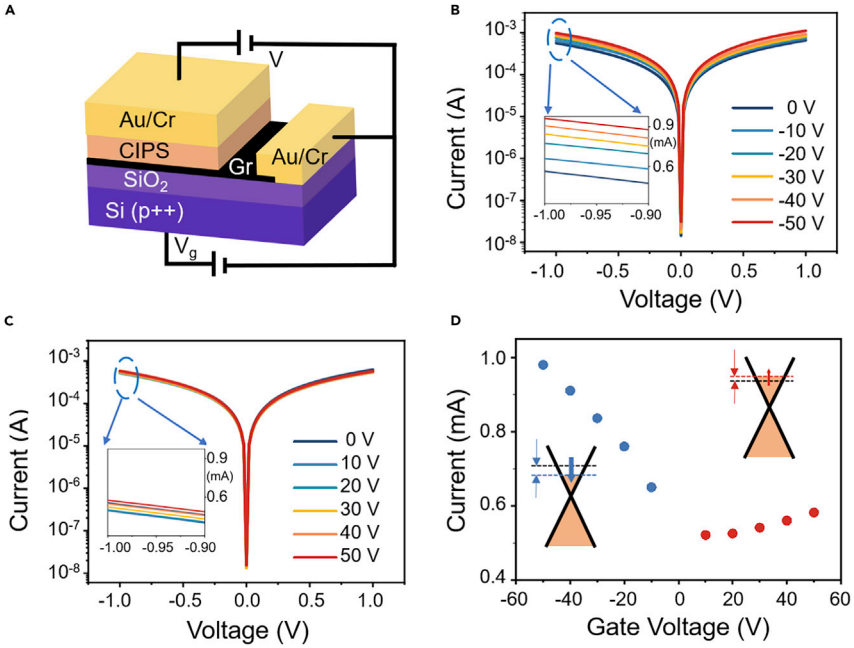

Figure 5. Asymmetric gate tunability in CrCG tunneling junction

(A) Schematic of the gate-tunable FTJ structure. The 260-nm-thick SiO_2 serves as the dielectric layer, and the bottom Si (p++) serves as the back-gate electrode.

(B and C) On-state current-voltage characteristics for FTJs under different negative (B) and positive (C) gate voltages. The difference in the on-state currents is highlighted in the inset. The on-state current increased more obviously with the varying negative gate voltages than with the varying positive gate voltages.

(D) On-state currents (with −1 V reading voltage) under different gate voltages. This asymmetric gate-tunable on-state current under positive and negative gate voltages arises from the initial n-type doping of graphene. As illustrated by the inset, when graphene is initially n-type doped, the negative voltages will move the Dirac point close to the Fermi level, but the positive voltages will move the Dirac point away from the Fermi level. The energy levels are easier to be modulated when the Dirac point is moved close to the Fermi level with respect to the scenario when the Dirac point is moved away from the Fermi level.

Asymmetric gate tunability in CrCG FTJs

Given the remarkable tunability of 2D materials in general, we further utilize the Si substrate and SiO_2 dielectric to supply a back gate to tune the TER of the CrCG FTJs with the device structure shown in Figure 5A. Figures 5B and 5C show the on-state current-voltage characteristics of our FTJ devices with different positive gate voltages (Figure 5B) and negative gate voltages (Figure 5C), respectively. The insets of Figures 5B and 5C show that the on-state current increased more obviously under negative gate voltages with respect to those under positive gate voltages. Figure 5D summarizes the on-state current values under different gate voltages with a reading voltage of −1 V, confirming that the on-state current changes faster with the varying negative gate voltages than with varying positive gate voltages.

The asymmetric gate tunability of on-state currents is related to the initial doping scenario of the graphene. Specifically, when a FTJ is in on state, the Fermi level of the graphene is above the Dirac point (Figure 5D). Applying the gate voltages of the same amplitude but of opposite signs will cause the same amount of charge increase or decrease. When applying a negative voltage, Fermi level will move downward at a faster pace with respect to moving upward under a positive voltage. This is

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simply because the density of states near the Dirac point is lower but the density of states away from the Dirac point is higher.

Conclusions

In summary, we constructed vdW heterostructures based FTJs consisting of 2D ferroelectrics CIPS and 2D electronic materials (i.e., graphene and TMDs) and demonstrated a giant TER of $>10^{10}$ at room temperature. The record-high TER arises from the giant ferroelectric modulation of the band alignments through the vdW stacks. The insertion of both monolayer MoS_2 and monolayer WSe_2 can effectively enhance the TER of CrCG tunnel junction by an order of magnitude yet with different underlying band realignment behaviors. Furthermore, the 2D vdW FTJs allow the fine gate tunability of the on-state tunneling current, which endows vdW FTJs with extra electrical controllability for enhanced functions. Our discovery of the giant TER in vdW FTJs and the demonstration of the effectiveness of the layer-by-layer engineering of FTJs open the door to the emerging class of vdW heterostructures for studying the fundamental tunneling physics and exploring tunneling devices such as nonvolatile memories, logics, and logic-in-memory devices.

EXPERIMENTAL PROCEDURES

Resource availability

Lead contact

Further information and requests for resources and reagents should be directed to and will be fulfilled by the lead contact, Cheng Gong (gongc@umd.edu).

Materials availability

This study did not generate new unique materials.

Data and code availability

Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon request.

Synthesis of CIPS crystals

We grew CIPS via a flux-based method.[35] First, we synthesized P_2S_5 via reaction of the elements P (Alfa Aesar, Puratronic, 99.999%) and S (Alfa Aesar, Puratronic, 99.999%) in a stoichiometric ratio at 300°C in a sealed, thick-walled quartz ampoule. The metal elements Cu (Alfa Aesar, powder, ~100 mesh, 99.999%, reduced in H_2 gas at 300°C prior to reaction) and In (Alfa Aesar, ingot, 99.999%) were mixed with the flux in a molar ratio Cu:In:P_2S_5 of 1:1:3 and placed in a 5-mL Canfield crucible set (LSP Industrial Ceramics). The crucible set, including frit and catch crucible, was sealed in quartz under partial Ar atmosphere. The sealed ampoule was then placed in a muffle furnace, heated to 650°C at 30°C/h, held at that temperature for 36 h, and then cooled to 250°C at 6°C/h. At 250°C, the sample was removed from the furnace and centrifuged to decant the P_2S_5 flux, leaving crystals behind of a maximum size of 8 × 8 mm. We performed energy-dispersive X-ray spectroscopy (EDS) analysis and found compositions of CIPS, within error. We also used CIPS synthesized via a chemical vapor transport method[6] in some testing experiments.

Device fabrication

For the Cr/CIPS/TMD/graphene FTJs, we first mechanically exfoliated thin-layer graphene on a 260-nm-thick SiO_2/Si substrate. Then, monolayer TMD and thin CIPS film were exfoliated on polydimethylsiloxane (PDMS) and transferred onto the graphene flake in sequence, using the all-dry viscoelastic stamping procedure through a

transfer stage under the optical microscope. The polymethyl methacrylate (PMMA) was spin coated on the graphene/CIPS or graphene/TMD/CIPS heterostructure as photoresist and annealed in air at 120°C for 2 min. Finally, electron-beam lithography was used to lay out the TE, and the bilayer metallic electrodes (Cr/Au, 5/50 nm) were deposited by thermal evaporation (Figure S4).

Electrical characterization

A pulse writing voltage with a period of 200 ms was used to flip the ferroelectric polarization of the tunneling devices by Keithley 4200A-SCS semiconductor parameter analyzer. Depending on the specific measurement modes, a series of sweeping voltages were applied to collect the current-voltage data or a single reading voltage (e.g., −0.4 V) was applied to record the tunneling current. To avoid the ferroelectric-paraelectric phase transition undesirably caused by the Joule heating effect arising from the tunneling current, a low duty cycle (0.5%) was used to keep the device temperature lower than the ferroelectric Curie temperature (*Tc*) of CIPS (~315 K).[17] The pulse writing voltage was tested from a relatively low amplitude (2 V) with an increasing step of 0.2 V to avoid unwanted device damage.

Raman spectroscopy

The measurement was based on an Andor spectrometer with a Newton 970 series camera at room temperature. The 532-nm laser was focused on the samples via a 50× objective lens with a numerical aperture of 0.5. We used one band-pass filter to clean up the laser spectral noise and three Bragg notch filters to suppress the Rayleigh line bandwidth down to ~8 cm^{-1}. A 1,200 grooves mm^{-1} grating was used to achieve a spectral resolution of 0.79 cm^{-1} per pixel. The integration time was 15 s for each spectrum acquisition.

DFT calculations

The *ab initio* calculations were performed by DFT using the Vienna Ab initio Simulation Package (VASP) code.[36,37] The exchange and correlation functionals were implemented by the generalized gradient approximation (GGA) of the Perdew-Burke-Ernzerhof (PBE) functional. The monolayer-MoS_2/bilayer-CIPS heterostructure was constructed with a vacuum layer larger than 15 Å, in order to avoid interactions between adjacent super cells. The lattice constants for pristine MoS_2 and CIPS were 3.16 and 6.05 Å, respectively. Here, we fixed the lattice constant of CIPS and deposited the 2 × 2 MoS_2 supercell on the bilayer CIPS unit cell. The lattice mismatch was ~4.3%. All structures were fully relaxed until the force converged on each atom less than 10^{-2} eV/Å, and the energy criterion was set to 10^{-6} eV. The plane-wave cutoff energy was set to 420 eV. Brillouin zone was sampled using Γ-centered 14 × 14×1 Monkhorst-pack k mesh. The vdW interaction was corrected by the DFT-D3 Grimme method.

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.matt.2022.10.014.

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AUTHOR CONTRIBUTIONS

C.G. conceived and supervised the project. Q.W., T.X., and Z.S. fabricated tunneling devices and carried out the Raman characterizations under the supervision of C.G. Q.W., T.X., and N.A.B. conducted the electrical measurements with assistance from A.T.H., under the supervision of C.G. and A.L.F. J.C.K. carried out AFM measurements under the supervision of A.L.F. M.A.S. and B.S.C. synthesized CIPS crystals via a flux-based method. Q.T. and X.L. synthesized CIPS crystals via a chemical vapor transport method. S.H.L. and Z.M. synthesized WSe_2 crystals. J.-P.W. and T.L. participated in the development of the device concept of vdW FTJs. Q.W. and C.G. analyzed the data. Q.W. and C.G. wrote the manuscript with assistance from Z.S. All authors commented on the manuscript.

DECLARATION OF INTERESTS

The authors declare no competing interests.

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