Generalized Architecture of a GaN-based Modular Multiport Multilevel Flying Capacitor Converter

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***Abstract*- This paper proposes a generalized Gallium Nitride (GaN) based modular multiport multilevel flying capacitor architecture. In other words, the attractive flying capacitor multilevel (FCML) design and the full-bridge unfolding circuit are employed to develop a multiport multilevel converter architecture that fits various applications. Each module can be designed to contain any combination of AC and DC ports connected through DC-to-DC and DC-to-AC power conversion paths. These conversion paths are FCML topologies that can be designed with any number of levels; the DC-to-AC paths incorporate the full-bridge unfolding circuit. Two example prototypes with open-loop control, three-port and four-port, have verified this generalized architecture. A single module 3 kW three-port four-level prototype with two DC ports and an AC port has achieved a compact size of 11.6 in^3 (4.8 in ×4.3 in × 0.56 in) and a high power density of 258.6 W/in^3. The three ports are connected through DC-to-AC and DC-to-DC paths that have achieved peak efficiencies of 98.2 % and 99.43 %, respectively. The total harmonic distortion (THD) of the AC port's voltage and current are 1.26 % and 1.23 %, respectively. It operates at a high switching frequency of 120 kHz because of the GaN switches and has an actual frequency (inductor's ripple frequency) of 360 kHz thanks to the frequency multiplication effect of the FCML. The four-port prototype contains three DC ports and an AC port and achieved similar high figures of merit. These experimental results of the two prototypes of high efficiency, power density, and compact size are presented in this article and highlight this architecture's promising potential. The choice of the number of modules, ports, and levels depends on the application and its specification; therefore, this proposed generalized structure may serve as a reference design approach for various applications of interest.**

I. INTRODUCTION

The growing concerns about climate change that has affected the environment negatively in many ways call for immediate actions to keep global warming below the limit set out in the Paris agreement of 1.5 degrees Celsius above the pre-industrial level [1]. The energy and transportation sectors are considered the primary sources of greenhouse gas emissions in the United States (US) [2]. In 2020, internal combustion engine vehicles accounted for the majority of CO_2 emissions in the US [2]; hence, replacing them with Electric Vehicles (EV) has the highest potential among other solutions to slow down global warming. However, they must be charged from renewable sources such as Photovoltaic (PV) to eliminate the indirect CO_2 emissions, so EVs become environmentally friendly in the true sense. To increase the rate of PVs and EVs penetration into the electric grid, battery energy storage (ES) should be added to the PV systems to overcome their intermittency nature and to the EV charging stations to reduce their negative impacts on the electric grid [3], [4]. Moreover, renewable energy sources deployment and integration have significantly increased due to this decarbonization era and the recent favorable developments in battery cost reduction, efficiency, and reliability [4].

As a result, multiport converters (MPCs) have gained increased attention since they are attractive candidates that integrate multiple ports, facilitating the interface of multiple sources and loads in a single unit and ensuring power flow between ports [4]–[6]. These qualities of the multiport converters made them fit various applications seamlessly and efficiently.

Generally, multiport converters are categorized as isolated, partially isolated, and non-isolated [4]–[6]. All ports are isolated from each other in the isolated multiport converters through high-frequency multiwinding transformers that provide the galvanic isolation and high voltage gain as they are required in some applications; however, the size, efficiency, and cost are compromised due to the bulky, lossy, and expensive transformers [7]–[11].

In the partially isolated MPC, nonisolated ports at one side of a high-frequency transformer are galvanically isolated from a single port or multiple nonisolated ports on the other side. They are suitable in applications where isolation is not required between all ports and high voltage gain is needed. They provide a reduced cost and size compared to the isolated MPCs and higher voltage gain compared to the non-isolated MPCs [12]–[19].

Lastly, in the non-isolated MPC, the design complexity, size, and cost are reduced, while power density and efficiency increased compared to the nonisolated and partially isolated MPCs due to the absence of the transformers. However, they can be employed only in applications where galvanic isolation is not a requirement. Plenty of nonisolated MPCs are proposed in the literature for various applications, including but not limited to the nonisolated DC-DC MPC proposed in [20] for PV-ES systems and regenerative braking applications. It is developed by combining buck and bidirectional buck-boost converters and contains one unidirectional and two bidirectional ports. It employs few components; however, it can be used only when the PV voltage is higher than the ES and the DC bus voltages. The family of the nonisolated MPCs in [21] is developed by introducing an ES third port using a bidirectional buck converter that shares its switches with two

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switches of various types of conventional two-port hybrid switched capacitor converters. It is verified for a PV standalone system. The nonisolated MPC proposed in [22] consists of five ports, three ports for different sources and two load ports. It is constructed of a bidirectional buck-boost-like structure and is suitable for DC microgrid applications. A high voltage gain nonisolated MPC boost converter is presented in [23]. It has the advantage of input current ripple cancellation and consists of two input ports and only one unidirectional output port. Another nonisolated MPC that is used for a standalone PV-ES system to drive a DC motor or LED lighting is proposed in [24]. It operates at different operating modes, allowing it to work as a boost, buck-boost, and forward converter. A nonisolated MPC employed as an off-board EV charging station is constructed in [25]. It is realized by linking the AC grid through a bidirectional totem pole PFC, a PV via a unidirectional DC-DC boost converter, and ES through a bidirectional buck converter to a common DC bus. In [26], a nonisolated MPC consisting of two unidirectional ports for PV and the load and a bidirectional port for the battery is developed through a unique connection of unidirectional buck and buck-boost converters and bidirectional boost converter. It offers a higher voltage gain than the conventional two-port converters that construct it. A family of nonisolated MPCs that contain only one inductor is derived in [27] based on four conventional two-level DC-DC converters.

The objective of our article is to design and develop extendable modular nonisolated multiport converter architecture that has the potential to fit various applications such as the ones mentioned in the literature above and more to include low, medium, and high voltage and power applications. Besides, the target is to achieve a small size, low weight, high efficiency, high power density, low harmonic distortion, and low cost multiport architecture.

Deriving the targeted nonisolated multiport converters from the two-level conversion concept is not attractive, especially in medium and high-voltage applications, because most of the conventional hard-switching two-level topologies have some common limitations, such as bulky magnetic components and the switches are required to block high voltages. The switches are required to block the entire input voltage for the buck, the entire output voltage for the boost, and the sum of the input and output voltages for the buck-boost converter, which necessitates employing high voltage rating switches that lead to lower efficiency, higher cost, high filter requirements, and high harmonic distortion [28]. This makes them unsuitable for achieving the targeted multiport converter with superior qualities for various voltage and power applications.

Therefore, developing the targeted nonisolated multiport converters based on the multilevel conversion concept is an attractive alternative to support our road map towards developing high figures of merit multiport converters.

The multilevel converters are popular among researchers as a preferred choice for a power conversion system in many applications such as traction drives [29] and off-board chargers [30] for electric vehicles (EV), renewable energy systems [31], high voltage DC/AC transmissions [32], energy storage [33], motor drives [34] and solid state transformers [35]. This is due to their several benefits over the conventional two-level converters, including low total harmonic distortion (THD), minimization of magnetic components, less voltage stress across switches, and reduced voltage transition between levels [36]–[39]. Multilevel topologies can be classified into three main types: cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor multilevel converters (FCML). The NPC multilevel converter suffers from asymmetrical distribution of power losses among switches and diodes, which makes the thermal design challenging. In addition, the balancing problem is critical for the NPC, and an additional balancing circuit is required [40]. Although CHB multilevel converters are highly modular and scalable, the voltage ripple at the fundamental frequency of the AC side requires larger energy storage for the sub-module capacitors [41]. The FCML allow for a minimum storage requirement for the capacitors because they are charging and discharging at the switching frequency [42], [43]. The FCML has been gaining increased attention since its first introduction in [44] because it has several attractive advantages: the capability to naturally balance its capacitor voltages to the desired values using Phase Shifted Pulse Width Modulation (PSPWM) [44]; the frequency multiplication effect seen by the inductor; the voltage swing reduction across the inductors; and the power semiconductor devices only need to block a fraction of the input voltage, which enables the use of low voltage rating switches in medium and high voltage applications [42]–[45]. In addition, FCML processes power with high quality output voltage and current [44]. The wide application of the FCML, due to its high power density, high efficiency and modularity, has made it possible to be successfully designed as: DC-AC [42]–[44]; AC-DC [46]–[49]; interleaved bidirectional AC-DC and inverter [50]–[52]; and as DC-DC [53], [54].

Thus, the FCML's multifunctionality, flexibility, and attractive inherent features are the motivation for choosing it to derive our targeted high figures of merit multiport architecture in this article.

To further support the road map toward achieving high figures of merit multiport multilevel converters, wide band gap (WBG) semiconductor Gallium Nitride (GaN) offers better suitability compared to silicon power devices. WBG materials provide a higher band gap, a higher electric breakdown, increased electric velocity, and a higher melting point [55]–[57]. Additionally, the devices can be built on Si substrate to achieve a low-cost fabrication process. The efficiency is enhanced because the GaN power devices inherit low on-resistance due to the generation of two-dimensional electron gas and low gate charge that reduces the conduction and switching loss, respectively [58]. Besides, GaN devices have a smaller footprint compared to their Si counterparts and can operate at higher frequencies with reduced switching losses; therefore, the passive components' weight and volume can be reduced, and the power density as a whole will be improved.

Based on the above discussions, it is clear that FCMLs in multiport configuration with GaN devices are highly attractive as a power conversion system for a wide range of applications.

The work in this article employs flying capacitor multilevel topology based on GaN switches and an unfolding circuit to

design and develop an expandable modular multiport multilevel architecture that has the potential to fit various applications.

The key contributions and salient features of this proposed multiport multilevel converter architecture are as follows:

1) Unprecedented employment of the attractive FCML based on GaN switches to develop multiport multilevel converter architecture.
2) This article's generalized architecture can be expanded to any number of input and output ports. It can be configured to contain either DC ports or AC ports, or a combination of both. All ports can be unidirectional or bidirectional. As a result, this architecture fits a wide range of applications.
3) It has achieved superior figures of merit, such as very high efficiency and power density and very low total harmonic distortion.
4) All ports are decoupled; hence, if one port source is not connected or fails, the other ports' operation is not affected.
5) In addition to employing GaN switches with low footprint and low switching and conduction losses, the switches block only a fraction of the input voltage, allowing the employment of low voltage rating switches with lower ON-resistance, which further reduces switching and conduction losses and d_v/d_t.

The proposed multiport architecture has the potential to fit a wide range of applications, including but not limited to the integration of ES with PV systems into the AC grid; PV and ES systems for residential and standalone AC loads; PV and ES integration into EV fast and ultra-fast charging stations; and uninterruptable power supply (UPS) systems. However, this article proposes this architecture in general without a specific application which lays the ground for researchers to use this architecture for specific applications and provides in-depth analysis and discussion of the proposed structure, including limitations of design and control based on the application.

The rest of this paper is organized as follows. Section II explains the generalized multiport multilevel converter architecture and discusses the design considerations. The principle of operation is presented in Section III, and it contains two subsections for the operation principles of the DC-to-DC path and the DC-to-AC path. In Section IV, two hardware prototypes, a modular three-port four-level prototype, and a four-port four-level prototype, their hardware design, component selection, and experimental results are provided separately in two subsections. Finally, the conclusion is drawn in Section V.

II. The Generalized Multiport Multilevel Converter Structure and Design Considerations

A generalized block diagram of the proposed modular multiport multilevel converter is shown in Fig. 1. This modular multiport multilevel converter may contain any number, k, of parallel modules and each module can be designed to have N number of ports. Each of these N ports can be unidirectional or bidirectional, since each port can output power from or input power to a respective path to which it is connected. Each path can be designed with any m number of levels and configured to operate as a bidirectional or unidirectional DC-to-DC or DC-to-AC m-level path. All m-level paths and port-1 are linked through a common linking capacitor C_{Link}. The number of ports N, paths $N-1$, levels m, and modules k can be determined based on the application and its specifications in the design stage.

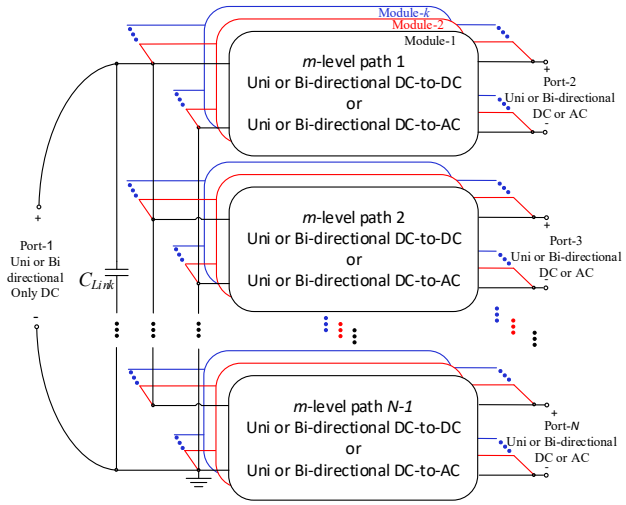


Fig. 1 The generalized block diagram of the modular multiport multilevel architecture.

The generalized schematic of a single multiport multilevel module is shown in Fig. 2. Each module can be constructed of any number, N, of DC and AC ports connected through $N-1$ m-level paths. Each path has two interfaces. One interface of each path and DC Port-1 are linked to the linking capacitor C_{Link}, while the other interfaces of each path are connected to a respective DC or AC port. Each path can be a bidirectional or a unidirectional DC-to-DC or a DC-to-AC path. The DC-to-DC path is a flying capacitor multilevel (FCML) with "m" number of levels. Similar to the DC-to-DC path, the DC-to-AC path is a FCML with "m" number of levels; however, it incorporates a full-bridge unfolder for the AC generation. The number of levels is a design criterion that affects the component counts, the capacitor and inductor value and size, the switching frequency, the blocking voltage of the power switches, the THD, efficiency, and power density. For instance, the higher number of levels yields more component counts and complexity due to the increased number of capacitors, switches, and associated driving circuitry. However, increasing the number of levels "m" reduces the nominal voltage that the power semiconductor switches need to block according to (1) and gives the advantage of employing low voltage switches, which have higher figures of merit compared to switches with high voltage ratings.

$$V_{switch} = \frac{V_{Link}}{m-1}, \tag{1}$$

where V_{switch} is the switch nominal blocking voltage and V_{Link} is the linking voltage across the linking capacitor. Therefore, the number of levels is a design criterion selected based on the application and its specifications.

The challenge of limiting the use of large filtering inductors in two-level PWM converters can be well addressed using the FCML topology [43]. The FCML reduces the filtering inductance

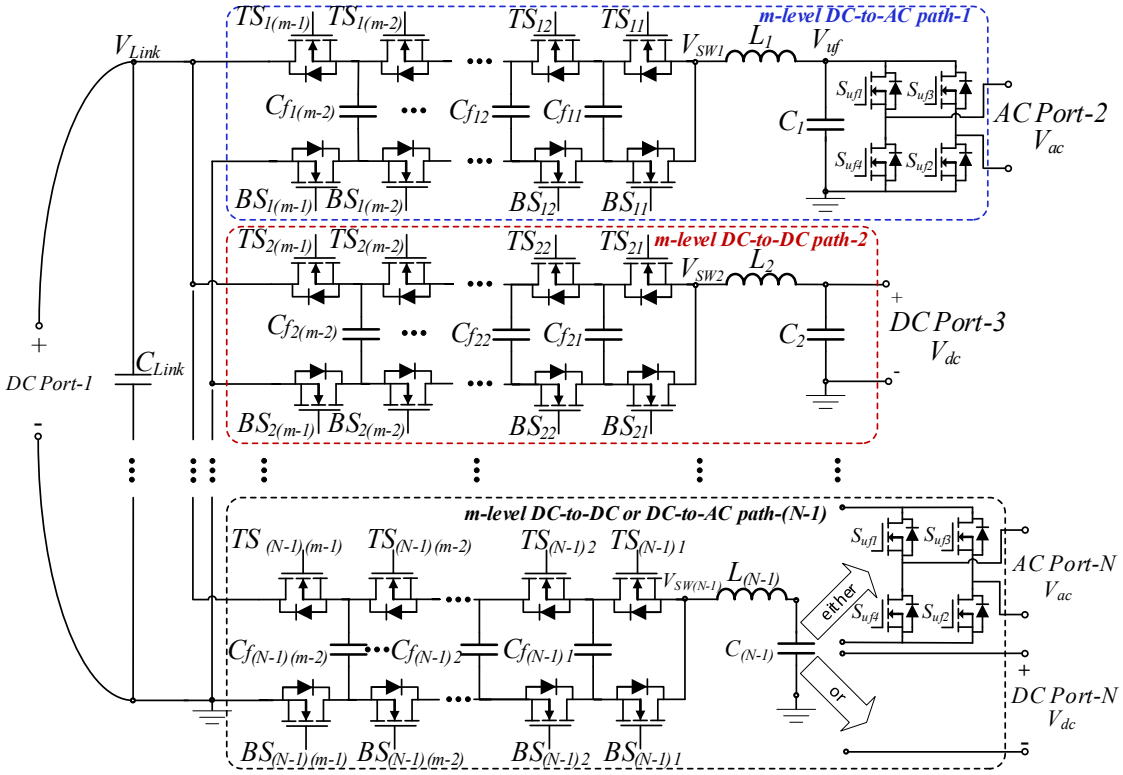


Fig. 2 The generalized schematic of a single multiport multilevel module.

due to two factors. The first factor is that the actual frequency (f_{actual}) seen by the filtering inductors (L_1, L_2…$L_{(N-1)}$) is increasing by a factor of (m – 1) more than the switching frequency (f_s) of each switch when controlling the switches using the PSPWM scheme [42]–[45]. The second factor is that the voltages across the filtering inductors (V_L) are reduced by a factor of (m – 1) and equal to the switch nominal blocking voltage in (1). These two factors make it possible to reduce the inductors' inductances by a factor of $(m-1)^2$ compared to the inductances of the two-level conventional topologies [42]–[45]. In other words, the inductors' current ripples decrease proportionally to $(m-1)^2$ [42]–[45].

The inductors' inductance (L) values are calculated as

$$L = \frac{(1-D_{actual})\ D_{actual} V_{actual}}{\Delta i_L\ f_{actual}}, \tag{2}$$

where Δi_L is the inductor current ripple, f_{actual} is the actual frequency seen by the inductors, which is defined in (3), D_{actual} is the actual duty cycle seen by the inductors, which is calculated by (4) [42]–[45], and V_{actual} is the actual voltage that is equal to all of the following: the step increment height of the switching voltage V_{SW1} annotated in Fig. 2 which is an m-level staircase voltage; the amplitude of the switching voltage V_{SW2} annotated in Fig. 2 which is a pulsed width modulated voltage; the switches' nominal blocking voltage V_{switch} in (1); and the voltage across the first flying capacitors (V_{Cf11}, V_{Cf21} and $V_{Cf(N-1)1}$) as will be seen later.

$$f_{actual} = (m-1) \times f_s. \tag{3}$$

$$D_{actual} = (m-1)D - Floor[(m-1)D], \tag{4}$$

where D is the top switches' duty cycle in each m-level path, which is the standard duty cycle of the conventional two-level topologies. The actual duty cycle value D_{actual} that should be used in (2) to size the inductor in order to guarantee that the inductor current ripple is below the maximum allowed value specified in the design for all the range of the standard duty cycle D is equal to 0.5. This 0.5 value of D_{actual} can be obtained for any m-level by substituting the value of D expressed in (5) into (4).

$$D = \frac{1}{2\,(m-1)}. \tag{5}$$

Equation (2) is used to draw the normalized inductor inductance (normalized to the 2-level) against the standard duty cycle for 2, 3, 4, and 5-level FCML paths at a fixed and equal switching frequency, linking voltage, and inductor current ripples, which are shown in Fig. 3. It is clear that a higher number of levels yields a lower inductance needed for filtering [42]–[45], [59]. According to (5), the values of the standard duty cycle that make the actual duty cycle equal to 0.5 for the two, three, four, and five levels are 1/2, 1/4, 1/6, and 1/8, respectively. It can be observed from Fig. 3 that these standard duty cycles' values correspond to the largest inductor inductance values at their respective level. Therefore, by substituting the actual duty cycle's value of 0.5, (1), and (3) into (2), the expression for the largest inductor needed for any m-level to keep the inductor current ripple within the designed limit under all operating conditions is

$$L = \frac{0.25\ V_{Link}}{(m-1)^2\ \Delta_{i_L}\ f_s} \tag{6}$$

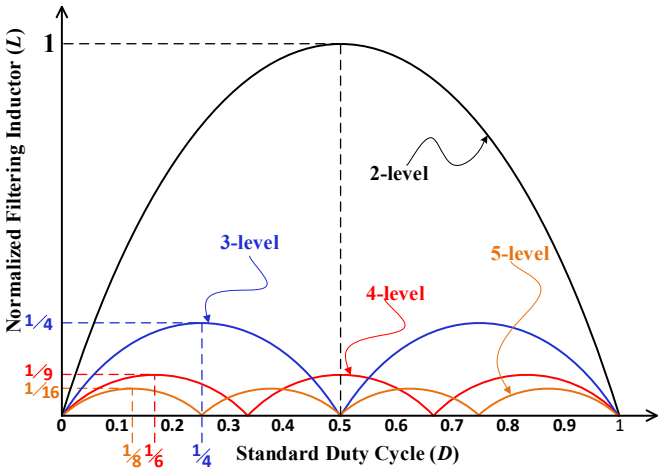


Fig. 3 The normalized inductor inductance vs standard duty cycle for 2,3,4, and 5-levels FCML paths with an equal switching frequency, linking voltage, and inductor current ripples.

Additionally, it should be noted that when putting the number of levels "m" equal to two and substituting (1), (3), and (4) into (2), it results in the expression of the inductor in (7), which is nothing but the equation used to design the inductance value for the conventional buck converter. Therefore, the conventional buck converter can be considered a two-level flying capacitor multilevel topology.

$$L = \frac{(1-D)\,D\,V_{Link}}{\Delta_{i_L}\,f_s} \tag{7}$$

Besides the inductors, the capacitors are the main energy transfer elements in the FCML paths. Each path in Fig. 2 contains $(m-2)$ flying capacitors; where flying capacitors $C_{f11}\ldots C_{f1(m-2)}$, are in the first path. $C_{f21}\ldots C_{f2(m-2)}$ are in the second path, and $C_{f(N-1)1}\ldots C_{f(N-1)(m-2)}$ are in the $(N-1)$ path. The desired voltages across the flying capacitors [42]–[45] are expressed as

$$V_{Cf_{xy}} = \frac{y\,V_{Link}}{m-1}, \tag{8}$$

where V_{Cfxy} is the voltage across the y^{th} flying capacitor in the x^{th} path, where $x = 1, 2\ldots(N-1)$ and $y = 1, 2\ldots(m-2)$. Therefore, the voltages across the first flying capacitors in all paths are equal to each other and the voltages across the second flying capacitors in all paths are equal and so on, where the voltages across the $(m-2)$ flying capacitors in all paths are equal to each other as detailed in Table I.

TABLE I
FLYING CAPACITOR VOLTAGE VALUES

Capacitors' Voltage Labels	Capacitor Voltages (V)
$V_{Cf_{11}} = V_{Cf_{21}} = V_{Cf_{(N-1)1}}$	$\frac{1\times V_{Link}}{m-1}$
$V_{Cf_{12}} = V_{Cf_{22}} = V_{Cf_{(N-1)2}}$	$\frac{2\times V_{Link}}{m-1}$
$V_{Cf_{1(m-2)}} = V_{Cf_{2(m-2)}} = V_{Cf_{(N-1)(m-2)}}$	$\frac{(m-2)\times V_{Link}}{m-1}$

To design the flying capacitors' capacitance, one should consider the maximum allowed voltage ripple across the capacitors because it affects the maximum voltage each switch must block. According to (1), each switch's nominal blocking voltage is a fraction of the linking voltage. However, because each switch blocks the voltage difference between its adjacent flying capacitor voltages, the switches should be selected to block a maximum voltage of

$$V_{SW,max} = \frac{V_{Link}}{m-1} + \Delta V_{Cf}, \tag{9}$$

where ΔV_{Cf} is the flying capacitor voltage ripple and $V_{SW,max}$ is the switch maximum blocking voltage [43].

According to (8) and as detailed in Table I, the voltage difference between every two consecutive flying capacitors is $V_{Link}/(m-1)$. Thus, there must be a voltage difference between the flying capacitor voltages at all times for the proper functionality of the FCML paths [42]–[45]. This voltage difference is maintained by making all top and bottom switch pairs work in a complementary fashion at all times. To illustrate, Fig. 4 shows a portion from an x^{th} path which contain the following top and bottom switch pairs, (TS_{xa}, BS_{xa}), ($TS_{x(a+1)}$, $BS_{x(a+1)}$), and ($TS_{x(a+2)}$, $BS_{x(a+2)}$). In each pair, the switches are complementary to each other to keep a voltage difference between the two consecutive flying capacitors C_{fxa} and $C_{fx(a+1)}$, where x is the path number 1, 2, …, or $(N-1)$ and a is an integer greater than 0. Moreover, the voltage ripple across the flying capacitors should be within the range of $0 < \Delta V_{Cf} < V_{Link}/(m-1)$ to avoid any unwanted instants of V_{Cfxa} exceeding $V_{Cfx(a+1)}$, resulting in the body diodes of the switch between the capacitors turning on and causing a malfunction in the FCML path [60]. Therefore, the capacitance of the flying capacitors should be designed to ensure that the voltage ripple across the flying capacitors is below the maximum allowed value in all operating conditions [60].

The voltages across the flying capacitors can be passively balanced at their desired values by controlling the switches of

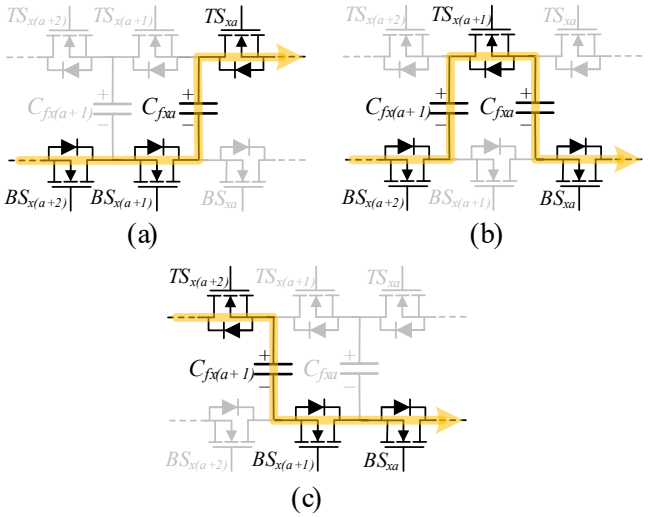


Fig. 4 A portion of the x^{th} FCML path shows the flying capacitors' charging and discharging mechanism for one cycle when operating within the range of $0 < D \leq \frac{1}{m-1}$.

the FCML paths using the PSPWM technique [44], [61], [62]. The flying capacitors charging and discharging mechanisms and times can be explained using Fig. 4 and Fig. 5, where Fig. 5 shows the PSPWM signals of the top switches for the portion of the x^{th} FCML path shown in Fig. 4 during the three main ranges of the standard duty cycle, D [43], [49].

The flying capacitor C_{fxa} discharges only if its adjacent top switches TS_{xa} and $TS_{x(a+1)}$ are ON and OFF, respectively, as shown in Fig. 4(a) and Fig. 5(a). It charges only if they are OFF and ON, respectively, as depicted in Fig. 4(b) and Fig. 5(a). In the same pattern, the flying capacitor $C_{fx(a+1)}$ discharges when its adjacent top switches $TS_{x(a+1)}$ and $TS_{x(a+2)}$ are ON and OFF, respectively, as in Fig. 4(b) and Fig. 5(a),. It charges only if they are OFF and ON, respectively, as in Fig. 4(c) and Fig. 5(a). Moreover, it is clear from Fig. 4 and Fig. 5(a) that each capacitor charges and discharges one time every switching cycle. This means that the charging and discharging process occurs at the switching frequency, which reduces the energy storage requirement and significantly reduces the required capacitance [42], [43].

It can be seen in Fig. 5 that the charging and discharging times of the flying capacitors depend on the duty cycle and the phase shift between the PWM signals of the adjacent switches [43], [49]. For $0 < D \leq 1/(m-1)$, the charging and discharging intervals depend on the duty cycle and are equal to $D \cdot T_s$ as shown in Fig. 5(a), where T_s is the switching period. For $1/(m-1) \leq D \leq 1-(1/(m-1))$, the charging and discharging intervals are constant and equal to the phase shift, or $T_s/(m-1)$, between the PWM signals of the adjacent switches [43], [49] as in Fig. 5(b). Finally, for $1-(1/(m-1)) \leq D < 1$, the charging and discharging intervals depend on the complementary of the duty cycle [43], [49] and are equal to $(1-D)\cdot T_s$ as in Fig. 5(c). Thus, the flying capacitor's capacitance value should be designed based on the largest charging and discharging interval, which is equal to the phase shift for $1/(m-1) \leq D \leq 1-(1/(m-1))$ as shown in Fig. 5(b) to account for the worst-case voltage ripple. It should be noted that the other operating conditions will result in lower flying capacitor voltage ripples, because they have lower charging and discharging times [41], [43], [49]. Therefore, the charging time, t_c, and the discharging time, t_d, that are used for sizing the flying capacitors are equal and can be expressed as

$$t_c = t_d = \frac{T_s}{m-1}. \tag{10}$$

According to the time in (10) and the load current, I_{Load}, that is charging and discharging the capacitors, the largest change in charge, ΔQ_{Cf}, of the capacitors is expressed as

$$\Delta Q_{Cf} = I_{Load} x \frac{T_s}{(m-1)}, \tag{11}$$

where I_{Load} is the DC load current in the DC-to-DC path, or the peak load current in the DC-to-AC path.

Finally, the required capacitance for each flying capacitor to keep the voltage ripple within the limit at a specific load current is determined as

$$C_f = \frac{\Delta Q_{Cf}}{\Delta V_{Cf}} = \frac{I_{Load}}{\Delta V_{Cf}\, f_s\, (m-1)}. \tag{12}$$

Therefore, the flying capacitor voltage ripple is a design criterion that affects the value of the flying capacitors [42]–[44]. The higher the voltage ripple across the capacitors, the smaller the required capacitance and the more energy is transferred during the switching cycle. However, the voltage stress across the switches becomes higher according to (9).

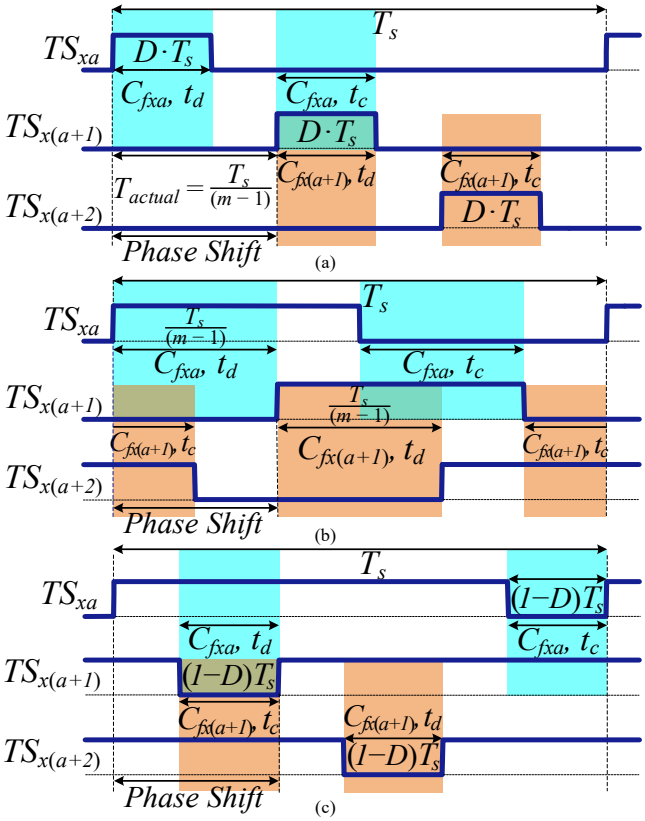


Fig. 5 The PSPWM control signals of the top switches for a portion of an x^{th} FCML path in Fig. 4 with the charging and discharging intervals of C_{fxa} and $C_{fx(a+1)}$ indicated during the three main ranges of the standard duty cycle (a) $0 < D \leq \frac{1}{m-1}$, (b) $\frac{1}{m-1} \leq D \leq 1-\frac{1}{m-1}$, (c) $1-\frac{1}{m-1} < D < 1$.

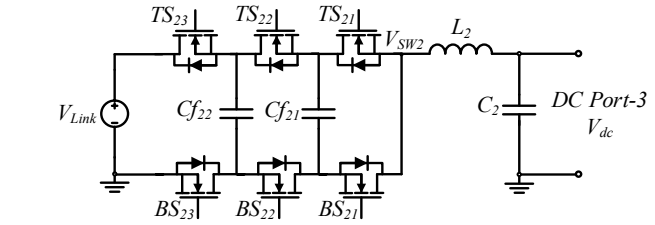
III. Operation Principle

The proposed multiport multilevel converter is constructed of DC-to-DC paths and DC-to-AC paths. Each path is an m-level FCML topology. The power can flow between the ports through the FCML paths that are connected to the linking capacitor. Each port can be unidirectional or bidirectional, since each port can output power from or input power to the respective path to which it is connected. Although the EMI evaluation is not the focus of this work, the proposed multiport converter inherently provides excellent EMI reduction thanks to the FCML topology employed in the proposed converter [42], [43]. Moreover, it should be noted that all the ports share a common ground that minimizes the leakage current and the EMI noise [63]. Moreover, if one port source is not connected or fails, the operation of the rest of the converter's ports are not impacted since all ports are decoupled. The operation of the proposed converter will be separated into two sections, the DC-to-DC path and the DC-to-AC path operation principles.

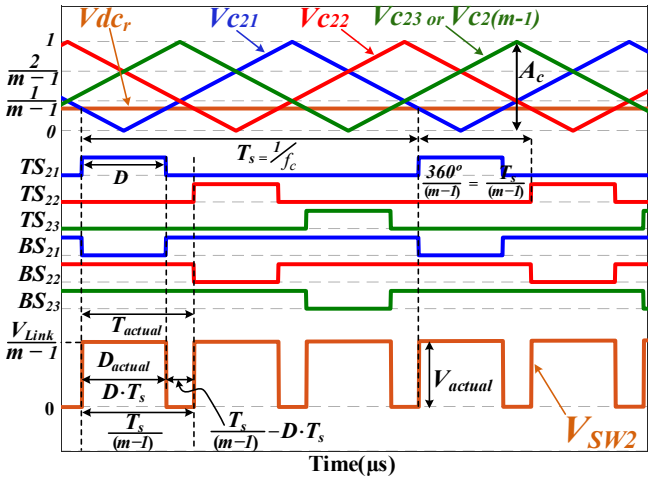
A. The DC-to-DC Path

As shown in Fig. 2, each DC-to-DC path is a flying capacitor multilevel converter with m number of levels. Each DC-to-DC path is constructed *of* $(m-2)$ flying capacitors, $Cf_{x1},\ldots,Cf_{x(m-2)}$, and $2(m-1)$ switches, $(m-1)$ top switches $TS_{x1},\ldots,TS_{x(m-1)}$, and $(m-1)$ bottom switches $BS_{x1},\ldots,BS_{x(m-1)}$. Each DC-to-DC path can operate in buck mode by stepping down the high voltage at DC port-1 or V_{Link} to a lower voltage at any other DC ports. It can also operate in boost mode by stepping up the low voltage at any of the DC ports to a higher voltage at DC port-1 or V_{Link}.

Since the phase shifted pulse width modulation (PSPWM) controls the FCML topology properly, and naturally balances the flying capacitor voltages [43], [44], [61], [62], it is deployed to control the switches of each DC-to-DC FCML path. For the purpose of illustrating the PSPWM scheme construction and generation principle, a four-level ($m = 4$) is selected and shown in Fig. 6. Fig. 6(a) shows the schematic of the DC-to-DC path from Fig. 2 when $m = 4$. Fig. 6(b) shows the simulation of the PSPWM scheme where the triangular carriers (Vc_{21}, Vc_{22} and Vc_{23} or $Vc_{2(m-1)}$) and the DC reference (Vdc_r) are on top, the generated PSPWM signals are in the middle, and the switching voltage V_{SW2} is in the bottom. It can be seen that for any m-level DC-to-DC path, $(m-1)$ triangular carriers are required. These carriers have the same frequency, f_c, the same peak to peak value, A_c, and shifted from each other by 360° / $(m-1)$ or T_s / $(m-1)$. Note the DC reference, Vdc_r, that is compared to each of the triangular carriers. When the DC reference voltage is greater than the triangular carrier, the top switch corresponding to that carrier is turned ON. When the reference is smaller than the triangular carrier, the top switch corresponding to that carrier is switched OFF. Therefore, $(m-1)$ triangular carriers are continuously compared with a DC reference voltage that results in $(m-1)$ PSPWM signals with a fixed duty cycle D that control the $(m-1)$ top switches. The $(m-1)$ bottom switches are complementary to the top ones and have a fixed duty cycle of $(1-D)$. It is clear from Fig. 6 that for $0 < D \leq 1/(m-1)$, the switching voltage, V_{SW2}, is a pulsed width modulated voltage that switches between zero and V_{actual} at the actual frequency, f_{actual}, which is $(m-1)$ times the switching frequency, f_s, of each switch. V_{SW2} is equal to V_{Link} / $(m-1)$ for $D \cdot T_s$ of the actual switching cycle (T_{actual}), when only one top switch is ON. It is zero for the rest of the actual switching cycle equal to $(T_s/(m-1)) - (D \cdot T_s)$, when all the top switches are OFF [43], [49].



(a)



(b)

Fig. 6 (a) the schematic of the DC-to-DC path in Fig. 2 when $m = 4$. (b) The phase shifted PWM Scheme of the four-level DC-to-DC path for $0 < D \leq 1/(m-1)$, the triangular carriers and the dc reference (top), the generated PSPWM signals (middle), and the pulsed width modulated voltage (switching voltage V_{SW2}) (bottom).

Since the voltage across the inductor, V_L, in the DC-to-DC path is the difference between the switching voltage, V_{SW2}, and the DC port-3 voltage, V_{dc}, as in (13), the gain of the DC-to-DC path can be found by applying the volt-second balance on the inductor using (13) over the actual switching cycle, which is equal to the phase shift or T_s / $(m-1)$, as given in (14)

$$V_L = V_{SW2} - V_{dc} \tag{13}$$

$$\left(\frac{V_{Link}}{m-1} - V_{dc}\right)(D \cdot T_s) - (V_{dc})\left(\frac{T_s}{m-1} - (D \cdot T_s)\right) = 0. \tag{14}$$

Simplifying (14) gives the gain of the DC-to-DC path as

$$\frac{V_{dc}}{V_{Link}} = D. \tag{15}$$

It is clear from (15) that the gain of the DC-to-DC m-level FCML path is the same as that of the conventional buck converter.

Additionally, Fig. 6 illustrates the frequency multiplication effect that was expressed in (3). It can be seen that there are $(m-1)$ or three pulses in the pulsed width modulated voltage (switching voltage V_{SW2}) against one pulse in the PSPWM signals in a single switching cycle (T_s) [42]–[45]. In other words, the actual switching cycle, T_{actual}, is $(m-1)$ times smaller than the switching cycle of the PSPWM signals, or the actual frequency seen by the inductors is $(m-1)$ times the switching frequency of each power semiconductor switch [42]–[45]. This switching voltage is filtered by the LC filter (L_2 and C_2) to produce a pure DC voltage (V_{dc}) at the DC Port-3.

B. The DC-to-AC Path

Like the DC-to-DC path, each DC-to-AC path is a flying capacitor multilevel converter with an "m" number of levels. However, each DC-to-AC path includes a full-bridge unfolder for the AC generation[42] . The switches are controlled using the PSPWM technique. For illustration, a simulation is conducted for the DC-to-AC path in Fig. 2 when $m = 4$, as shown in the schematic in Fig. 7(a). For any m-level DC-to-AC path, $(m-1)$ triangular carriers (Vc_{11}, Vc_{12} and Vc_{13} or $Vc_{1(m-1)}$) are required, and they have the same frequency (f_c), same peak-

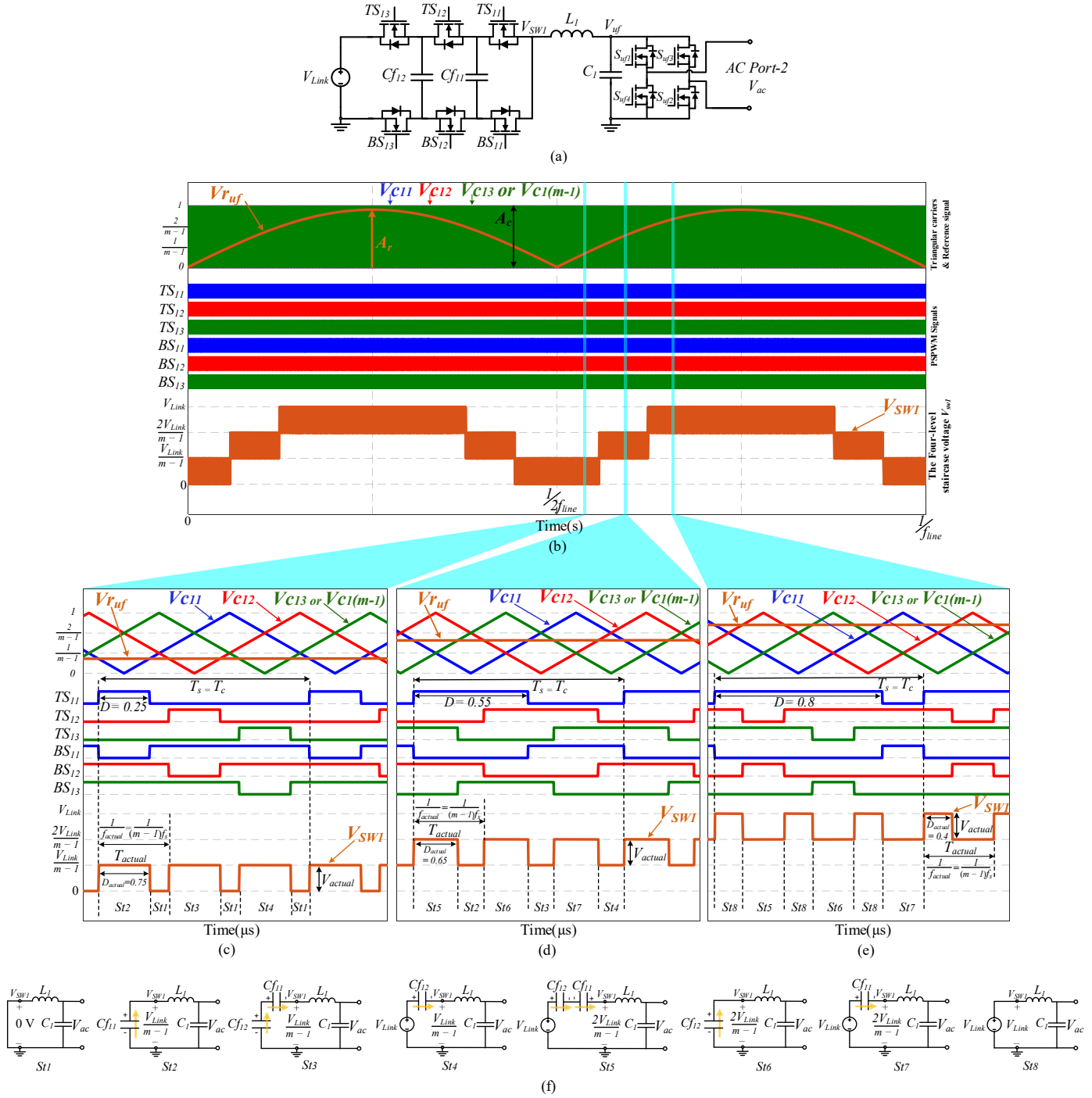


Fig. 7 (a) The schematic of the DC-to-AC path from Fig. 2 when m = 4. (b) The phase shifted PWM scheme of the four-level DC-to-AC path, the triangular carriers and the full-wave rectified sinusoidal reference (top), the generated PSPWM signals (middle), and the four-level staircase voltage (switching voltage VSW1) (bottom). (c) A zoomed-in portion for $0 < D \leq 1/(m-1)$ range. (d) A zoomed-in portion for $1/(m-1) \leq D \leq 1-(1/(m-1))$ range. (e) A zoomed-in portion for $1-(1/(m-1)) \leq D < 1$ range (f) the equivalent circuits for each switching state.

to-peak value (A_c), and shifted from each other by 360° / (m – 1) or T_s / (m – 1).These triangular carriers are continuously compared with a full-wave rectified sinusoidal reference (Vr_{uf}), as shown in Fig. 7(b)(top) or, more clearly, the zoomed-in portions in Fig. 7(c)-(e)(top), to generate (m – 1) PSPWM signals with varying duty cycle D that control the (m – 1) top switches. When Vr_{uf} is greater than the triangular carrier, the top switch corresponding to that carrier is turned ON. When the reference is less than the triangular carrier, the top switch corresponding to that carrier is switched OFF. The (m – 1) bottom switches are switching in a complementary way to the top switches and have a varying duty cycle of ($1 – D$), as shown in Fig. 7(b)(middle), or in the zoomed-in portions in Fig. 7(c)-(e)(middle).

The triangular carriers' frequency equals the switching frequency of each switch, and it determines the frequency modulation

ratio m_f as

$$m_f = \frac{f_c}{2f_{line}}, \tag{16}$$

where $2f_{line}$ is the double line frequency. It should be noted that the frequency modulation ratio is very high, m_f =1000 in Fig. 7(b), and that is why the triangular carriers cannot be distinguished from each other. The higher the frequency modulation ratio, the more accurate the AC voltage will follow the full-wave rectified sinusoidal reference Vr_{uf}, resulting in a cleaner AC voltage and lower THD; however, this will be a trade-off with the increasing switching losses.

The amplitude of the fundamental component of the AC voltage (V_{ac1}) can be controlled by the amplitude modulation ratio (m_a), which ranges between *0* and *1* as

$$V_{ac1} = m_a \cdot V_{Link}, \tag{17}$$

where the amplitude modulation ratio, m_a, is defined in (18) as the ratio of the peak value (A_r) of full-wave rectified sinusoidal reference Vr_{uf} to the peak-to-peak value of the triangular carriers.

$$m_a = \frac{A_r}{A_c}, \tag{18}$$

The generated PSPWM signals shown in Fig. 7(b)(middle) have a duty cycle that varies with time to achieve a short-term average voltage ($V_{average}$) that follows a full-wave rectified sinusoidal reference (Vr_{uf}) to synthesize the switching voltage, V_{SW1}. This switching voltage V_{SW1} is a pulsed *m*-level (4-level in Fig. 7(b)(bottom) staircase voltage that is switching at the actual frequency between two levels of the *m*-level staircase voltage, as shown in Fig. 7(b)(bottom) or the zoomed-in portions in Fig. 7(c)-(e)(bottom). In any level path, there are three main ranges for the duty cycle *D* [43], [49] as summarized in Table II and the zoomed-in portions of Fig. 7(c)-(e) for the four-level case. Table II summarizes the three main ranges for the standard duty cycle *D*; the corresponding short-term average voltage ranges $V_{average}$ of the unfolder's input voltage (the switching voltage, V_{SW1}, after filtering by the L_1C_1 filter) at node V_{uf}; the values of the switching voltage V_{SW1} and how they are generated in each switching state; the switching states; and the charging and discharging of the flying capacitors in each switching state.

The first range of the duty cycle is $0 < D \leq 1/(m-1)$, as shown in the zoomed-in portion in Fig. 7(c), specifically at D = 0.25. In this range, the pulsed *m*-level (4-level in this case) staircase voltage (V_{SW1}) always switches between zero and V_{Link} / $(m-1)$ according to the switching states sequence in Table II, which is $S_{t1} \rightarrow S_{t2} \rightarrow S_{t1} \rightarrow S_{t3} \rightarrow S_{t1} \rightarrow S_{t4} \rightarrow S_{t1}$. The equivalent circuits corresponding to all possible switching states that indicate which flying capacitor is charging or discharging at every switching state are shown in Fig. 7(f). It can be noted from the equivalent circuits and Table II that a combination of the addition or subtraction of the linking voltage and the flying capacitor voltages constructs the switching node voltage V_{SW1}. In addition, it is clear from Fig. 7 and Table II that each flying capacitor charges and discharges once every switching cycle. In other words, the flying capacitors charge and discharge at the switching frequency [42], [43].

The second range of the duty cycle is $1/(m-1) \leq D \leq 1 - (1/(m-1))$ or $1/(m-1) \leq D \leq 2/(m-1)$, as shown in the zoomed-in portion in Fig. 7(d), specifically at D = 0.55. In this

TABLE II
SWITCHING STATES FOR 4-LEVEL FCML PATH

Duty Cycle Range	Switching States	TS_{11}	TS_{12}	TS_{13} or $TS_{1(m-1)}$	C_{f11}	C_{f12} or $C_{f1(m-2)}$	V_{SW1} (V)	Short-Term Average Voltage Range of V_{uf} (V)
$0 < D \leq \frac{1}{m-1}$	*St1*	off	off	off	-	-	*0*	$0 \leq V_{average} \leq \frac{V_{link}}{m-1}$
	St2	on	off	off	↑*Dis*	-	$V_{C_{f11}} = \frac{V_{Link}}{m-1}$	
	St1	off	off	off	-	-	*0*	
	St3	off	on	off	↓*Ch*	↑*Dis*	$V_{C_{f12}} - V_{C_{f11}} = \frac{V_{Link}}{m-1}$	
	St1	off	off	off	-	-	*0*	
	St4	off	off	on	-	↓*Ch*	$V_{Link} - V_{C_{f12}} = \frac{V_{Link}}{m-1}$	
$\frac{1}{m-1} \leq D \leq 1 - \frac{1}{m-1}$ *OR* $\frac{1}{m-1} \leq D \leq \frac{2}{m-1}$	*St4*	off	off	on	-	↓*Ch*	$V_{Link} - V_{C_{f12}} = \frac{V_{Link}}{m-1}$	$\frac{V_{link}}{m-1} \leq V_{average} \leq V_{link} - \frac{V_{link}}{m-1}$ *OR* $\frac{V_{link}}{m-1} \leq V_{average} \leq \frac{2V_{link}}{m-1}$
	St5	on	off	on	↑*Dis*	↓*Ch*	$V_{Link} - V_{C_{f12}} + V_{C_{f11}} = \frac{2V_{Link}}{m-1}$	
	St2	on	off	off	↑*Dis*	-	$V_{C_{f11}} = \frac{V_{Link}}{m-1}$	
	St6	on	on	off	-	↑*Dis*	$V_{C_{f12}} = \frac{2V_{Link}}{m-1}$	
	St3	off	on	off	↓*Ch*	↑*Dis*	$V_{C_{f12}} - V_{C_{f11}} = \frac{V_{Link}}{m-1}$	
	St7	off	on	on	↓*Ch*	-	$V_{Link} - V_{C_{f11}} = \frac{2V_{Link}}{m-1}$	
$1 - \frac{1}{m-1} \leq D < 1$ *OR* $\frac{2}{m-1} \leq D < 1$	*St7*	off	on	on	↓*Ch*	-	$V_{Link} - V_{C_{f11}} = \frac{2V_{Link}}{m-1}$	$V_{link} - \frac{V_{link}}{m-1} \leq V_{average} \leq V_{link}$ *OR* $\frac{2V_{link}}{m-1} \leq V_{average} \leq V_{link}$
	St8	on	on	on	-	-	V_{Link}	
	St5	on	off	on	↑*Dis*	↓*Ch*	$V_{Link} - V_{C_{f12}} + V_{C_{f11}} = \frac{2V_{Link}}{m-1}$	
	St8	on	on	on	-	-	V_{Link}	
	St6	on	on	off	-	↑*Dis*	$V_{C_{f12}} = \frac{2V_{Link}}{m-1}$	
	St8	on	on	on	-	-	V_{Link}	

range, the pulsed four-level staircase voltage always switches between V_{Link} / $(m-1)$ and $2V_{Link}$ / $(m-1)$ according to the switching states sequence in Table II, which is $S_{t4} \rightarrow S_{t5} \rightarrow S_{t2} \rightarrow S_{t6} \rightarrow S_{t3} \rightarrow S_{t7} \rightarrow S_4$. Finally, the third range of the duty cycle is $1-(1/(m-1)) \leq D < 1$ or $2/(m-1) \leq D < 1$ as shown in the zoomed-in portion in Fig. 7(e), specifically at $D = 0.8$. In this range, the pulsed four-level staircase voltage always switches between $2V_{Link}/(m-1)$ and V_{Link} according to the switching states sequence in Table II, which is $S_{t7} \rightarrow S_{t8} \rightarrow S_{t5} \rightarrow S_{t8} \rightarrow S_{t6} \rightarrow S_{t8} \rightarrow S_7$.

As shown in Table II and Fig. 7, the four-level staircase voltage (switching voltage V_{SW1}) is synthesized by the zero volt, V_{Link}, and the flying capacitor voltages as shown in the equivalent circuits for the eight switching states. One can tell the level count from the staircase voltage in Fig. 7(b)(bottom) by counting each voltage level including the zero voltage level.

The pulse frequency of the m-level staircase voltage is $(m-1)$ times the switching frequency of each switch, as seen in the zoomed-in portions of Fig. 7(c)-(e). The L_1C_1 filter filters the m-level (4-level in this case) staircase voltage to obtain a clean rectified sinusoidal voltage at the unfolder's input at node V_{uf}.

The unfolder is a full-bridge unfolding circuit. The pair of switches S_{uf1} and S_{uf2} is complementary to the pair of switches S_{uf3} and S_{uf4}. The gating signals of the unfolder switches are generated by comparing an AC sinusoidal reference (Vac_r) to the zero. This AC sinusoidal reference is synchronized with the full-wave rectified sinusoidal reference (Vr_{uf}) as shown in Fig. 8. If the AC sinusoidal reference is greater than zero, the unfolder switches, S_{uf1} and S_{uf2} , turn ON. If the AC sinusoidal reference is less than zero, the unfolder switches, S_{uf3} and S_{uf4}, turn ON. After filtering the four-level staircase voltage, V_{SW1}, by the L_1 C_1 filter, this full-bridge unfolder unfolds the clean rectified sinusoidal voltage at the node V_{uf} every $1/2f_{line}$ of a second to generate a nearly pure AC voltage (V_{ac}) at the AC Port-2, as shown in Fig. 8.

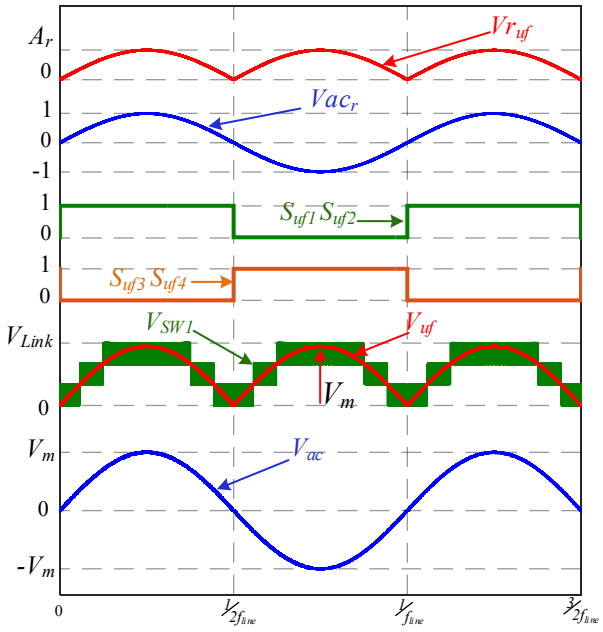


Fig. 8 The unfolder switching scheme including the switching voltage V_{SW1}, the clean rectified unfolder's input voltage V_{uf} and the AC voltage V_{ac}.

IV. Hardware Prototypes and Experimental Results

Two hardware prototypes with open-loop control have been built to experimentally verify the proposed multiport converter structure. The first prototype is a GaN-based modular three-port four-level converter, and the second one is a GaN-based four-port four-level converter. Since the two prototypes rely on the natural balancing of the flying capacitor voltages using PSPWM, the number of levels for each flying capacitor multilevel path is chosen to be an even number equal to four. This is because a FCML path with an even number of levels inherently has higher immunity to capacitor voltage imbalance than a FCML path with an odd number of levels [64]. The two prototypes are built with off-the-shelf components, including the high figures of merit low voltage Gallium Nitride (GaN) switches.

A. GaN-based Modular Three-Port Four-level Prototype.

1. *Hardware Design and Component Selection*

This modular three-port four-level converter structure fits various applications, such as battery and photovoltaic (PV) integration into the grid and stand-alone AC load.

The proposed structure has been verified experimentally by building a modular three-port four-level converter prototype consisting of two identical parallel modules. Each module has three ports and two paths, where each path is a four-level FCML topology, as shown in the schematic in Fig. 9. Each module is designed to process a maximum power of 3 kW. The DC-to-AC conversion path is 1 kW, incorporating a full-bridge unfolder circuit to provide the AC voltage [65]. The DC-to-DC conversion path is bidirectional and can process a maximum power of 2 kW [65]. Port-1 and one interface of the two interfaces of each path are linked across the linking capacitor (C_{Link}); the other interfaces of each path are connected to their respective DC and AC port [65].

The port-1 voltage range is between 125 V to 225 V, which is the voltage across the linking capacitor [65]. The range of port-2 voltage is between 85 V_{RMS} to 120 V_{RMS} and can support 50 Hz or 60 Hz line frequencies [65]. Whereas the range of port-3 is between 0 to 200 V [65]. The voltage value of each port is chosen based on the application and its specification [65]. The

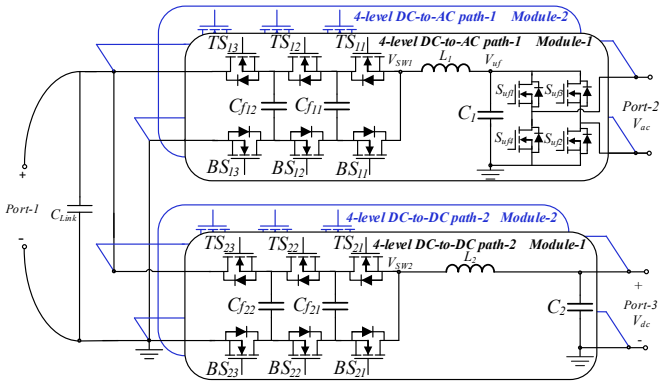


Fig. 9 Modular three-port four-level FCML converter schematic.

two paths and the linking capacitor allow the power to flow between the three ports. It should be mentioned that because the three ports are decoupled, the operation of the three-port four-level converter is not impacted if one port source is not connected or fails[65].

Annotated photographs of the prototype's single module top, bottom, and profile views are shown in Fig. 10, and a photo of the modular prototype with two modules connected in parallel is shown in Fig. 11.

The number of levels in this design is chosen to be four, m = 4; therefore, each flying capacitor multilevel path has $2(m-1)$ or six switches. With V_{Link} designed to be 225 V in this prototype, the nominal blocking voltage of each switch according to (1) is a fraction of the linking voltage equal to V_{switch} or 75 V. However, with ΔV_{cf} chosen to be 9.3 % of V_{switch}, each switch should be selected to block the maximum voltage according to (9) of $V_{SW,max}$ or 82 V.

The switches used in this prototype are the 200 V GaN switches from EPC, EPC2034C, that are well above the maximum blocking voltage and have advanced figures of merit compared to their silicon MOSFET counterparts.

The low-side gate drivers from Texas Instruments, LM5114, are used to drive the GaN switches. The gate drivers must be supplied with isolated DC supplies for functional and protection purposes. The required isolated supplies for each gate driver are obtained via isolated DC-DC converters from Analog Devices, ADUM5210 [42]. Furthermore, the PWM signals are isolated using digital isolators from Silicon Labs, SI8423BB-D-IS. A simplified schematic atop a photo of a portion of the hardware prototype for the complementary top and bottom GaN switches and their driving circuitry, including the decoupling capacitors, is shown in Fig. 12.

This prototype operates at a high switching frequency of 120 kHz, thanks to the GaN switches. Fast transitions between ON and OFF states are implemented to minimize the overlapping losses, especially when operating at such a high switching frequency [42], [43]. The PCB layout and component placement

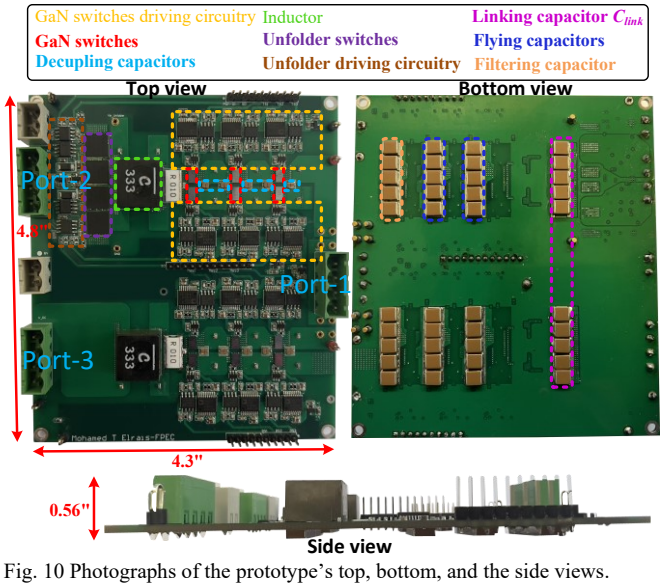


Fig. 10 Photographs of the prototype's top, bottom, and the side views.

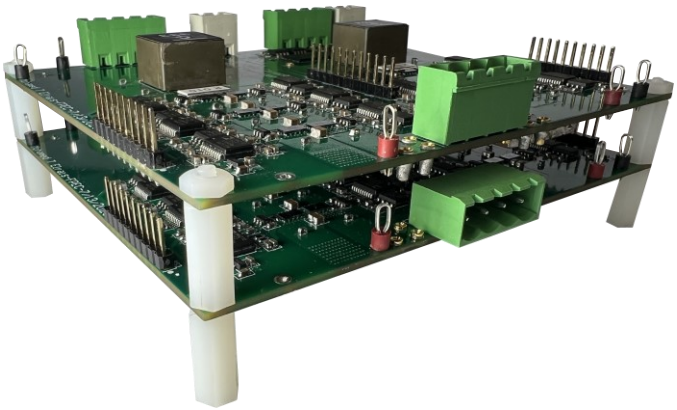


Fig. 11 Photograph of two modules connected in parallel.

are carefully designed to achieve compact size, minimize all loops as much as possible, route the current return paths of all the PWM signal's tracks right below them, and reduce the commutation loops and the PCB parasitic inductance, which minimizes the drain-source voltage ringing resulting from the fast transitions. To further reduce the commutation loops, parasitic inductance, and ringing during GaN switches' ON/OFF fast transitions, small decoupling capacitors that have low parasitic inductance are placed as close as possible to the complementary switches in parallel with the main flying capacitors to minimize the commutation loop [42], [43], [65], as depicted in Fig. 12. The selected decoupling capacitors are the 47 nF capacitors from TDK, C2012X7T2W473K125AE.

The deployment of the four-level FCML as a power conversion path gives the advantage of increasing the frequency seen by the inductors according to (3), which is three times the switching frequency of each switch or 360 kHz. It also decreases the voltage across the inductors three times, which is equal to V_{actual} or 75 V, resulting in a low required inductance of 33.6 µH. This inductor value is designed to ensure that the inductor current ripple is always below its designed maximum value of 1.55 A. The inductor value can be calculated using (2) when D_{actual} = 0.5, V_{actual} = 75 V and f_{actual} = 360 kHz, or using (6), when m = 4, V_{Link} = 225 V, and f_s = 120 kHz.

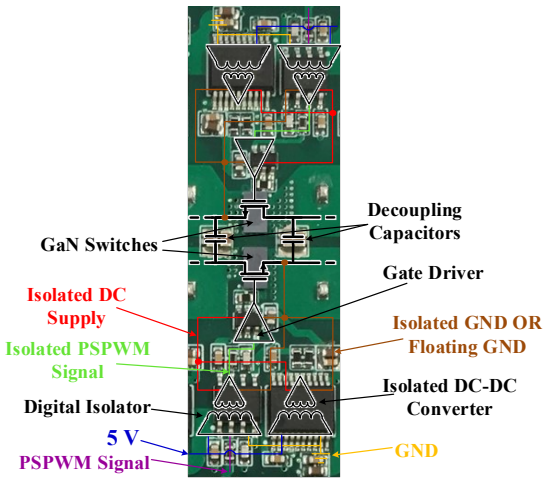


Fig. 12 A simplified schematic over a photo of a portion of the hardware prototype for the complementary top and bottom GaN switches and their driving circuitry, including the decoupling capacitors.

Off-the-shelf composite inductors are the selected solution for this prototype owing to the inductor's low inductance and high-frequency operation. The composite inductors have several additional advantages: they have a slow saturation even at high currents[49]; they are cubic, compact, and low profile, which is ideal for high-density PCB[49]; their cost is low because of their low-cost iron powder material and large production volume; and they are efficient at high-frequency operation[49]. The inductors deployed for each path are 33 µH composite inductors from Coilcraft, XAL1510-333MED[65]. This inductor value is the closest value to the designed value of 33.6 µH, found in any of the off-the-shelf composite inductors. It results in a maximum inductor current ripple of 1.58 A, which is acceptable.

In the FCML paths, although energy is partially transferred by the inductors, the main energy transfer is via the capacitors. As shown in Fig. 9, each four-level FCML path has two flying capacitors, C_{f11} and C_{f12}, for the first path (DC-to-AC path) and C_{f21} and C_{f22} for the second path (DC-to-DC path).

According to (8), the voltages V_{Cf11} and V_{Cf21} are equal to 75V, and the voltages V_{Cf12} and V_{Cf22} are equal to 150 V. As discussed earlier, the flying capacitor voltage ripple ΔV_{Cf} is a design criterion that should be within the range of $0 < \Delta V_{Cf} < V_{Link}/(m-1)$. In this design, it is chosen to be 7 V.

Using the capacitors voltage ripple $\Delta V_{Cf} = 7$ V, the switching frequency f_s = 120 kHz, the number of levels m = 4, and with the DC load current I_{load} = 10 A for the DC-to-DC path or peak load current I_{load} = 11.74 A_{peak} for the DC-to-AC path, the flying capacitor capacitance's value is designed according to (12) and found to be 4 µF for the DC-to-DC path and 4.7 µF for the DC-to-AC path.

The capacitors selected for the flying capacitors are the 2.2 µF TDK, C5750X6S2W225K250KA, multilayer ceramic capacitors. They were chosen based on their high energy density [41], [66], and placed on the bottom side of the PCB. According to the datasheet for these ceramic capacitors, 2.2 µF is the capacitance value at zero bias. However, this capacitance value deteriorates with DC bias; it decreases 31.4 % at 75 V and 56.3 % at 150 V, which become 1.51 µF and 0.962 µF, respectively. Therefore, each flying capacitor is configured by several parallel capacitors calculated using their capacitance values at their respective operating DC voltage.

The minimum number of parallel capacitors required for C_{f11} and C_{f12} are 3 and 5, respectively and for C_{f21} and C_{f22} are 4 and 5, respectively. In this hardware, the five parallel capacitors configuration that results in 4.81 µF is chosen to construct all four flying capacitors to ensure that the voltage ripple will be within the designed limit. According to the datasheet, the equivalent series resistance, ESR, for a single capacitor at 120 kHz is 5.258 mΩ. This means that the ESR is 1.051 mΩ for a configuration of five capacitors in parallel. Table III illustrates the minimum number of parallel capacitors needed to achieve the designed values.

The full-bridge unfolder operates at a line frequency of 60 Hz. Therefore MOSFET switches from STMicroelectronics, STL57N65M, are used because they provide sufficient switching speed[65]. The unfolder switches are driven by half-bridge gate drivers from Fairchild, FAN73932MX[42], [47].

TABLE III
MINIMUM NUMBER OF PARALLEL CAPACITORS TO ACHIEVE THE DESIGNED FLYING CAPACITOR VALUES

Parameters	DC-to-AC path		DC-to-DC path	
	C_{f11}	C_{f12}	C_{f21}	C_{f22}
Flying Cap voltages or DC bias	75 V	150 V	75 V	150 V
Caps designed capacitance	4.7 µF	4.7 µF	4 µF	4 µF
TDK Caps value @ DC bias	1.51 µF	0.962 µF	1.51 µF	0.962 µF
Minimum # parallel Caps	4	5	3	5
Total capacitance	6 µF	4.81µF	4.53 µF	4.81µF

All the switches' PWM signals, including the unfolder switches, are generated via a single C2000 Microcontroller from Texas Instruments, TMS320F28379D LaunchPad[65]. The box volume of a single hardware module is 11.6 in^3, excluding the heat sink and the microcontroller. The box dimensions are 4.8 in × 4.3 in × 0.56 in. Table IV summarizes the complete components list for a single module.

2. *Experimental Results*

The PSPWM signals out of the gate drivers of the top switches and the switching voltage, V_{SW2}, for a 0.25 duty cycle are shown in Fig. 13. It validates the simulated waveform in Fig. 6, where V_{SW2} is equal to $V_{Link}/(m-1)$ or 75 V when only one top switch is ON, and zero when all the top switches are OFF. Moreover, it is clear that the actual frequency seen by the inductor in the DC-to-DC path is the frequency of the switching voltage V_{SW2}, which is three times the switching frequency of each switch or 360 kHz. The equal pulse heights of $225/(m-1)$ or 75 V of V_{SW2} clearly indicate that the flying capacitors of the DC-to-DC path are well balanced at their desired voltage values. The well-balanced capacitor voltages are evident in Fig. 14. The voltages across the flying capacitors and the linking voltage are demonstrated for 40 *ms*, and are evenly spaced by an amount of $225/(m-1)$ or 75 V.

The three ports, working simultaneously with the port-1 voltage of 225 V, the port-2 voltage of 120 V_{RMS}, and port-3

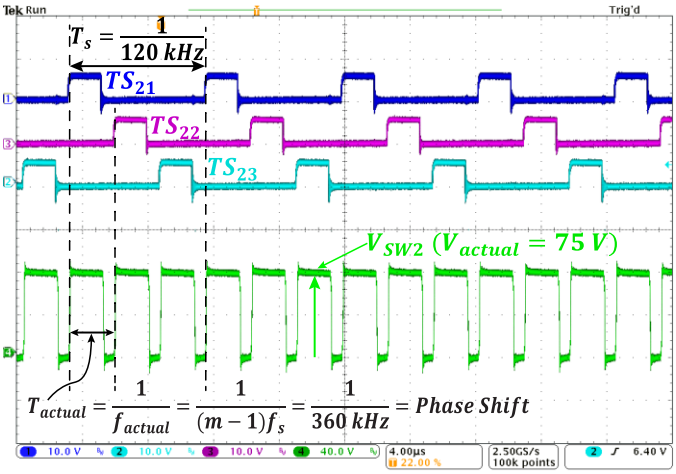


Fig. 13 The gate drivers PSPWM output signals and the pulsed width modulated voltage (switching voltage V_{SW2} in Fig. 9).

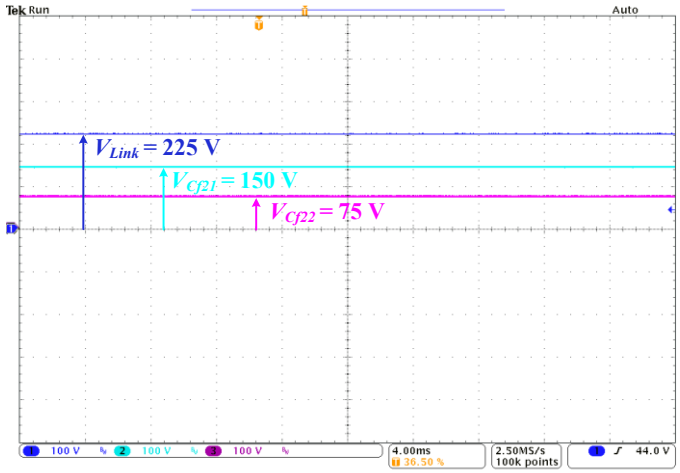


Fig. 14 The linking voltage V_{Link} and the flying capacitor voltages V_{Cf21} and V_{Cf22} of the DC-to-DC path for a period of 40 *ms*.

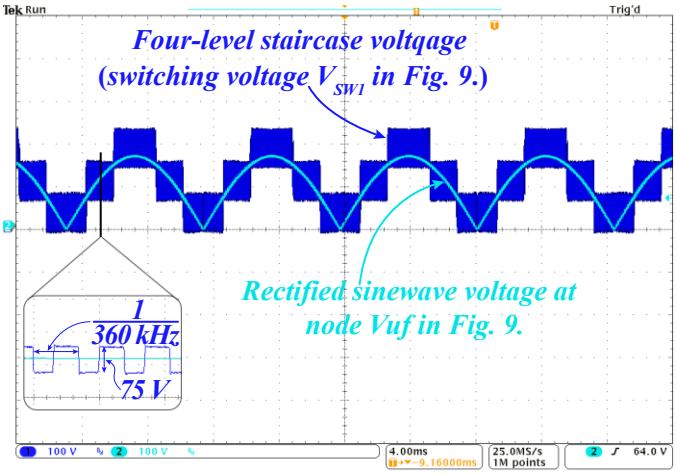


Fig. 16 The four-level staircase voltage at node V_{SW1} and the rectified sinewave voltage at node V_{uf} (annotated in Fig. 9)

voltage of 200 V, including the four-level staircase voltage (switching voltage V_{SW1}), are shown in Fig. 15.

The switches of the DC-to-AC FCML path synthesize the four-level staircase voltage. Then, a clean rectified sine wave with a peak voltage equal to 170 V_{peak} at node V_{uf} (annotated in Fig. 9) is obtained by filtering the four-level staircase voltage as shown in Fig. 16. Finally, the rectified sine wave voltage is unfolded using the unfolder to get the required 60 Hz 120 V_{RMS} voltage at port-2, as shown in Fig. 15.

The pulse frequency of the four-level staircase voltage is 360 kHz. This results from tripling the 120 kHz switching frequency because of the frequency multiplication effect of the four-level FCML path according to (3), as shown in the zoomed-in portion of Fig. 16. Note that the 360 kHz is the frequency seen by the inductor L_1 in Fig. 9. The equal 75 V step increments of the four-level staircase voltage in Fig. 16 indicate well-balanced voltages across the flying capacitors in the DC-to-AC path[65].

To illustrate the bidirectional capability of the DC-to-DC path, a 36 V supply is connected to port-3 with a 1 to 5 step-up conversion ratio to dispatch power to port-1. The bi-directionality is evident from the negative polarity of the inductor current (i_L) shown in Fig. 17. In addition, the switching voltage V_{SW2} (in Fig. 9.) is shown in Fig. 17 while it is stepping up from 36 V at port-3 to 180 V at port-1.

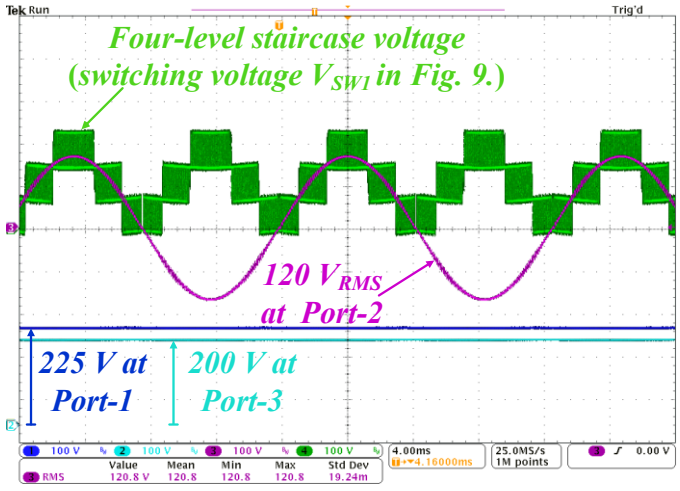


Fig. 15 The voltages of the three ports working simultaneously at Port-1 = 225V, Port-2 = 120 V_{RMS} and Port-3 = 200 V.

The voltage and current of port-2 at 1 kW received from port-1 are shown in Fig. 18. These output voltage and current of 120 V_{RMS} and 8.3 A_{RMS} have clean waveforms very close to a sinusoidal waveform with a Total Harmonic Distortion (THD) of 1.26 % and 1.23 %, respectively. Each DC-to-AC path in each module is conducting 4.15 A_{RMS} that results in the 8.3 A_{RMS} at port-2. Therefore, Fig. 18 demonstrates the operation of the two modules working in parallel, delivering 1 kW to port-2 through the DC-to-AC paths of the two modules. Each module is processing 0.5 kW. The voltage and current of port-2 and the flying capacitor voltages V_{Cf11} and V_{Cf12} of the DC-to-AC path during a current step-up from 1 A_{RMS} to 5 A_{RMS} are shown by Fig. 19. Despite open loop control, the effect of the change in load current on all voltages is insignificant, and the flying capacitor voltages are still balanced and stable. The voltage drop in port-2's voltage after the current step-up is only 3 V.

Fig. 20 shows that the transient occurring in one port does not impact the other ports of the converter. Specifically, this is

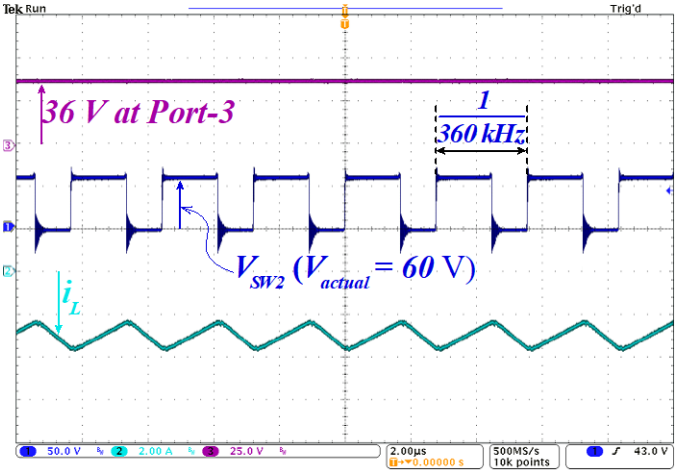


Fig. 17 Port-3 voltage, switching voltage V_{SW2} (annotated in Fig. 9.), and the inductor current in the DC-to-DC path in a 36 V to 180 V step-up operation.

TABLE IV
THE COMPONENT LIST OF THE THREE-PORT FOUR-LEVEL HARDWARE PROTOTYPE

Component	Part number	Specifications
GaN switches	EPC2034C	GANFET, N-Channel, 200 V, 48 A, 8 mΩ
GaN switches gate drivers	LM5114BMF/NOPB	
Decoupling Capacitors	C2012X7T2W473K125AE	47 nF, 450 V
Isolated dc-to-dc supplies	ADUM5210CRSZ	
Digital isolators	SI8423BB-D-IS	
Flying capacitors	C5750X6S2W225K250KA	2.2 µF, 450 V, ESR at 120 kHz is 5.258 mΩ
Inductors	XAL1510-333MED	33 µH, 16.7 A
Unfolder switches	STL57N65M	MOSFETs N-Channel 650 V, 22.5A, 69 mΩ
Unfolder switches gate drivers	FAN73932MX	
Microcontroller	TMS320F28379D	

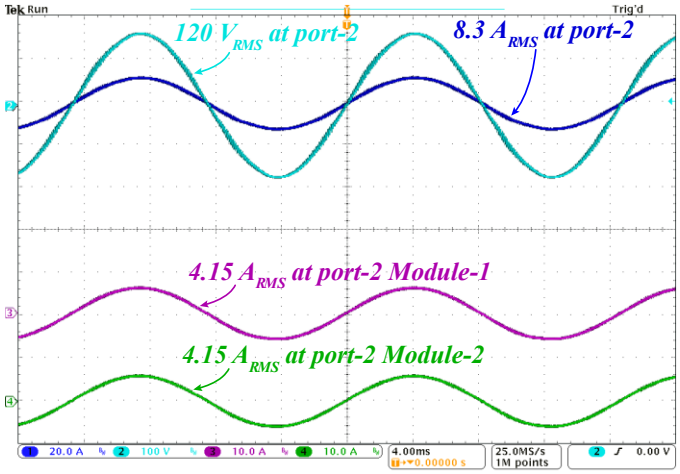


Fig. 18 The voltage and current of 120 V_{RMS} and 8.3 A_{RMS} of port-2 at 1 kW received from port-1.The two modules working in parallel and processing 1 kW, 0.5 kW processed by each module.

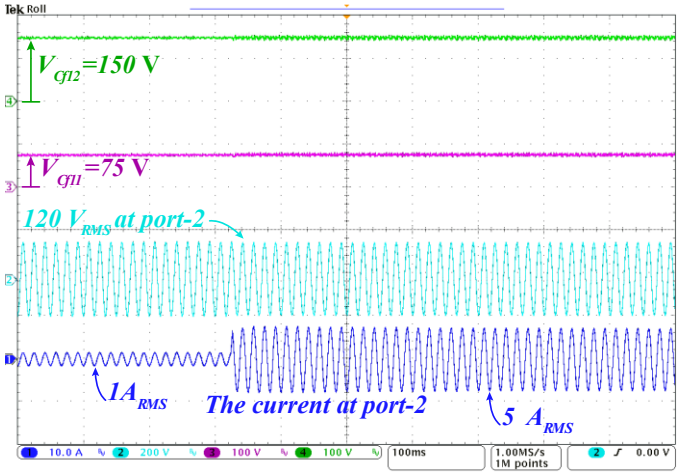


Fig. 19 Port-2 voltage and current and the flying capacitor voltages of the DC-to-AC path during a load step-up from 1 A_{RMS} to 5A_{RMS}.

demonstrated by using Port-1 as an input port that sends power to Port-2 and Port-3. Port-2 is drawing a current of 1A_{RMS} during a step increase in the current drawn by Port-3 from 1A to 4A. The result of this test indicates that the step increase in the current of Port-3 has no impact on the current drawn by Port-2.

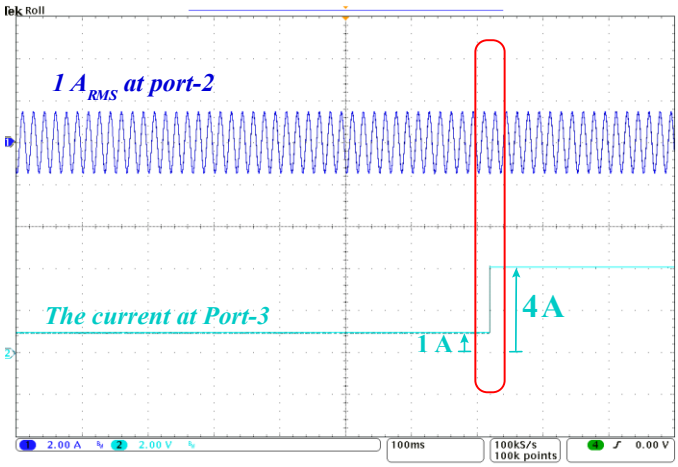


Fig. 20 Port-2 current of 1 A_{RMS} and Port-3 current during step up from 1A to 4A to show that the transient in one port does not impact the other ports.

The YOKOGAWA PZ4000 power analyzer is used to measure the efficiencies of the two conversion paths for a single module. The measured data is plotted in Fig. 21. It is clear from Fig. 21 that the DC-to-AC conversion path's peak efficiency, η_{12}, from port-1 to port-2, when their operating voltages are 225 V and 120 V_{RMS} respectively, is 98.2%, which occurs at 500 W. The DC-to-DC conversion path's peak efficiency, η_{13}, from port-1 to port-3, when their operating voltages are 225 V and 200 V, respectively, is 99.43 %, occurring at 990 W. The light load efficiencies at about 50 W are 90 % for η_{12} and 93.1 % for η_{13} without any light load control.

The specifications for a single module three-port four-level converter prototype are given in Table V. A single module three-port converter was tested at full load power by dispatching

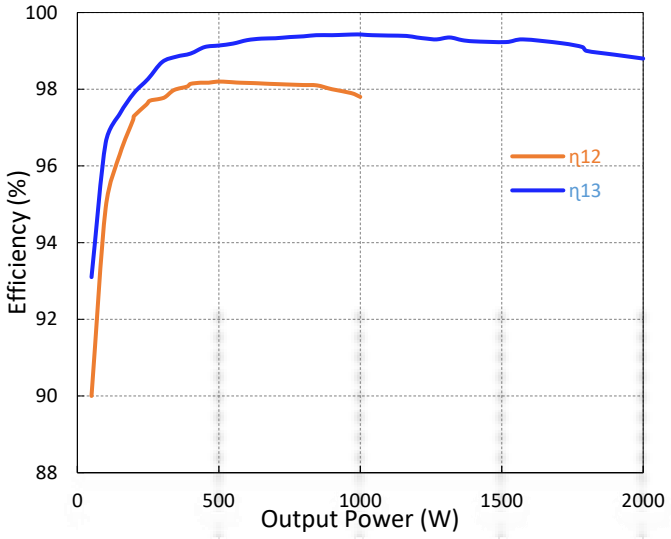


Fig. 21 The individual experimental efficiency curves of both paths: the DC-to-AC path efficiency (η_{12}) and the DC-to-DC path efficiency (η_{13}).

3 kW from port-1 through the two paths where port-2 receives 1 kW and port-3 receives 2 kW. Therefore, using this tested power of 3 kW with the converter box dimensions of 4.8 in × 4.3 in × 0.56 in (12.2 cm × 10.9 cm × 1.44 cm), the tested power density for a single module is found to be 285.6 W/in^3 (15.7 W/ cm^3), excluding the heatsink and the microcontroller.

TABLE V
THE THREE-PORT FOUR-LEVEL CONVERTER SINGLE MODULE SPECIFICATIONS

Specifications	Tested Value
V_{Link}	225 V
Port-1 voltage	225 V
Port-2 voltage	120 V_{RMS}
Port-3 voltage	200 V
Port-1 power	3 kW
DC-to-AC path / Port-2 power	1 kW
DC-to-DC path / Port-3 power	2 kW
Switching frequency (f_s)	120 kHz
Actual frequency (f_{actual}) (seen by inductors)	360 kHz
THD of Port-2 voltage	1.26 %
THD of Port-2 current	1.23 %
Peak DC- to-AC path efficiency, η_{12} at 500 W	98.2 %
Peak DC- to-DC path efficiency, η_{13} at 990 W	99.43 %
Hardware dimensions excluding heatsink and microcontroller	4.8 in ×4.3 in ×0.56in
Hardware box volume excluding heatsink and microcontroller	11.6in^3 (191.5 cm^3)
Overall power density excluding heatsink and microcontroller	258.6 W/ in^3

B. GaN-based Four-Port Four-level Prototype.

1. Hardware Design and Component Selection.

Another variation of the proposed structure that has been verified experimentally is the GaN-based four-port four-level converter[67]. The four-port four-level converter can be used in various applications such as AC-grid integration with Photovoltaic, Energy Storage, and Electric Vehicles.

As illustrated in the schematic of Fig. 22, there are four ports and three paths, and each path is a four-level FCML topology. The four-port four-level converter is designed to process a maximum power of 5.7 kW through one 1.7 kW DC-to-AC FCML path and two identical 2 kW DC-to-DC FCML paths. The range of AC port-2 voltage is between 85V_{RMS} to 260 V_{RMS} and can support 50 Hz or 60 Hz line frequencies. Whereas the DC ports 3 and 4 voltages ranges are between 0 to 400 V. Finally, the DC port-1 voltage range is between 125 to 450 V. Each port's voltage value is chosen based on the application and its specification [67].

Fig. 23 shows annotated photographs of the GaN-based four-port four-level hardware prototypes' top, bottom, and profile views[67].

The number of levels in this design is chosen to be four, m = 4; therefore, each flying capacitor multilevel path has 2(m – 1) or six switches. With V_{Link} chosen to be 425 V in this prototype, the nominal blocking voltage of each switch according to (1) is 141.7 V. However, with ΔV_{Cf} chosen to be 7 % of V_{switch}, each switch should be selected to block the maximum voltage according to (9) of $V_{SW,max}$ or 151.6 V. The switches used in this prototype are the 200 V GaN switches from EPC, EPC2034C and are driven by the Low-side gate drivers from Texas Instruments, LM5114. Isolated supplies, ADUM5210, have been used to supply the required floating sources to each gate driver, and SI8423BB-D-IS is used as digital isolators to isolate each switch PWM signal [67].

A switching frequency of 120 kHz is implemented, which is enabled by the GaN switches. Careful layout and small

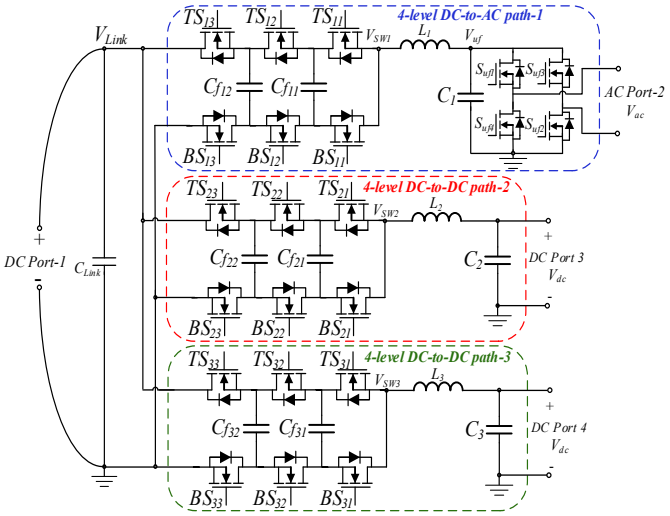


Fig. 22 Schematic for the four-port four-level converter.

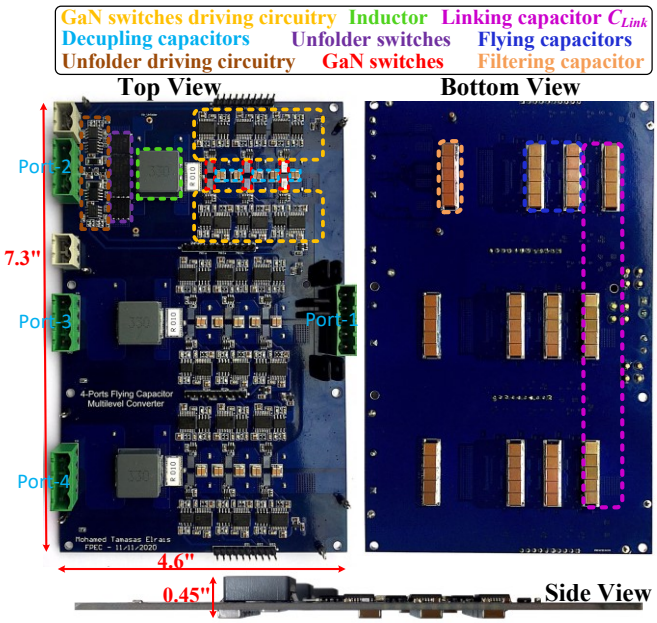


Fig. 23 Annotated photos of the GaN-based four-port four-level hardware prototype's top, bottom, and side views.

decoupling capacitors placed close to the complementary switches are used to reduce ringing during transitions between ON and OFF states[42], [43], [67]. The used decoupling capacitors are 0.047µF KEMET, C1206V473KCRACAUTO [67].

The frequency multiplication effect, which resulted in f_{actual} being 360 kHz according to (3), and the voltage swing reduction across the inductor, which is equal to 141.7 V in this hardware, are two factors that make it possible for each path to have an inductance value as low as 32.8 µH. This inductor value of 32.8 µH ensures that the inductor current ripple is always below its designed maximum value of 3 A. The inductor value can be calculated using (2) when D_{actual} = 0.5, V_{actual} = 141.7 V, and f_{actual} = 360 kHz, or calculated using (6), when m = 4, V_{Link} = 425 V, and f_s = 120 kHz. The inductor that has been used for each path is a 33 µH composite inductor from Laird-Signal Integrity Products, MGV1707330M-10 [67].

Each m-level path has (m – 2) flying capacitors that are two flying capacitors in the four-level case. As shown in Fig. 22, each four-level FCML path has two flying capacitors: C_{f11} and C_{f12} for the first path (DC-to-AC path); C_{f21} and C_{f22} for the second path (DC-to-DC path); and C_{f31} and C_{f32} for the third path (DC-to-DC path). According to (8), the voltages of the first flying capacitors in all paths V_{Cf11}, V_{Cf21}, and V_{Cf31} are equal to 141.7 V. The voltages of the second flying capacitors in all paths V_{Cf12}, V_{Cf22}, and V_{Cf32} are equal to 283.4 V.

According to (12), where ΔV_{Cf} = 10 V, switching frequency f_s = 120 kHz, the number of levels m = 4, and the peak load current I_{Load} = 10 A_{peak} for the DC-to-AC path or DC load current I_{Load} = 5 A for the two DC-to-DC paths, the flying capacitor capacitance's value is calculated to be 2.8 µF for the DC-to-AC path and 1.4 µF for the DC-to-DC paths. The 2.2 µF multilayer ceramic capacitors from TDK, C5750X6S2W225K250KA, are used for the flying capacitors and are placed on the bottom side of the PCB. This capacitance value of 2.2 µF is the capacitance value at zero DC bias. This 2.2 µF deteriorates with DC bias to become 1.01 µF and 0.58 µF at 141.7 V and 283.4 V, respectively. Therefore, each flying capacitor is configured by several parallel capacitors calculated using their capacitance values at their respective operating DC voltage.

The minimum number of parallel capacitors required for C_{f11} and C_{f12} are 3 and 5, respectively. The minimum number of parallel capacitors required for C_{f21} and C_{f31} is 2, and for C_{f22} and C_{f32} is 3. Therefore, the configuration of five parallel capacitors with an equivalent capacitance of 2.9 µF is chosen to construct all of the six flying capacitors to ensure that the voltage ripple will be within the designed limit, and for consistency and robustness. Table VI illustrates the minimum number of parallel capacitors to achieve the designed values.

TABLE VI
MINIMUM NUMBER OF PARALLEL CAPACITORS TO ACHIEVE THE DESIGNED FLYING CAPACITOR VALUES FOR FOUR-PORTS

Parameters	DC-to-AC path		DC-to-DC paths	
	Cf_{11}	C_{f12}	C_{f21} & C_{f31}	C_{f22} & C_{f32}
Flying Cap voltages or DC bias	141.7 V	283.4V	141.7 V	283.4 V
Caps designed capacitance	2.8 µF	2.8 µF	1.4 µF	1.4 µF
TDK Caps value @ DC bias	1.01µF	0.58 µF	1.01 µF	0.58 µF
Minimum # parallel Caps	3	5	2	3
Total capacitance	3.03 µF	2.9 µF	2.02 µF	1.74 µF

The switches used for the full-bridge unfolder are MOSFETs from STMicroelectronics, STL57N65M. They switch at a line frequency of 60 Hz. The unfolder switches are driven by half-bridge gate drivers from Fairchild, FAN73932MX [67].

TI C2000 Microcontroller, TMS320F28379D LaunchPad, was used to generate all the PWM signals, including the unfolder switches [67]. The complete components list is summarized in Table VII

The hardware prototype box dimensions are 7.3 in × 4.6 in × 0.45 in, resulting in a box volume without a heat sink and the microcontroller of 15.1 in^3.

2. *Experimental Results*

The converter is tested at a DC port-1 voltage of 425 V (which is also the voltage of the linking capacitor), an AC port-2 voltage of 240 V_{RMS},, and 400 V at both DC port-3 and DC port-4. It can be seen in Fig. 24 that the four ports are working simultaneously at different voltages of 425 V at the DC port-1, 240 V_{RMS} at the AC port-2, 48 V at DC port-3, and 400 V at DC port-4. Therefore, depending on the application for which this four-port converter will be used, all of the four port voltages can be adjusted to work at any combination of voltages within the designed voltage range of each port.

In the DC-to-AC path, a four-level staircase voltage (switching voltage, V_{SW1}, in Fig. 22) is generated and then filtered to get a clean rectified sinusoidal voltage with a peak voltage equal to 339.5 V_{peak} at node V_{uf}. It is then unfolded to give the AC voltage at the AC port-2. These two voltages V_{SW1} and V_{uf} are shown in Fig. 25. The well-balanced voltages across

TABLE VII
THE COMPONENT LIST OF THE FOUR-PORT FOUR-LEVEL HARDWARE PROTOTYPE

Component	Part number	Specifications
GaN switches	EPC2034C	GANFET, N-Channel, 200V, 48A, 8 mΩ
GaN switches gate drivers	LM5114BMF/NOPB	
Decoupling Capacitors	C1206V473KCRACAUTO	0.047μF, 500V
Isolated dc-to-dc supplies	ADUM5210CRSZ	
Digital isolators	SI8423BB-D-IS	
Flying capacitors	C5750X6S2W225K250KA × 5	2.2 μF, 450V
Inductors	MGV1707330M-10	33μH, 20A
Unfolder switches	STL57N65M	MOSFETs N-Channel 650 V, 22.5A, 69 mΩ
Unfolder switches gate drivers	FAN73932MX	
Microcontroller	TMS320F28379D	

the flying capacitors in the DC-to-AC path are evident from the equal 141.7 V step increments of the staircase voltage waveform in Fig. 25. Moreover, the pulse frequency of the staircase voltage is 360 kHz, which is the same frequency seen by the inductor. Fig. 25 shows the output voltage and current of the AC port-2 of 240 V_{RMS} and 7.1 A_{RMS} at 1.7 kW. They are almost pure sinusoidal waveforms with THD of 0.78% and 0.71%, respectively.

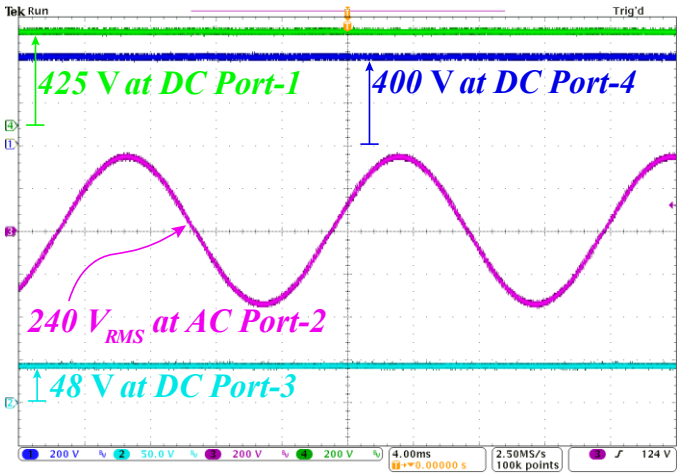


Fig. 24 The four ports working simultaneously, Port-1 = 425 V, Port-2 = 240 V_{RMS}, DC Port-3 = 48 V and Port-4 = 400 V.

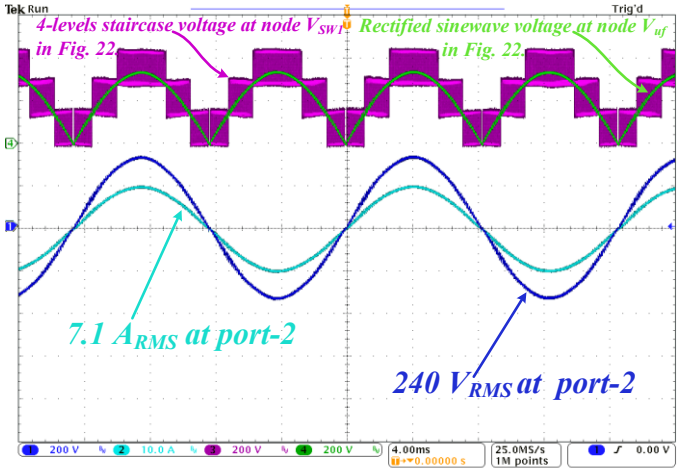


Fig. 25 The four-level staircase voltage (switching voltage, V_{SW1}) and the clean rectified sinewave voltage at node V_{uf}, the output voltage and current of 240 $240V_{RMS}$ and 7.1 ARMS of the port-2 at 1.7 kW(annotated in Fig. 22).

The transient response is verified by stepping up the current from 1A to 4 A, as shown in Fig. 26. During this load step-up, the two flying capacitor voltages Vc_{f21} and Vc_{f22} are stable and balanced at their 141 V and 283 V values, respectively.

The individual efficiency curves of all paths are measured using the YOKOGAWA PZ4000 power analyzer and plotted in Fig. 27. The efficiencies are identified as follows: the DC-to-AC path efficiency from the DC port-1 to the AC port-2 (η_{12}); the DC-to-DC path efficiency from the DC port-1 to DC port-3 (η_{13}); and the DC-to-DC path efficiency from the DC port-1 to the DC port-4 (η_{14}). It is clear from Fig. 27 that the peak efficiency (η_{12}) of the DC-to-AC path, when the DC port-1 and the DC port-2 voltages are 425 V and 240 V_{RMS}, respectively, is 98.2%, which occurs at 1.27 kW. The peak efficiencies of the

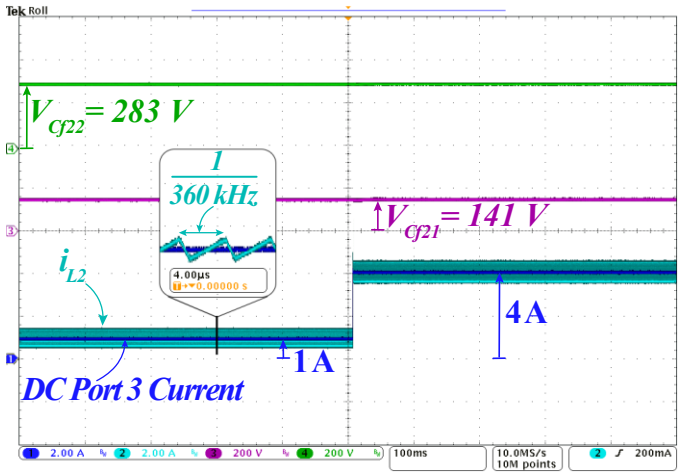


Fig. 26 DC Port-3 current and the flying capacitor voltages of the DC-to-DC path during a load step-up from 1 A to 4 A.

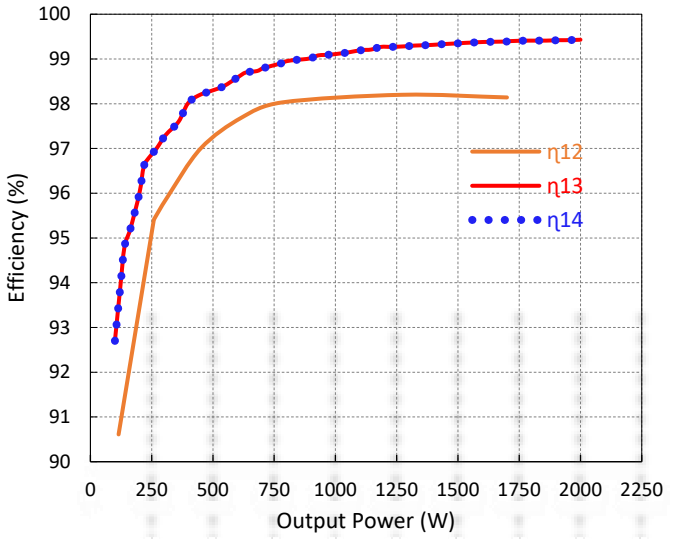


Fig. 27 Measured individual efficiency curves of all paths.

two DC-to-DC paths (η_{13} and η_{14}) are identical and equal to 99.43%, which occur at 2 kW, when the operating voltages of the DC port-1 and both DC port-3 and 4 are 425 V and 400 V, respectively. The efficiencies at a light load of about 100 W are 90.6% for η_{12} and 92.5% for both η_{13} and η_{14} without including any light load control.

Fig. 28 shows a thermal image of the four ports working simultaneously with forced air cooling and without a heat sink while port-1 dispatches 4 kW as follow: 1 kW to AC port-2, 1.5 kW to DC port-3, and 1.5 kW to DC port-4. The hottest spots are the GaN switches with a maximum temperature of 65.8°C which is well below the used GaN switches operating temperature of 150°C. It is also well below the lowest operating temperature among all the other components on the hardware prototype of 125°C. The specifications of the four-port four-level converter prototype are given in Table VIII.

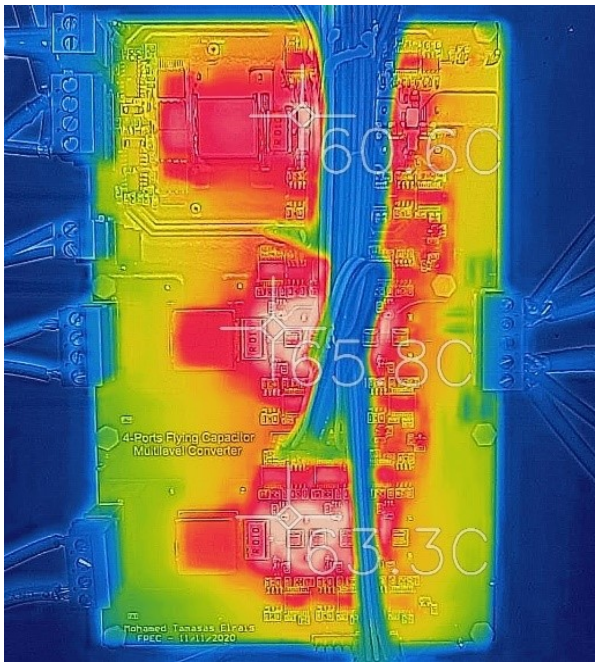


Fig. 28 Thermal image for the three ports working simultaneously while port-1 dispatching 4 kW to the rest of the ports: 1 kW to AC port-2, 1.5 kW to DC port-3 and 1.5 kW to DC port-4.

TABLE VIII
THE CONVERTER SPECIFICATIONS

Specifications	Tested Value	Notes
V_{Link}	425 V	Voltage range 125 V to 450 V
DC Port-1 voltage	425 V	Voltage range 125 V to 450 V
AC Port-2 voltage	240 V_{RMS}	Voltage range 85 V_{RMS} to 260 V_{RMS}
DC Port-3 voltage	400 V	Voltage range 0 to 400 V
DC Port-4 voltage	400 V	Voltage range 0 to 400 V_{DC}
DC Port-1 power	5.7 kW	Power range 0 to 5.7 kW
DC-AC path / AC Port-2 power	1.7 kW	Power range 0 to 1.7 kW
DC-DC path / DC Port-3 power	2 kW	Power range 0 to 2 kW
DC-DC path / DC Port-4 power	2 kW	Power range 0 to 2 kW
Switching frequency	120 kHz	Switching frequency of each switch
Actual frequency seen by the inductors	360 kHz	At the nodes V_{SW1}, V_{SW2}, *and* V_{SW3}
THD of the AC Port-2 voltage	0.78 %	Tested at 1.27 kW
THD of the AC Port-2 current	0.71 %	Tested at 1.27 kW
Peak DC-to-DC paths efficiencies, η_{13} & η_{14}	99.43 %	Peak conversion efficiencies at 2 kW
Peak DC-to-AC path efficiency η_{12}	98.2 %	Peak conversion efficiency at 1.27kW
The converter box volume	15.1 in^3 (246.8 cm^3)	The dimensions excluding the heatsink and the microcontroller are 7.3 in ×4.6 in×0.45 in (18.5 cm × 11.7 cm × 1.14 cm)
Overall power density	377 W/ in^3 (23 W/cm^3)	Measured at 5.7 kW, excluding the heatsink and the microcontroller

The converter box dimensions, excluding the heat sink and the microcontroller, are 7.3 in × 4.6 in × 0.45 in (18.5 cm × 11.7 cm × 1.14 cm).

The total converter box volume is 15.1 in^3 (246.8 cm^3). By using the converter volume and the rated power of 5.7 kW, the overall converter power density, excluding the heat sink and the microcontroller, is 377 W/ in^3 (23 W/cm^3).

V. Conclusion and Future Work

A modular multiport multilevel converter architecture that is applicable for various applications is developed in this paper using FCML topology for its inherent advantages: (1) it reduces the inductor size because of the voltage reduction across the inductors and the frequency multiplication effect seen by the inductors; (2) it reduces the required capacitance because the capacitors charge and discharge at the high switching frequency; and (3) it facilitates the use of the high figure of merits low voltage switches because the switches block only a fraction of the input voltage. In the developed architecture, any combination of AC and DC ports connected through GaN-based FCML paths with any number of levels can be built based on the application and its specifications. The 3 kW, three-port four-level and the 5.7 kW four-port four-level hardware prototypes have been successfully built and tested. Promising experimental results are provided that indicate the potential of the proposed structure with high efficiency and compact designs. In this article, the proposed converter was investigated and verified with open-loop control for a general non-specific application. This article may serve as an initial design to develop and verify this multiport multilevel converter architecture, considering the limitation of the design and control for specific applications.

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