Theoretical, Simulation, and Experimental Comparison of GaN-based Two-level and Multilevel Converters

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***Abstract*—The size, weight, power density, cost, and efficiency are crucial factors that should be considered when designing or employing power electronics converters for a specific application. Therefore, comparing different converters to investigate which converter provides better figures of merit at the same application and operating condition is essential. This paper uses theoretical, simulation and experimental comparisons between the two-level and multilevel converters. The DC-DC two-level buck and the flying capacitor multilevel (FCML) buck converters are chosen to carry out the theoretical, simulation and experimental prototypes when both employ Gallium Nitride (GaN) power semiconductor switches. It was found that the FCML converter inherently provides superior performance and figures of merit over both the two-level and multilevel converters. Simulation and experimental results that validate each other are provided in this paper.**

Keywords—Two-level converter, multilevel converters, high power density, low harmonic distortion, switches blocking voltage, Gallium Nitride switches, GaN.

I. INTRODUCTION

The power electronics converters are needed to perform specific functions to match the loads with the sources, depending on the application. These power electronics converters should be designed and developed with the target of achieving small size, low weight, high power density, high efficiency, low harmonic pollution, and low cost while achieving their desired functions. The limitations of power electronics topologies motivate researchers and designers to develop and improve other topologies that overcome these limitations. As a case in point, the two-level converters are not ideal for medium and high voltage applications since their switches need to block the entire input voltage and using high voltage rating switches is not recommended [1].

Multilevel converters can address this limitation since their switches block only a fraction of the input voltage, as will be discussed in this paper. The multilevel converters are becoming attractive alternatives in various applications such as renewable energy systems [2], motor drives [3], solid-state transformers [4], multiport converters [5]–[7] and on-board chargers (EV)[8].

This paper compares the common two-level and multilevel converters in terms of the quality of the switching voltages that need to be filtered by the LC filter and their switches blocking voltage values that affect the size, weight, power density, cost, and efficiency. Then a detailed comparison between the DC-DC two-level buck converter and the DC-DC FCML buck converter is carried out theoretically, through simulation, and experimentally to clarify how and why the FCML is superior to the two-level buck converter, especially in medium and high voltage applications.

This research is partially funded by NSF-ECCS-2103442.

II. THE TWO-LEVEL CONVERTERS

The two-level converters employ the half-bridge cell as a building block in conjunction with energy storage elements to construct converters for various functions, as shown in Fig. 1 [9]. The bidirectional DC-DC buck and boost converters' power circuit and basic waveforms are shown in Fig. 1(a) and (b), respectively. They are constructed of a single half-bridge cell that contains top and bottom switches, S_T and S_B, that work in a complementary fashion[9]. When S_T is ON and S_B is OFF, S_B blocks the entire input voltage of V_{in} in the case of the buck converter and blocks the entire output voltage V_o for the boost converter. When S_T is OFF and S_B is ON, S_T blocks V_{in} in the case of the buck converter and blocks V_o for the boost converter. Each switch turns ON and OFF once every switching cycle and continuously operates in this way at a switching frequency(f_s). The switching voltages V_{SW} annotated in Fig. 1(a)(b)(top) that needs to be filtered by the inductors have a frequency equal to the switching frequency of each switch. V_{SW} equals V_{in} for the buck and V_o for the boost when S_T is ON and zero for both the buck and the boost when S_T is OFF as shown in the waveforms in Fig. 1(a)(b)(bottom).

The two-level half-bridge, full-bridge, and three-phase DC-AC inverters' power circuit schematic and the basic waveforms are shown in Fig. 1(c - e). They are constructed of a single half-bridge cell, two half-bridge cells, and three half-bridge cells, respectively[9]. These cell's top and bottom switches work in a complementary way with each other to prevent short circuit occurrence across the DC input voltage, V_{in}. The top switches' gating signals have dynamic duty cycles D that change following sinusoidal references to generate switching voltages V_{SW} that follow sinusoidal patterns. For the full-bridge inverter in Fig. 1(d), the sinusoidal patterns of the duty cycles of the top switches of the two cells are out of phase. In the case of three-phase inverter in Fig. 1(e), the sinusoidal patterns of the duty cycles of the top switches of the three cells are shifted from each other 120°. In the half-bridge inverter in Fig. 1(c), two large capacitors are connected in series to split the DC input voltage to provide positive and negative voltages with respect to the neutral to enable AC generation. The switching voltage V_{SW} waveform for the half-bridge inverter is an AC pulse width modulated waveform with a frequency equal to the switching frequency of each switch, f_s, as in Fig. 1(c)(bottom).

Similarly, the frequency of the switching voltages V_{SW1}, V_{SW2} for the full-bridge shown in Fig. 1(d) and V_{SW1}, V_{SW2}, and V_{SW3} for the three-phase shown in Fig. 1(e) are equal to the switching frequency of each switch, f_s. The switching voltage V_{SW} of the half-bridge inverter is equal to V_{in} / 2 when S_T ON and S_B OFF and equal to $-V_{in}$ / 2 when S_T OFF and S_B ON. In the case of the full-bridge and the three-phase inverters, the switching voltages are equal to V_{in} when their respective cells' top and bottom switches are OFF and ON, respectively; they are equal to zero when they are ON and OFF, respectively.

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The AC output voltage before filtering ($V_{o,before}$ in Fig. 1(d)(bottom)) in the full-bridge inverter is generated by the voltage difference between the switching voltages, V_{SW1} and V_{SW2}, of each half-bridge cell.

The AC output voltages V_{AB}, V_{BC}, and V_{CA} are generated by the voltage difference between the switching voltages $V_{SW1} - V_{SW2}$, $V_{SW2} - V_{SW3}$, and $V_{SW3} - V_{SW1}$, respectively.

Finally, an important observation is that all the half-bridge, full-bridge, and three-phase switches block the entire input voltage V_{in} while in the OFF state.

III. The Multilevel Converters

There are three main multilevel converters: cascaded H-bridge (CHB), neutral point diode clamped (NPC), and flying capacitor multilevel (FCML) converters. The CHB inverter is constructed by connecting the outputs of full-bridge cells in series [10]. The number of full-bridge cells, x, that should be connected in series depends on the required number of levels, N, as

$$x = \frac{N-1}{2} \quad (1)$$

Each full-bridge inverter cell, when controlled using unipolar PWM gating signals, generates output voltage with three levels: V_{in}, 0, and $-V_{in}$ [11]. Therefore, to generate output voltage with five levels ($N = 5$), the output voltages of two full-bridge cells must be connected in series according to (1), as shown in the five-level cascaded H-bridge inverter in Fig. 2(a). Each full-bridge requires an isolated DC source for the proper functionality of the inverter. The amplitude of each step in the switching voltage V_{SW} is equal to the entire DC input voltage V_{in} of each full-bridge and switching between two levels of the switching voltage at a frequency equal to the switching frequency of each switch, f_s,which is the frequency seen by the filtering inductor, as shown in the basic waveforms in Fig. 2(a). All switches are required to block the entire input voltage V_{in} while in the *OFF* state.

The five-level NPC inverter shown in Fig. 2(b) is used to show the NPC topology's switching voltage waveform and switches' blocking voltages. The five-level NPC requires (N–1) or four capacitors connected in series to split the DC input voltage, and the voltage across each capacitor is found as [12].

$$V_c = \frac{V_{in}}{N-1} \quad (2)$$

It is constructed of $N - 1$ or four top switches S_{T1}, S_{T2}, S_{T3},and S_{T4}, and $N - 1$ or four bottom switches S_{B1}, S_{B2}, S_{B3}, and S_{B4}. The top and bottom switches in each pair (S_{T1}, S_{B1}), (S_{T2}, S_{B2}), (S_{T3}, S_{B3}), and (S_{T4}, S_{B4}) are switching in a complementary fashion. The amplitude of each step in the switching voltage V_{SW} is equal only to $V_{in}/(N-1)$ or $V_{in}/4$, when $N = 5$, and switching between two levels of the staircase voltage waveform at a frequency equal to the switching frequency of each switch, f_s, which is the frequency seen by the filtering inductor, as shown in the basic waveforms in Fig. 2(b). In addition, all switches block only a fraction of the input voltage equal to the voltage of each capacitor or V_{in} / 4 according to (2).

The number of clamping diodes that are required for the NPC inverter is $2(N - 2)$ or six clamping diodes for the five-level case: three top diodes D_{T1}, D_{T2}, and D_{T3} and three bottom diodes D_{B1}, D_{B2}, and D_{B3}. Depending on the location of the clamping diode, the required blocking voltage across it changes. One of the main disadvantages of the NPC topology is its unbalanced DC link capacitor voltages, which necessitate the inclusion of a balancing circuit.

The five-level FCML inverter shown in Fig. 2(c) is used to highlight the inherited features of the FCML topology that was first introduced in [13]. The DC input voltage is required to be split by at least two capacitors, C_{bus1} and C_{bus2}, to construct the DC bus and give access to a midpoint to be used as the switching voltage V_{SW} neutral point. There are ($N - 2$) or three flying capacitors, C_1, C_2, and C_3, for $N = 5$. The voltage across each of these flying capacitors varies depending on the nodes they are connected to, as follows:

$$V_{cn} = \frac{nV_{in}}{N-1}, \quad \text{where } n \text{ is 1, 2, or 3} \quad (3)$$

Therefore, the flying capacitor voltages are as follow: $V_{C1} = V_{in}/4$, $V_{C2} = V_{in}/2$, and $V_{C3} = 3V_{in}/4$. Thus, flying capacitors with different voltage ratings are required. It can be noticed that there is a voltage difference between every two adjacent flying capacitors that is equal to $V_{in}/(N-1)$ or $V_{in}/4$. This voltage difference between every two adjacent flying capacitors is the voltage that every switch is required to block.

The five-level FCML inverter consists of $2(N - 1)$ or eight switches, four top switches S_{T1}, S_{T2}, S_{T3}, and S_{T4}, and four bottom switches S_{B1}, S_{B2}, S_{B3}, and S_{B4}. The top switches are working in a complementary fashion with the bottom ones. The amplitude of each step in the switching voltage V_{SW} is equal only to $V_{in}/(N-1)$, and switching between two levels at a frequency that ($N - 1$) times greater than the switching frequency of each switch or $3f_s$ and this frequency seen by the filtering inductor, as shown in the basic waveforms in Fig. 2(c).

IV. Comparison Between Two-Level and Multilevel Buck Converters

A comparison between all mentioned converters (two and multilevels) in terms of frequency and pulse height of the switching voltages V_{SW} and the switches' drain-source blocking voltages are summarized in Table I. It is clear from the table that the FCML topology requires the smallest filter size because the switching voltage that needs to be filtered has a frequency higher than the frequency of each switch by a factor of ($N - 1$), and the step height is only a fraction of the input voltage equals $V_{in}/(N-1)$. These two inherited features reduce the size, weight, and cost and increase power density and efficiency. In addition, the FCML switches block only $V_{in}/(N-1)$, which results in lower voltage rating switches that improve the cost and efficiency.

To conduct the comparison between the two-level and the multilevel converters, the DC-DC two-level buck converter shown in Fig. 1(a) is chosen to represent the two-level converters, and the four-level DC-DC FCML shown in Fig. 3 is chosen from the multilevel converters since it provides the highest figures of merit among all types of multilevel converters. The capacitor voltages of the FCML prototype in this paper are passively balanced using phase shifted pulse width modulation (PSPWM)[13]. For this reason, the number of levels is chosen to be an even number equal to four because FCML with even levels provides higher immunity for capacitors imbalance than FCML with odd levels [14].

A. The Switches Blocking Voltage

The switch voltage rating is an essential factor that affects the efficiency because the switching losses approximately proportional to V_{block}^2 / R_{on} [15], where V_{block}^2 and R_{on} are the switch blocking voltage and the drain-source on-resistance of the switch, respectively. Moreover, the switches blocking voltages affect the EMI of the converter because the lower the

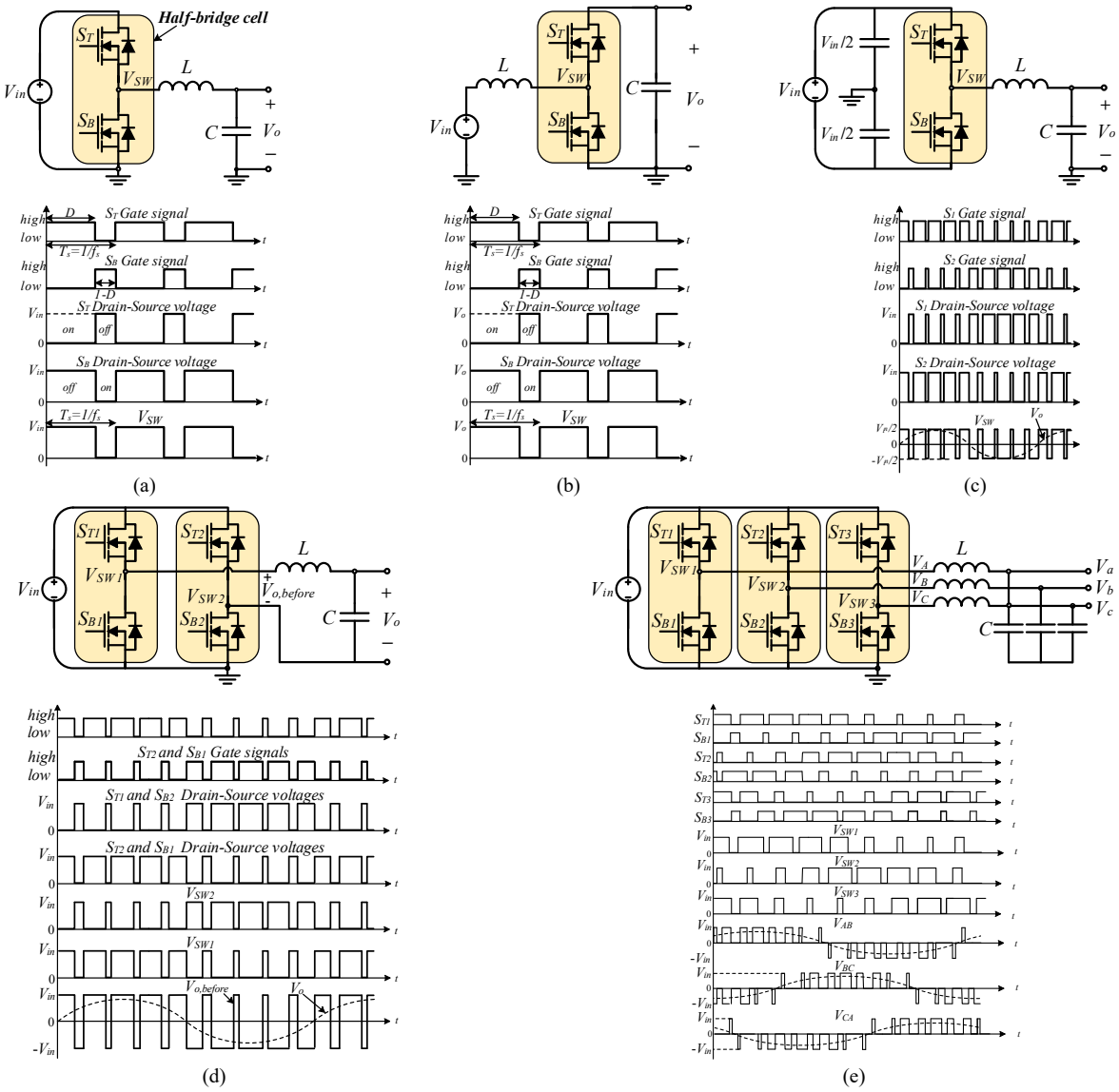

Fig. 1. The two-level converters, (Top) Power circuit schematic, (Bottom) basic waveforms. (a) Two-level DC-DC buck converter (b) Two-level DC-DC boost converter (c) Two-level half-bridge DC-AC inverter (d) Two-level full-bridge DC-AC inverter (e) Two-level three-phase DC-AC inverter.

TABLE I. COMPARISON BETWEEN THE CONVERTERS IN TERMS OF FREQUENCY AND PULSE HEIGHT OF THE SWITCHING VOLTAGES AND THE SWITCHES BLOCKING VOLTAGES.

Topology Type	The Switching Voltage V_{SW} that Needs to be Filtered		The Switches' Drain-Source Blocking Voltage
	Frequency	Pulse/Step Height	
Buck	f_s	V_{in}	V_{in}
Boost	f_s	V_o	V_o
Half-bridge	f_s	V_{in}	V_{in}
Full-bridge	f_s	V_{in}	V_{in}
Three-phase	f_s	V_{in}	V_{in}
CHB Multilevel	f_s	V_{in}	V_{in}
NPC Multilevel	f_s	V_{in} / $(N-1)$	V_{in} / $(N-1)$
FCML Multilevel	$(N-1)f_s$	V_{in} / $(N-1)$	V_{in} / $(N-1)$

switches blocking voltages or the $d_v/\ d_t$ the lower the EMI. As shown in the simulated drain to source voltage (V_{DS}) in Fig. 4(a), each switch in the four-level FCML converter, blocks only $V_{in}/(N-1)$ or 53.3 V when V_{in} = 160 V. This will allow leveraging the high figures of merit low voltage ratings, low R_{on}, high frequency, and more miniature footprint switches and reduce the switching losses significantly. However, in the two-level buck converter, each switch must block the entire input voltage V_{in} as shown in the simulated drain to source voltage in Fig. 4(b), necessitating the employment of the unrecommended high voltage rating switches.

B. *The Inductor Sizing*

The large filtering inductor is one of the main challenges that power electronic converter designers face. In the buck converter, the inductor is sized according to

$$L = \frac{(1-D)\,.\,D.V_{in}}{\Delta i_L\ f_s} \tag{4}$$

where Δi_L is the inductor current ripple.

In comparison, the filtering inductor for the N-level FCML converter is calculated as [16]

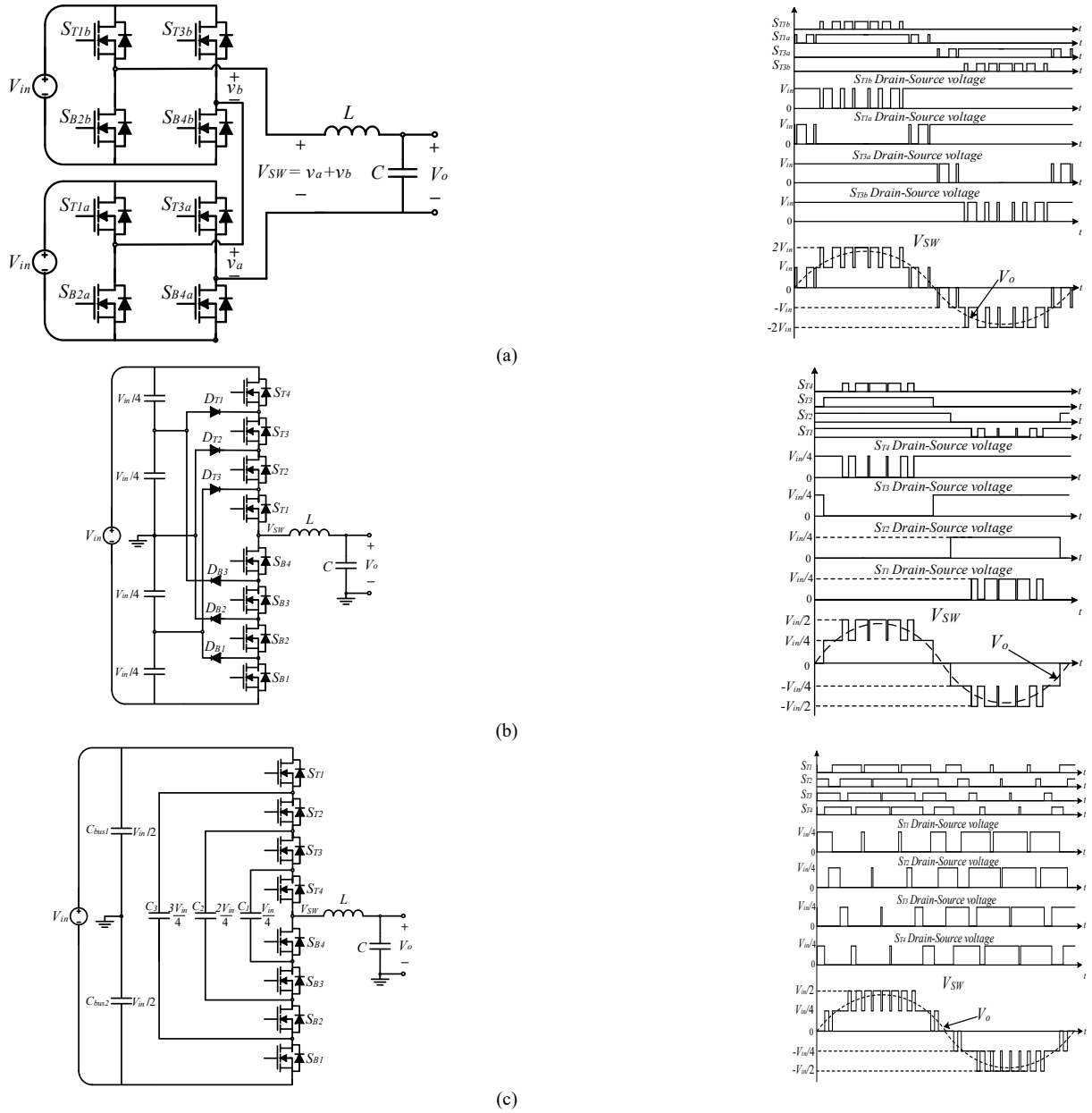

Fig. 2. The multilevel converters (a) CHB five-level inverter (b) The NPC five-level inverter (c) The FCML five-level inverter

$$L = \frac{(1-D_{actual}) \cdot D_{actual} \cdot V_{in}}{\Delta_{i_L} f_S (N-1)^2} \quad (5)$$

where D_{actual} is the actual duty cycle calculated as

$$D_{actual} = (N-1)D - Floor[(N-1)D] \quad (6)$$

When comparing (4) with (5), it is found that the inductor in the N-level FCML is $(N-1)^2$ times smaller than that of the buck converter when both operate at the same input voltage, switching frequency, and inductor current ripple. This $(N-1)^2$ inductor size reduction is because of two factors [16], [17]: the first factor is that the amplitude of the switching voltage (V_{SW}) that needs to be filtered by the inductor is only V_{in} / $(N-1)$, resulting in an inductor voltage (V_L) swing of V_{in} / $(N-1)$, as

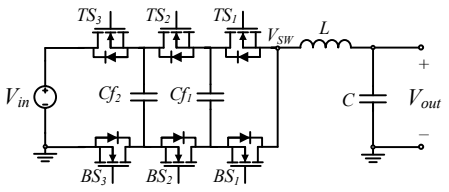

Fig. 3. Bidirectional DC-DC four-level flying capacitor converter.

as shown in Fig. 5(a). In the two-level buck case, the amplitude of the switching voltage that needs to be filtered by the inductor is the entire V_{in}, resulting in an inductor voltage swing equal to V_{in}, as illustrated in Fig. 5(b). The second factor is that the frequency seen by the inductor in the N-level FCML converter is $N-1$ times higher than the switching frequency f_s of each switch; with f_s equal to 120 kHz, the inductor sees 360 kHz as shown in Fig. 5(a). In the two-level buck case, the frequency seen by the inductor is the same as each switch's switching frequency, as shown in Fig. 5(b).

For visualization, (4) and (5) are used to draw the inductor inductance of the four-level FCML and the two-level buck converter normalized to the inductance of the buck converter against the duty cycle at a fixed V_{in}, Δ_{iL}, and f_s, which is shown in Fig. 6.

C. The Capacitor Sizing

The buck converter has no flying capacitors, and the energy transfer is mainly done by the inductor. However, there are $(N-2)$ flying capacitors in the N-level FCML converter

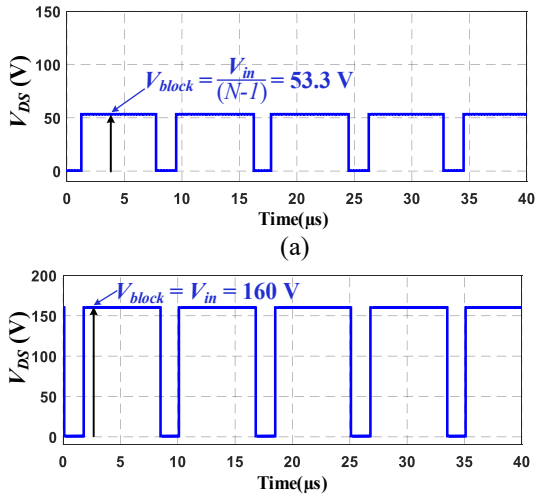

Fig. 4 (a) The switch drain-source voltage in the four-level flying capacitor converter (b) The switch drain-source voltage of the buck converter.

(two flying capacitors for $N = 4$), which are the main energy transfer elements along with partial energy transferred by the inductor. Since the capacitors inherently have 2-3 orders of magnitude higher energy density (energy storage capability per unit volume) than inductors[18], the total passive component volume of the N-level FCML converter can be decreased, yielding improved power density compared to the buck converter that depends mainly on the inductor.

Moreover, the flying capacitors are charging and discharging at the switching frequency, which reduces the capacitors' energy storage requirement, resulting in minimal flying capacitors values[16], [17]. The flying capacitors do not increase the complexity of the FCML converter because the capacitor voltages are naturally balanced at their desired value when the FCML converter is controlled using the PSPWM modulation[13].

D. The Losses and Heat Dissipation

Although the N-level FCML converter has $2(N-1)$ switches, $(N-1)$ top switches, and $(N-1)$ bottom switches, which is six in the four-level case compared to two switches for the two-level buck converter, the total conduction and switching losses of both converters can be designed to be the

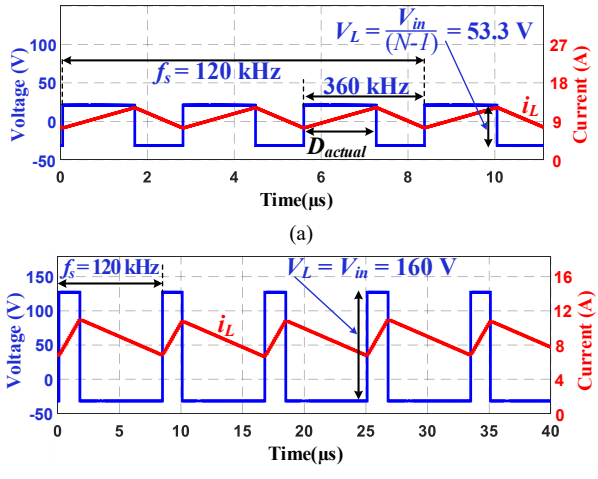

Fig. 5. (a) The inductor voltage and current of the four-level flying capacitor converter. (b) The inductor voltage and current of the buck converter

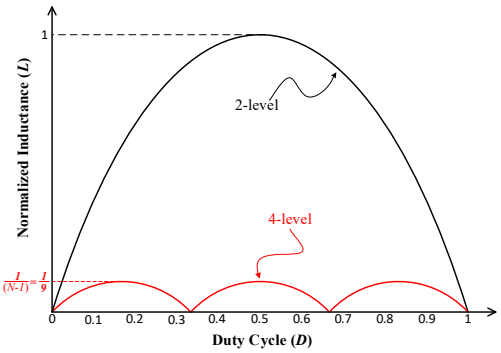

Fig. 6. The normalized inductor inductance vs duty cycle D for the two level buck and four-level FCML with equal switching frequency, input voltage, and inductor current ripples.

same [19]. The conduction losses of the N-level FCML and the buck converters can be made the same as follows: there are always $(N-1)$ or three switches conducting in series at all times because the top and bottom switches of the N-level FCML converter are working in a complementary manner. In comparison, only one switch is always conducting in the buck converter. Therefore, if R_{on} is the drain-source on-resistance of the buck converter switches, then by choosing the on-resistance of the N-level FCML converter switches to be $R_{on}/(N-1)$, then $(N-1)$ switches conducting in series result in an equivalent resistance equal to R_{on}, and hence the conduction losses of both converters will be equal [19].

The switching losses of the N-level FCML and the buck can be made the same as follows: as mentioned in section IV *A*, the switching loss of each switch is approximately proportional to V_{block}^2 / R_{on}. Therefore, to make it clear that both the buck and the N-level FCML have the same switching losses, the total switching losses of the two switches of the buck converter should be equal to the total switching losses of the $2(N-1)$ (six switches when $N = 4$) switches of the N-level FCML converter. There are two switches in the buck converter: each has an on-resistance equal to R_{on}; each must block the entire input voltage V_{in}; and each one switches at the switching frequency of f_s. Thus, the total approximate switching losses of the buck converter can be found by

$$P_{sw_{loss}} = \sum \frac{V_{block}^2}{R_{on}} f_s = 2 \frac{V_{in}^2}{R_{on}} f_s \qquad (7)$$

where $P_{sw_{loss}}$ is the total switching losses.

On the other hand, there are $2(N-1)$ switches in the N-level FCML: each chosen to have an on-resistance equal to $R_{on}/(N-1)$; each blocks a voltage of $V_{in}/(N-1)$; and each one switches at a switching frequency of f_s. Thus, the total approximate switching losses of the N-level FCML can be found as

$$P_{sw_{loss}} = \sum \frac{V_{block}^2}{R_{on}} f_s = 2(N-1) \frac{(N-1)}{R_{on}} \cdot \frac{V_{in}^2}{(N-1)^2} f_s \qquad (8)$$

After simplifying (8), it is clear that it equals (7). Therefore, the buck converter and the N-level FCML can be designed to have the same total switching losses [19].

Moreover, the total switching and conduction losses are spread out over $2(N-1)$ or six switches for the four-level FCML converter compared to two switches for the buck; therefore, the heat will be distributed between $2(N-1)$ switches resulting in lower operating temperature per switch, more area for heat dissipation and improved thermal

management. It should be noted that the lower operating temperature of the switches will improve the reliability as it is known that reliability is inversely proportional to the square of the temperature.

V. The Experimental Results

Both converters are working at a high switching frequency of 120 kHz, thanks to the GaN switches. The inductor voltage and current of the two-level buck converter are shown in Fig. 7. It is clear that the frequency seen by the inductor is the same as the switching frequency of each switch which is 120 kHz and the inductor needs to filter a voltage with an amplitude equal to the entire input voltage of 160 V.

However, the inductor voltage and current of the four-level FCML shown in Fig. 8 indicate that the frequency seen by the inductor is ($N-1$) times or three times the switching frequency of each switch which is 360 *kHz*. The inductor needs to filter a voltage with an amplitude equal only to $V_{in}/(N-1)$ or 54 V. In addition, Fig. 8 demonstrates the FCML bi-directionality as it is clear from the negative inductor current polarity.

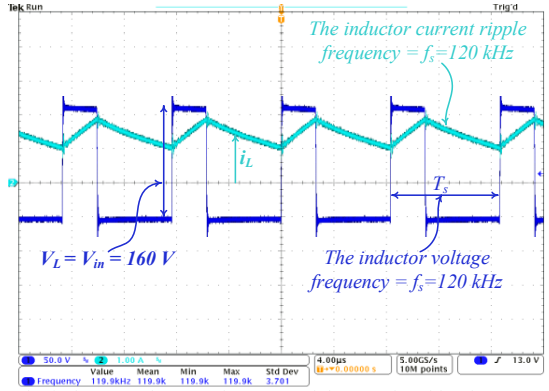

Fig. 7. The inductor voltage and current of the two-level buck converter.

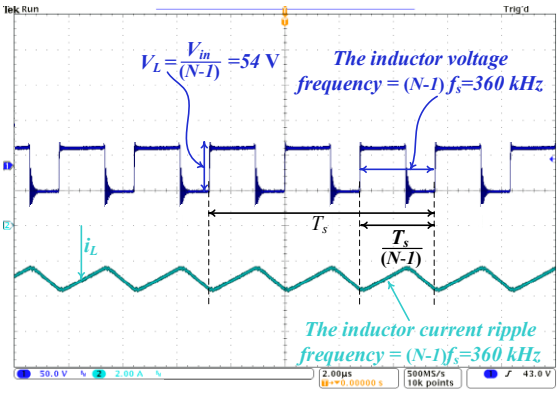

Fig. 8. The inductor voltage and current of the four-level FCML converter.

VI. Conclusion

A comparison is carried out between the common two-level and multilevel power electronics topologies. First, the comparison is conducted between all converters in two qualities: the switches' drain-source blocking voltages and the switching voltages in terms of their frequency and pulse/step highs. These two qualities affect the choice of employing high or low voltage rating switches and the specification of the LC filter and hence affecting the converters' size, weight, power density, cost, and efficiency. Second, a detailed comparison is carried out between the two-level buck converter as a representative for the two-level converters and the FCML because it was found that it provides superior figures of merit among the other multilevel converters; the comparison is conducted in the following qualities: switches blocking voltages, the inductors sizing, the capacitors sizing, and the losses and heat dissipation. The comparison is done theoretically, via simulation, and experimentally and it was found and clarified why the FCML buck converter provides superior performance over the two-level converters.

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