A method for achieving sub-2nm across-wafer uniformity performance

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ABSTRACT

Reducing process development time and speeding up time to market are perennial challenges in the microelectronics industry. The development of etch models that permit optimizations across the wafer would enable manufacturers to optimize process design flows and predict process defects before a single wafer is run. The challenges of across-wafer uniformity optimizations include the large variety of features across the wafer, etch variations that occur at multiple scales within the plasma chamber, feature metrology, and computationally expensive model development. Compounding these challenges are trade-offs between data quality and time/cost-effectiveness, the disparity of information provided by different measurement tools, and the sparsity and inconsistency of human-collected data.

We address these challenges with a feature and wafer level modeling approach. First, experiments are conducted for a variety of etch conditions (e.g., pressure, gas composition, flow rate, temperature, power, and bias). Second, a feature level model is calibrated at multiple sites across the wafer based on OCD and/or cross-sectional SEM measurements. Finally, the calibrated model is used to predict an optimal set of process conditions to preserve uniformity across the wafer and to meet recipe targets.

We demonstrate the methodology using SandBox Studio™ AI for a FinFET application. Specifically, we show the rapid and automated calibration of feature level models using experimental measurements of the 3D feature etch at a variety of process conditions. Automated image segmentation of X-SEM data is also performed here for single case using Weave® to demonstrate how such data can be acquired quickly in a development environment. We then demonstrate the effectiveness of the reduced-order model to predict optimal recipe conditions to improve overall recipe performance. We show how, with this hybrid-metrology computational approach, a process window that yields 89.2% of the wafer can be captured.

Keywords: Etch, FinFET, Experimental Design, Process Optimization, Recipe Creation, Image Segmentation, SEM

1. INTRODUCTION

Modern chips can contain over 100 billion complex nanodevices that are less than 50 atoms across.[1] While there have been a number of advances in 2D and 3D metrology in recent years, each method has tradeoffs in terms of time, accuracy, and cost. Viable high-volume manufacturing metrology tools must be fast, accurate, and non-destructive to meet throughput requirements. During development, more information-dense destructive means such as cross-sectional SEMs are typically taken, which increases the amount of local feature information gained from each experiment, but has several downsides such as long sample preparation and measurement times as feature dimensions must be painstakingly measured. These difficulties can lead to taking few sample measurements which inhibits information gain on the overall process space, which reduces the predictive power of any analysis and ultimately results in increased process variation.

Other non-destructive measurement methods involve techniques such as Atomic Force Microscopy (AFM), Tunneling Electron Microscopy (TEM), and ellipsometry. However, these primarily yield information about the surface of an etch as compared to an X-SEM, which yields information throughout the etch geometry. Table 1 highlights some of the trade-offs between existing metrology approaches.[2,3]

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Table 1. Trade-offs between traditional metrology tools (green = good, orange = middling, red = bad)

	Traditional OCD	CD-SEM	AFM	Cross-Sectional SEM/TEM
Time-to-solution				
Time-to-measure				
Non-destructive				
Area				
3D Profile Information				

One strategy to mitigate these metrology challenges and accelerate process development is to leverage a computational modeling approach which can holistically combine the measurement outputs from multiple metrology tools in order to create a high accuracy, high resolution depiction of the process space. One such way, here shown in section 2.2, is to build a model using SandBox Studio™ AI.[2,4–6] SandBox Studio™ uses a combination of physical simulation and machine learning to synthesize the information from multi-modal metrology tools such as OCD and X-SEM and make substantive predictions across a design space without being prohibitively expensive experimentally or computationally. To take in the multi-modal metrology information, SandBox Studio™ AI manages the preprocessing of data taken in multiple modes (images versus numerical), multiple length scales (local feature versus across wafer), and resolves conflicting and/or missing data. SandBox Studio™ AI models have also been shown to be effective in cases where few experimental data are available thereby reducing R&D time and waste.[2] By using diverse measurement methods, a model which accurately captures feature-level and across-wafer variability can be constructed, which enables a greater realized wafer yield than using a single measurement method alone.

2. METHODOLOGY

2.1 Automated Model Build using Sandbox Studio™ AI

Using the input data described in section 2.2, a SandBox Studio™ AI model was automatically built using the provided experimental process parameters and critical dimensions. The key governing mechanisms associated with the etch behavior were selected using a hybrid physics and machine learning approach.

2.2 Identifying an Optimal Recipe Window

Using predictive models allows us to explore the recipe design space such that we can choose process parameters which result in both good wafer coverage and robustness against small process parameter variations. Experimentally exploring this space would be prohibitively expensive and logistically challenging. After constructing a representative model using SandBox Studio™ AI, one can map predicted CDs across a wafer in space and across process parameters (PPs). Doing so results in a series of nested plots hereafter referred to as "Quilt®" process maps. Plotting these for a single CD across a subset of the most important PPs in the case study explored in section 2.2 yields a Quilt® process map as shown in figure 1. To find the optimal process window for the following case study, 3D behavior was simulated across the wafer for 1,594,323 (3^{13}) different recipes.

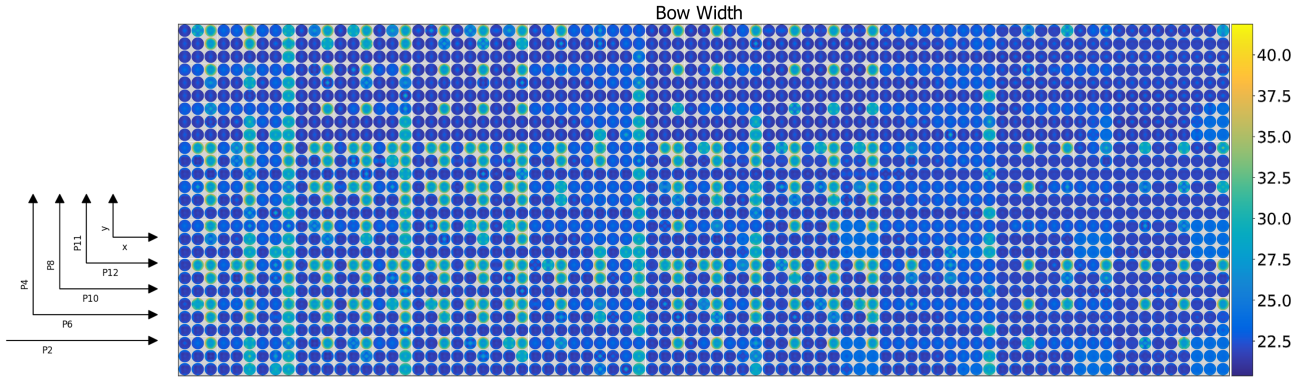


Figure 1. A Quilt® process map demonstrating the variable and non-linear impact of process parameters on bow width. Each individual wafer plot indicates bow width variation across the wafer for a different set of process parameters. From the inside out, referring to the guide axes on the left: each small 3x3 cluster of wafers represents all possible combinations of three different values of P11 and P12 (low, medium, high). Each 3x3 cluster of 3x3 wafer blocks, containing 81 wafers in total, represents all possible combinations of three different values of P8 and P10. Each 3x3 grouping of 9x9 wafer blocks, containing 729 wafers in total, represents all possible combinations of three different values of P4 and P6. Finally, the macro-structure is broken up into three 27x27 blocks along the horizontal axis, each corresponding to a single value of P2. This structure is easiest to visually pick out in the leftmost block (where P2 is at its minimum).

The recipe optimization for a FinFET etch is considered.[7] Recipe performance is evaluated based on the critical dimension targets listed in table 2.

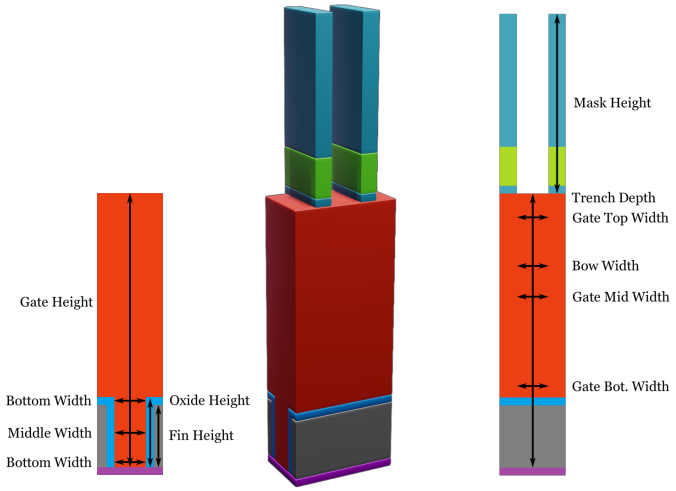


Figure 2. The geometry considered in this paper. Two 2D cross-sections are considered for measurement purposes and the entire 3D feature is considered for simulation.

Table 2. Target Critical Dimensions and tolerances (nm)

Critical Dimension	Target Value
Bow Width	22.0 ± 2.0
Gate Bottom Width	20.0 ± 2.0
Trench Depth	130.0 ± 3.0
Oxide Height	45.0 ± 2.5
Fin Height	40.0 ± 2.0
Gate Height	0.0 ± 5.0

This synthetic use case has the following parameters:

- 1 step etch
- 13 process parameters to optimize
- 20 synthetic experiments executed
- Process parameters cannot be controlled as a function of position

An example of the CD distribution of the gate height for one of the experiments in the synthetic data set is shown in figure 3. The gate height varies across the wafer from 0 to 160 nanometers indicating process non-uniformities.

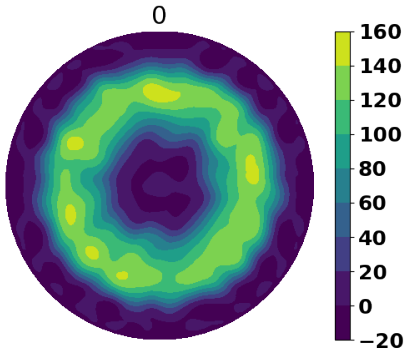


Figure 3. Gate height distribution across the wafer for experiment 0.

Yield is calculated by first optimizing the process window using the data available for each case, then calculating the wafer area fraction that achieves the measurement targets to the required tolerances in table 2.

Three cases were analyzed based on the following metrology sources:

1. Optical Critical Dimension (OCD) data taken from 25 sites across the wafer
2. Cross-sectional SEM (X-SEM) data taken from one site at the center, middle, and edge of the wafer
3. Hybrid metrology using both 25-site OCD and 3-site X-SEM

The 25 cross-wafer OCD and 3 X-SEM measurements were taken in the following configuration:

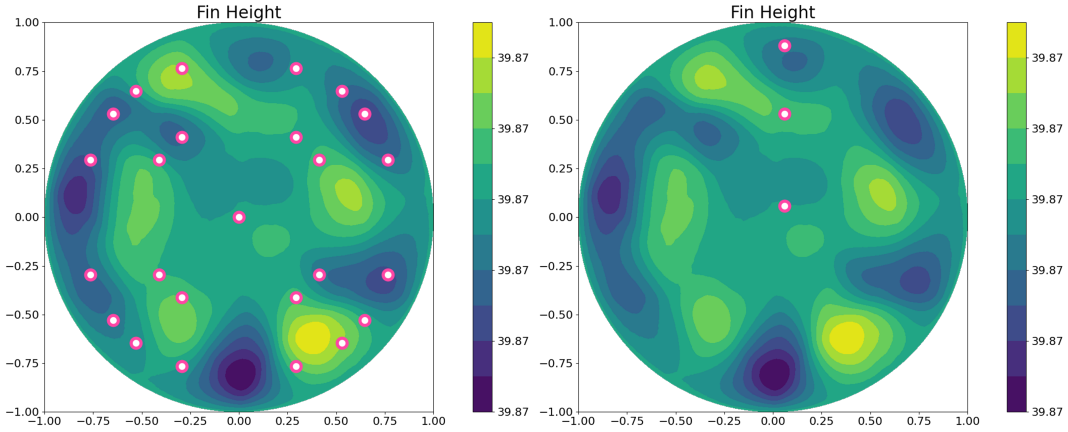


Figure 4. Measurements across the wafer were taken at the indicated sites, partitioned into "center", "middle", and "edge" radial bands, respectively from the center of the wafer outwards. Left: OCD measurement locations. Right: X-SEM measurement locations.

The goals of this exercise are the following:

1. Demonstrate how computational modeling can be used to synthesize metrology information for 3D architectures
2. Demonstrate how computational modeling can be used to improve process yield with minimal experiments

3. RESULTS AND DISCUSSION

Table 3 highlights the differences in metrology information for each of the three cases. The OCD measurements were taken over a larger area, but provided less detailed CD measurements of the local feature profiles. The cross-sectional SEMs were taken at only 3 locations but provided significant material and 3D metrology information. Each of the three models was built in $\leq$ 96 hours.

Table 3. Model Build Summary

Case	Metrology	Types of CDs	Total Model Build Time (4 nodes)
1	OCD	Bow Width Trench Depth Gate Bottom Width Fin Height Top Width	72 hours
2	XSEM	Bow Width Trench Depth Gate Bottom Width Fin Height Top Width Gate Height Oxide Height	24 hours
3	OCD + XSEM	Combined OCD and XSEM data	96 hours

3.1 Case 1 – OCD Measurements Only

Using Optical Critical Dimension (OCD) measurements, taken at 25 sites across the wafer, and no X-SEM information, a pass region was identified in the produced process map. The pass region exhibited a yield of 14.5% across the wafer.

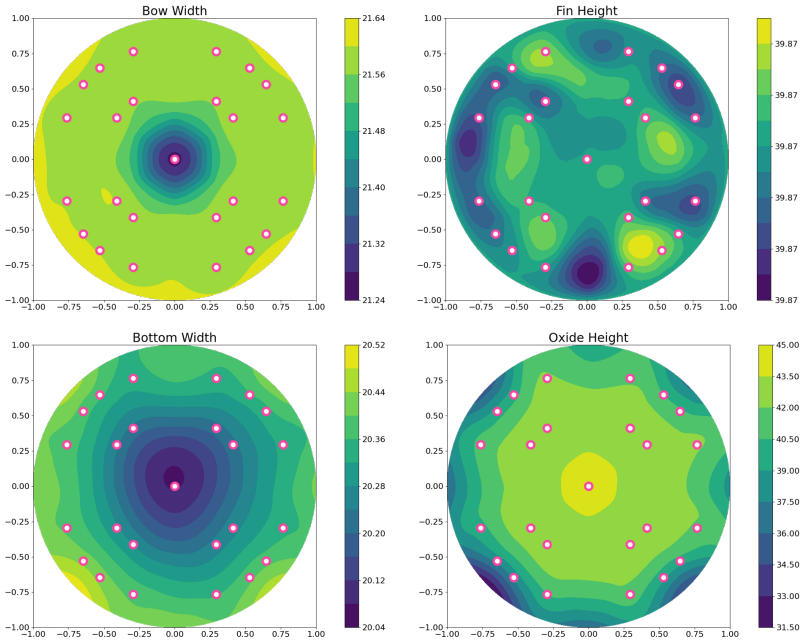


Figure 5. CD distributions across four wafers overlaid with the sites of the OCD measurements. Referencing table 2, we can see that only the middle region passes in these four CDs. This is further indicated in table 4 where it can be seen that the center and edge fail for trench depth, gate height, and oxide height respectively.

Table 4. Case 1 CD averages (nm)

Critical Dimension	Target Value	Center	Middle	Edge
Bow Width	22.0 ± 2.0	21.3	23.5	22.6
Gate Bottom Width	20.0 ± 2.0	20.1	20.34	20.4
Trench Depth	130.0 ± 3.0	99.1	131.1	131.2
Oxide Height	45.0 ± 2.5	44.4	42.1	39.4
Fin Height	40.0 ± 2.0	39.9	39.9	39.9
Gate Height	0.0 ± 5.0	73.1	0.0	0.0

3.2 Case 2 – X-SEM Measurements Only

Using only the much more information-rich cross-sectional SEM (X-SEM) measurements, taken at 3 sites across the wafer, a pass region was again identified. This pass region yielded 65.9% of the wafer area.

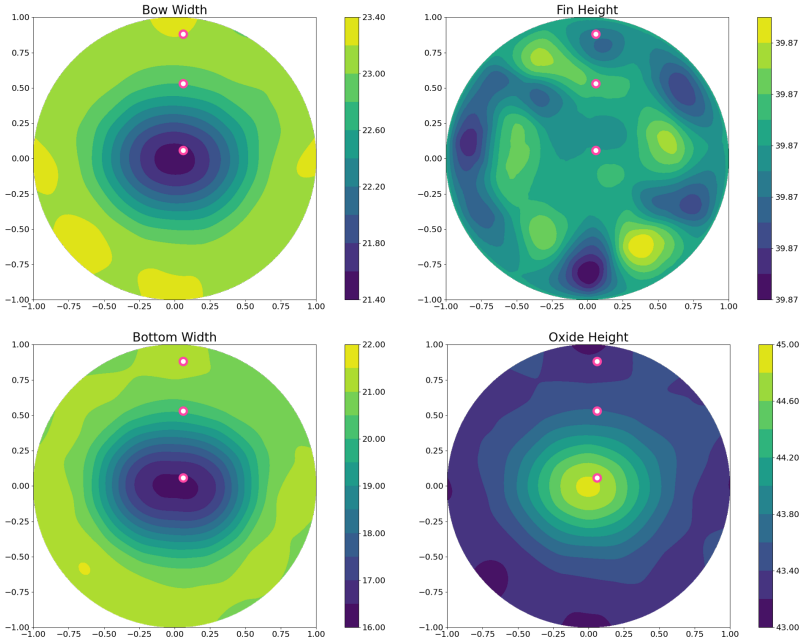


Figure 6. Measurement sites and CD distributions across the wafer for case 2. The density of information in an X-SEM is significantly higher for local features than that of the employed OCD measurements. This information density results in significantly greater predictive accuracy for profile control of local 3D features.

Table 5. Case 2 CD averages (nm)

Critical Dimension	Target Value	Center	Middle	Edge
Bow Width	22.0 ± 2.0	21.5	23.0	23.3
Gate Bottom Width	20.0 ± 2.0	16.3	20.8	21.3
Trench Depth	130.0 ± 3.0	113.0	131.5	131.7
Oxide Height	45.0 ± 2.5	44.9	43.4	43.1
Fin Height	40.0 ± 2.0	39.9	39.9	39.9
Gate Height	0.0 ± 5.0	59.2	0.0	0.0

3.3 Case 3 – OCD + X-SEM Measurements

This last case, which utilizes all 25 OCD as well as the 3 X-SEM measurements, has the greatest yield at 89.2%. Only localized regions of the wafer fail, as can be seen in figure 7.

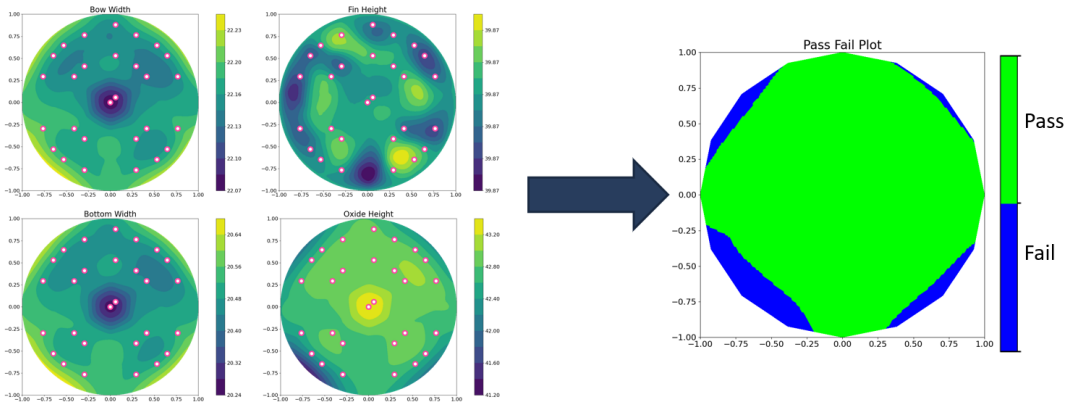


Figure 7. Measurement sites and CD distributions across the wafer for case 3. Using all 25 OCD data and 3 X-SEM measurements results in the highest yield of the three cases (OCD only: 14.5%, X-SEM only: 65.9%, OCD + X-SEM: 89.2%). The pass/fail coverage is shown in the right plot. Except for small regions near the edge, this wafer passes all CD criteria defined in table 2 and demonstrates a marked improvement in manufacturing efficiency.

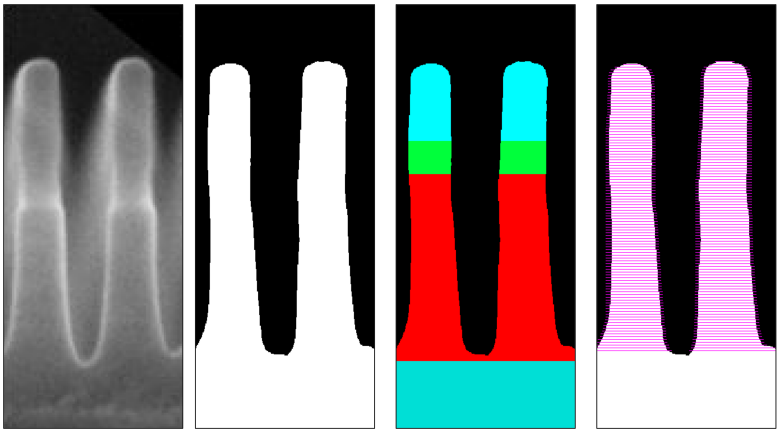
Table 6. Case 3 CD averages (nm)

Critical Dimension	**Target Value**	**Center**	**Middle**	**Edge**
Bow Width	22.0 ± 2.0	21.1	22.2	22.2
Gate Bottom Width	20.0 ± 2.0	20.3	20.5	20.5
Trench Depth	130.0 ± 3.0	130.8	131.1	131.1
Oxide Height	45.0 ± 2.5	43.4	42.9	42.8
Fin Height	40.0 ± 2.0	39.9	39.9	39.9
Gate Height	0.0 ± 5.0	0.0	0.0	0.0

Case 3 shows the benefit of leveraging both means of measurement. The more effectively we can utilize the experiments we do run, the more accurate a map of process parameter space we can generate. Armed with that map, we can design more robust, high yield processes which will enable future generations of microelectronic manufacturing.

4. IMAGE SEGMENTATION VIA WEAVE™

One of the key hindrances in making effective X-SEM measurements is the work required to measure and compare images accurately and consistently. Weave™ can be used to automatically segment cross-sectional SEM and TEM images and extract key profile and CD information. In the Weave® workflow, previewed in figure 8, X-SEM or TEM images are automatically aligned, segmented, and colorized per material. Profile information is extracted based on user-defined targets. Model builds for Weave® typically take < 30 minutes and involve a processing time of < 1 minute per image.



Phase	Time (min)
Initial Model	2:29
Time per image	0:48

Weave™ Analysis	
Min Width (nm)	11.2
Max Width (nm)	36.5
Average Width (nm)	22.3

Figure 8. A step-by-step demonstration of the Weave™ workflow. From left to right, the original SEM image (taken by any commercially available SEM), the segmented image, the segmented image colorized to indicate material boundaries, and the segmented image annotated with a large number of horizontal width measurements. All three were automatically generated using Weave™. The time to train the segmentation model and the processing time per image are given in the top table. The resulting measurements of those bulk probes are shown in the bottom table.

This functionality is useful for in-house quality control, and can be used in conjunction with Sandbox Studio™ AI to increase the information density of X-SEM data even further.

5. CONCLUSION

As node sizes shrink and architectures become more complex, etch processes increase in complexity and sensitivity. Using purely experimental methods for developing manufacturing processes is quickly becoming untenable; predictive tools are therefore being developed to improve this process.

In this work, automated model development for a 3D FinFET was demonstrated using SandBox Studio™ AI, using three different types of metrology inputs. In all three cases, key governing mechanisms were automatically selected and the resulting model calibrated. The models were then used to simulate 3D behavior across the wafer for 1,594,323 (3^{13}) different recipes to define optimal operating windows that achieve the recipe targets and maximize wafer yield. Comparison of the three models illustrated how computational simulations can be used to leverage multiple types of metrology at once. With a multi-modal metrology approach, an optimal process recipe which yielded 89.2% of the wafer was achieved. Finally, a new streamlined workflow for processing X-SEM data was demonstrated using Weave™. This workflow can be used in conjunction with SandBox Studio™ AI to increase the information density, reproducibility, and cost-effectiveness of X-SEM metrology for model calibration or internal quality control.

Acknowledgments

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