Materials Letters 330 (2023) 133364

Contents lists available at ScienceDirect

Materials Letters

journal homepage: www.elsevier.com/locate/matlet

Electrical property-microstructure of copper interconnects printed by localized pulsed electrodeposition (L-PED)

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ARTICLE INFO

Keywords:
Mesoscale printing of metals
Localized electrodeposition
Interconnects
Nanotwinned microstructure
Electrical characterization

ABSTRACT

Printing processes that enable printing high conductivity metals at small scale (<mm) are in demand for microelectronics, interconnects, and sensors applications. Since electrical properties of metals are controlled by their microstructure, microstructure-property relation for each process needs to be established. In the recently developed localized pulsed electrodeposition (L-PED) process, the pulsed voltage applied during metal printing allows control over the microstructure. In this article, we quantify the electrical resistivity of copper (Cu) interconnects printed by the L-PED process and correlate it with its microstructure. The results show a microstructure combined of nanotwinned (nt) grains and nanocrystalline (nc) grains, with an average grain size of 190 nm and twin thickness of ~8 nm to ~29 nm. The electrical resistivity was measured to be 8.25 μΩ.cm, which correlates with the observed microstructure and is remarkable for a printing process with no post-processing annealing done on the printed metal.

1. Introduction

3D printing of metals and alloys at the small scale (<mm) is promising for microelectronics, interconnects, and sensors applications [1–4]. Direct ink writing (DIW) and electrohydrodynamic printing (EHD) processes are examples of such processes [1]. Localized electrodeposition (LED) is a 3D printing process in which high crystalline metals and alloys are electrochemically printed without any polymer additives [2–4]. The LED process has several advantages including printing of nanotwinned metals under pulsed current [5,6], control over microstructure [7], and printing on rigid and flexible substrates [8]. The most differentiating feature of the LED process is achieving low electrical resistivity of the printed metal without any postprocessing [3,8]. In a variation of the process termed localized pulsed electrodeposition (L-PED), a pulsed voltage is applied during metal printing, which results in a microstructure combined of nanotwinned (nt) grains and nanocrystalline (nc) grains [5–7]. Such a microstructure has distinct mechanical and electrical properties compared to pure nt and nc metals. Mechanical properties of metals printed by the L-PED process has been investigated [5,7]. However, since this process requires a conductive substrate (that affects electrical property measurements), accurate measurement of electrical conductivity has not been so far reported.

In this article, we quantify the electrical resistivity of Cu interconnects printed by the L-PED process (Fig. 1A) and correlate it with its microstructure. To do so, we demonstrate that the L-PED process can be expanded to print on non-conductive surfaces, so long as printing is started from a conductive point as the cathode, and continuous connection to the cathode is maintained during printing. This process allowed us to print interconnects directly on a patterned 4-point probe measurement device (Fig. 1B and C), which enabled measurement of electrical conductivity without influence from any conductive substrate or contact resistance.

2. Results and discussion

The L-PED process is schematically shown in Fig. 1A. A detailed description of the setup and printing process are available in our previous publications [5,6]. Fig. 1B, C demonstrate the feasibility of direct

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https://doi.org/10.1016/j.matlet.2022.133364
Received 6 September 2022; Received in revised form 8 October 2022; Accepted 16 October 2022
Available online 21 October 2022

printing of an interconnect of Cu using this process on a 4-point probe device (Fig. 2A). We note that interconnect fabrication requires continuously printing on the conductive and insulator surface, therefore, it is critical for the electrolyte and print front to maintain electrical/ionic contact. This is the first demonstration that in the L-PED process if the process is initiated on a conductive substrate, it can be continued on a nonconductive substrate, so long as the necessary electric ground is maintained with the conductive substrate.

Fig. 2B shows an example of an AFM image and a line-scan profile with a cross-sectional area (S) of 18.6 μm^2 (Fig. 2C). We developed a computational model using COMSOL Multiphysics to quantify the effective length in 4-point probe measurement (details in SI). We calculated the electrical resistivity of the printed interconnect (8.25 μΩ.cm) based on the obtained AFM geometry, the measured resistance by probe station, and effective length from the computational model. The measured resistivity of the printed interconnects is in between the resistivity values of fully nanotwinned (nt) and nanocrystalline (nc) Cu. The electrical resistivity of coarse-grained Cu, nanotwin Cu, nanocrystalline Cu, and nanocrystalline-nanotwin Cu measured at room temperature have been reported to be ~1.48 μΩ.cm, 1.5 μΩ.cm, 18 μΩ.cm, and 27.6 μΩ.cm, respectively [9,10].

To correlate the measured electrical resistivity with the microstructure, we acquired FIB and TEM images. Fig. 3A, B show the FIB ion channeling contrast cross-section images of a 3D printed interconnect. Printing process parameters are given in Table S1. A nanocrystalline structure was observed (an average grain size of ~190 nm). Grains exhibit a variation in aspect ratio, with small semicircular grains and elongated irregular grains. A radial distribution may be suggested although the trend is not strong. A TEM Bright Field (BF) image (shown in Fig. S4) shows a roughly equiaxed grain structure with random orientations and crystals varying in size (50 to 350 nm). No columnar grains were observed in TEM images. The ion channeling contrast FIB images revealed the existence of nanotwins within grains (Fig. 3B). Based on image analysis, the percentage of twinned areas relative to the overall cross-sectional area was estimated to be ~20 %. This correlates well with the finding that the measured resistivity of the printed interconnects is in between that of the fully nanotwinned (nt) and nanocrystalline (nc) Cu.

The TEM image in Fig. 3C confirmed the formation of densely packed nanotwins. The corresponding diffraction pattern and high-resolution TEM (HRTEM) images are shown in Fig. 3D, and 3E, respectively. Fig. 3D shows the selected area diffraction pattern (SADP) with typical reflections (double-spot characteristic of twinning) from twin boundaries. Fig. 3E shows an HRTEM image of a TB. The TB is shown by the dashed line and the orientation of the lattice on two sides of the TB is denoted by mirror solid lines. According to this analysis, the electron beam direction in this image was along the [0 1 1] axis. Measurements of twin lamellar spacing along the [0 1 1] direction showed that the average twin spacing varies from ~8 nm to ~ 29 nm. In the HRTEM image, the insets (i-iii) are FFT patterns for (i) the TB, and (ii) and (iii) the two sides of the TB. The patterns display rotation from one side to another side of the TB (the inset). The rotation pattern, while preserving the same zone axis, confirms the presence of a TB.

Based on the measured electrical properties and considering the superior electrical properties of nt-Cu compared to coarse-grained and nanocrystalline Cu, we believe that the L-PED process can be reliably used for interconnects fabrication. By nanotwining, oxidation resistance and electromigration (EM) resistances [11], and thermal stability [12] are greatly enhanced without significantly sacrificing electrical conductivity [9]. Thus, it could be an optimal solution for the semiconductor industry. Thermodynamics analysis on the nucleation of twins in metal films predicts that a higher electrodeposition rate (higher current density) will lead to higher metal nucleation rate, and thus a higher twin density (smaller average twin spacing) [13–15]. The twin density can be also controlled by adjusting the physical and chemical parameters, such as the pH value, current density, and temperature. Twin spacing has direct effect on the resistivity of the electroplated films. It has been reported that an increase of twin spacing from 15 to 90 nm, the resistivity has increased gradually from 1.75 to 2.12 μΩ. *Cm* [16]. Hence, the future work may be focused on changing the printing process parameters to map the process-microstructure-electrical properties. Process parameters may be identified through which desirable twin density and twin lamellae thickness can be obtained. We note that external stimuli such as electron irradiation may be used to alter mechanical properties of metallic structures [17]. Additionally, local electric field may be used to heal potential defects in these structures and enhance electrical properties [18]. Mechanical properties of such nanostructures and their potential size-effect can be quantitatively measured [19,20].

3. Conclusions

This work demonstrated the possibility of printing low resistivity Cu interconnects that have a combined of nanotwinned and nanocrystalline microstructure using localized pulsed electrodeposition (L-PED), without any post-processing. The correlation of the electrical conductivity and microstructure of the printed Cu promises that further improvements can be achieved through a full and systematic process-microstructure-property relations to quantify the optimal process parameters of the L-PED process for expansion into interconnect, microelectronics, and sensors applications.

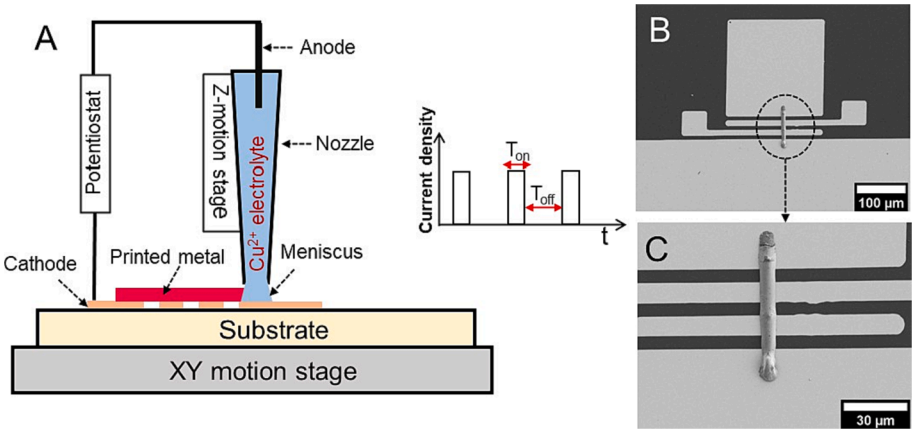

Fig. 1. (A) The LED metal 3D-printing process. (B) and (C) An SEM image of the printed interconnect.

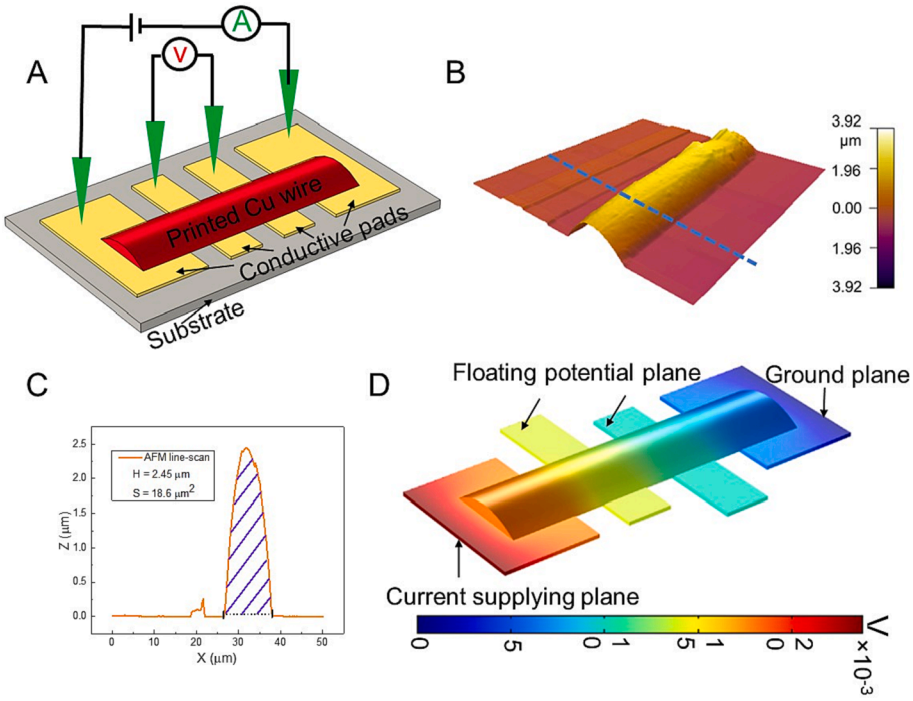

Fig. 2. (A) The four-point probe used for the electrical resistivity measurement of printed interconnect. (B) An AFM topography image of a printed interconnect. (C) An AFM line-scan. The height of the printed Cu interconnect is ~2.4 μm. (D) The distribution of the electric potential for the 4-point probe measurement obtained from the Multiphysics simulation.

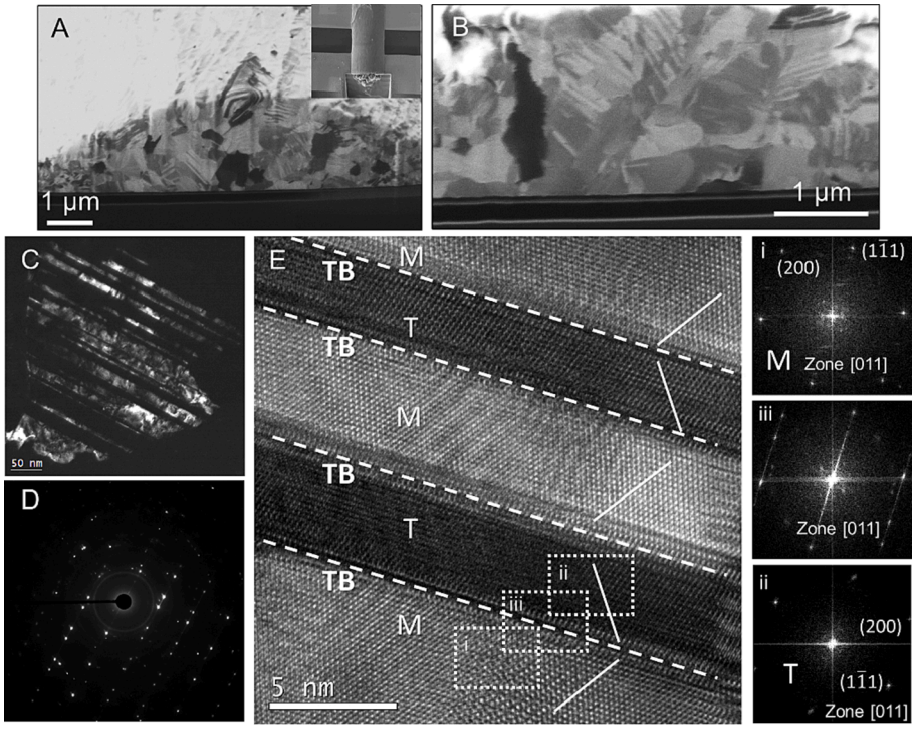

Fig. 3. Microstructure of the Cu interconnect printed using the L-PED process. (A) Cross-sectional FIB ion channeling contrast image. (B) High magnification image of an area of part A shows high-density parallel TBs in several of the grains. (C) Dark-field image of a grain ~350 nm in size that shows the characteristic contrast of twin boundaries. (D) Selected-area diffraction pattern corresponding to the grain in C reveals the typical reflections from twin boundaries. (E) High-resolution TEM (HRTEM) image of a typical coherent TB. The TBs are shown by the dashed lines. Insets are FFT patterns of (i, ii) two mirrored sides of the TB, and (iii) the TB, respectively.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

This work was supported by the US National Science Foundation

grant # 2152725.

Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.matlet.2022.133364.

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Supplementary Information

Electrical Property-Microstructure of Copper Interconnects Printed by Localized Pulsed Electrodeposition (L-PED)

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Materials and methods

The printing process: Cu interconnects were printed using a glass nozzle with a diameter of ~5 μm and filled with an electrolyte of $CuSO_4$ (50 mM) and H_2SO_4 (1 M). Photolithographically patterned silicon substrate (Fig. S1) coated with Au served as the cathode and a Cu wire inserted into the nozzle was the anode. A pulsed voltage with an on-time of 0.01 s, an off-time of 0.99 s, and average current density of ~0.08 A/cm^2 was applied during printing based on previous reports [5, 6]. The custom-made printer utilizes a piezo nano-positioning system as previously described [5-7].

Electrical conductivity measurement: The electrical conductivity measurement was carried out by connecting four micromanipulator probes to four gold pads of the 4-probe device (Fig. S2). The probes were then connected to a Keithley 2450, with current and voltage resolutions of 10 nA and 20 mV, respectively. Current was supplied to the two gold pads at the two ends of the printed Cu

wire in a linearly increasing fashion with a 5 μA ramp. Voltage was measured simultaneously from the two middle pads. The experimentally measured resistance was used to calculate the resistivity of the printed Cu interconnect using $\rho = \frac{RA}{L}$. The interconnect cross-section was measured by Atomic Force Microscopy (AFM). 10-line scans in the 3D AFM topography image (Fig. 2B) were averaged to be considered as the cross-section of the interconnect (Fig. 2C). As gold pads have finite width, *L* as the effective length was estimated using the COMSOL finite element simulation (Figs S3C and 2D). Details are provided in the SI.

Preparation of the 4-point probe substrate

The geometric shape of the four-point probes on a mask was transferred to the insulator surface of a silicon wafer coated with 300 nm SiO_2 by photolithography process. To prepare the substrate for electrodeposition, 40 nm conductive metal layer (gold (Au)) was deposited using an e-beam vapor deposition system. A 20 nm Cr layer was deposited before Au deposition to improve the adhesion. After deposition, the substrate was ultrasonically cleaned with acetone for 3 minutes to perform the lift-off process and make the substrate ready for printing. The process flow of the substrate preparation is schematically shown in (Figure S1).

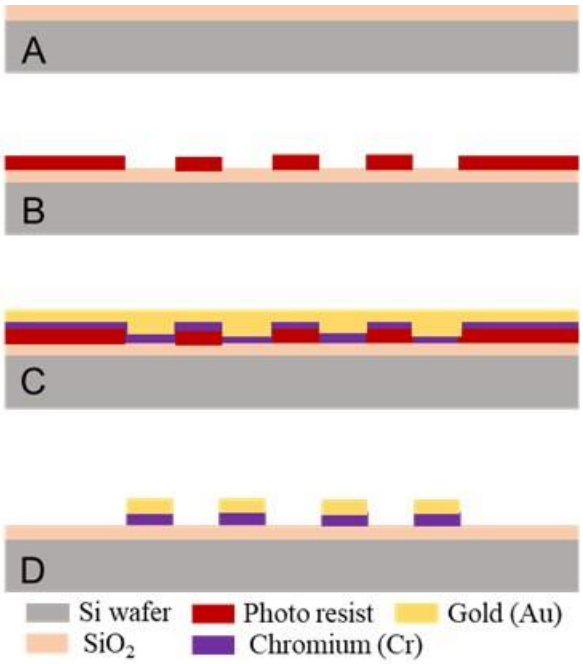

Figure S1 Detailed diagram of fabrication steps of four-probe measurement device. (A) 300 nm SiO_2 deposition step using e-beam vapor deposition process. (B) Photoresist pattering step for the lift-off process. (C) Deposition of chromium (Cr), and gold (Au) using e-beam vapor deposition process. (D) Photoresist lift-off process.

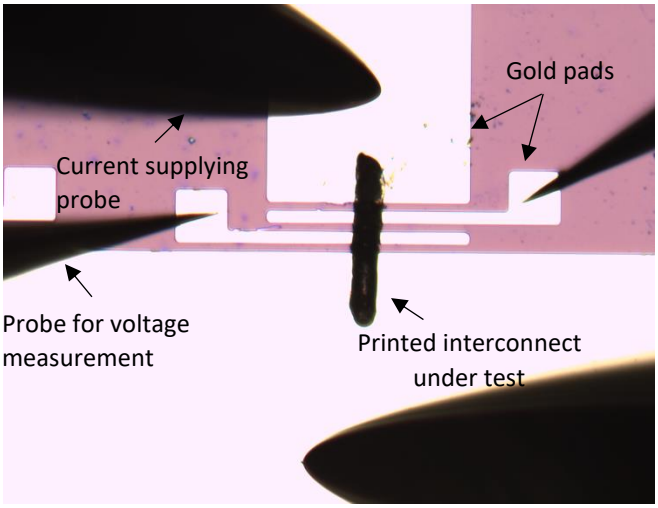

Figure S2. Experimental setup of the electrical measurement.

Estimation of effective length using COMSOL simulation for resistivity calculation

L is the length between two points where voltage was measured along the Cu interconnect. As gold pads (figure S3A, and figure S3B) have finite width, *L* can have two values, without adding the width of the pads and with adding the width of the pads. Therefore, finding the effective length is required for accurate resistivity calculation. We conducted numerical simulation in COMSOL Multiphysics commercial package using a 3D finite element model to estimate the effective length. The experimentally measured cross-section (by AFM) was used to build the geometry of the Cu interconnect. Three-dimensional triangular elements were used to mesh the geometry. A total number of 1,77,836 elements were used in the simulation, after a mesh sensitivity analysis to ensure that the results are independent of the mesh size. The details of the model for different physics are shown in figure S3B.

Electric Currents module was used as the main physics in the simulation. The model considers current conservations in all domains, electric insulation in all boundaries, and zero initial electric potential in all domains. The initial values and boundary conditions in the model were assigned based on the experimental conditions. A constant current (1A) was applied between the current carrying and ground plane of the model, and voltage was measured between the two floating potential planes. Current and initial value for voltage was set as zero for both floating potential planes. Measured voltage between two floating planes and provided current between current supplying and ground planes were used in the Ohm's law ($V = IR$) to calculate the resistance of the printed Cu interconnect. As a material property, resistivity of the bulk copper was set as the resistivity of the Cu wire in the simulation. Using the resistivity equation ($R = \frac{\rho L}{A}$), the effective length of the Cu interconnect was calculated computationally and was used to estimate

the resistivity of the printed Cu interconnect. The effective length was estimated to be ~ 17.65 µm, which is in between L_{min} (8 µm) and L_{max} (31 µm).

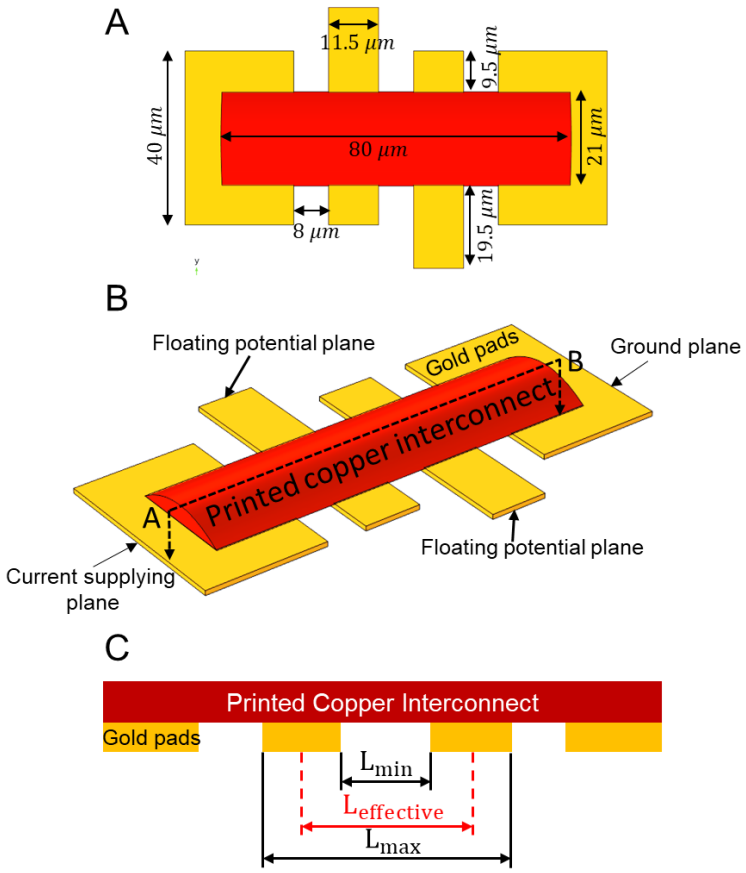

Figure S3. (A) The top-view of the COMSOL model. **(B)** The boundary conditions for electric current physics. **(C)** Cross-sectional view of the geometry shown in B along the A-B line.

Microstructure characterization

The microstructure of the printed Cu interconnects was characterized utilizing scanning electron microscopy (SEM, Zeiss Supra 40), high-resolution focused ion beam (FIB, FEI Nova Nanolab 200), and transmission electron microscopy (TEM, JEM-ARM200F). Ion channeling imaging and TEM sample preparation were completed using the FIB. For ion channeling imaging, the FIB

instrument was operated at 30 keV and 30 pA. High-resolution TEM imaging, Dark Field imaging, and Selected Area Diffraction Pattern (SADP) were performed using a JEM-ARM200F, operated in TEM mode at 200 keV.

Table S1 Process parameters for printed Cu interconnect.

Voltage (V)	**Average current density (A/cm^2)**	**Nozzle speed (nm/s)**	**Pulse On-time (s)**	**Duty cycle**	**Nozzle diameter**
0.25	0.08	50	0.01	1/100	6.6 μm

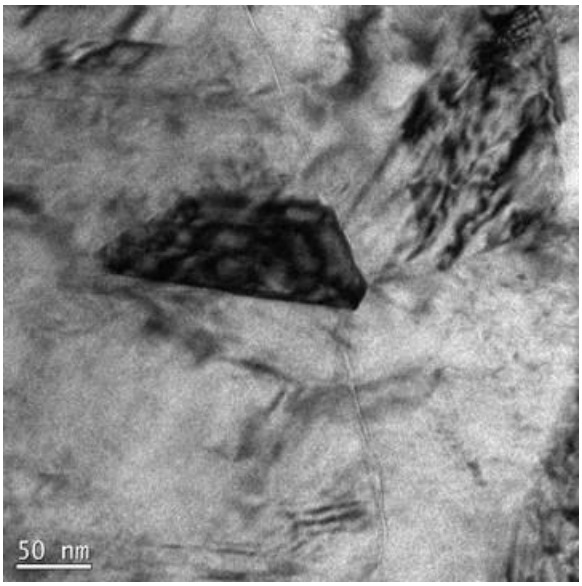

Figure S4. A TEM bright field (BF) image of Cu grains in a 3D printed interconnect.