

Enhanced Thermoelectric Performance of Holey Silicon Thin Films using F₄TCNQ Surface Doping

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Abstract

Silicon thin films have great potential as chip-integrated Peltier micro-coolers and thermoelectric power generators due to their industry compatibility and cost effectiveness. Improving the thermoelectric figure of merit, zT , and therefore the device efficiency can be achieved by increasing the power factor while decreasing the thermal conductivity. In this work, we study single crystalline silicon thin films with patterned nano-holes with sizes comparable to the phonon mean free path to suppress thermal conductivity. The holey silicon thin films are then surface doped with organic molecules F₄TCNQ to create a three-dimensional modulation doping scheme. As the dopants are outside the host material, there is less impurity scattering, which improves carrier mobility and the overall power factor. We fabricate silicon thin films with periodic arrays of nano-sized holes, with a fixed pitch size of 300nm. By changing the hole diameters, we vary the neck size from 169nm to 22nm. The in-plane thermal conductivity, measured using the heat diffusion imaging method, demonstrates an order of magnitude reduction compared to bulk silicon and a change from $26\text{Wm}^{-1}\text{K}^{-1}$ to $5\text{Wm}^{-1}\text{K}^{-1}$ at room temperature. The films with large hole diameters allow space for the relatively large F₄TCNQ molecules and hence effective surface doping, which is evident by orders of magnitude improvement in the electrical conductivity and power factor.

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1. Introduction

Silicon thin films are potential candidates for thermoelectric applications such as on-chip thermal management [1] and power generation for wearable electronics [2], due to their industrial process compatibility and cost-effectiveness. It is shown that silicon thin-films are flexible and upon transfer to flexible substrates, they can be used for wearable electronic applications [3, 4]. The efficiency of thermoelectric power generators and the coefficient of performance of Peltier coolers are an increasing function of the thermoelectric figure of merit, $zT = \sigma S^2 T / \kappa$, where σ is the electrical conductivity, S is the Seebeck coefficient and κ is the thermal conductivity. Improving the zT of a material can be achieved by increasing the power factor ($PF = \sigma S^2$) while decreasing the thermal conductivity κ .

An effective route to reducing the thermal conductivity of Si is through the addition of nanostructures [5, 6] or increasing surface roughness [7], which induces more frequent phonon scattering and limits the phonon mean free path (MFP). This has been implemented on Si thin films, by patterning arrays of nano-sized holes [8, 9, 10, 11, 12, 13]. These silicon thin films with an array of holes are referred to as holey Si thin films or sometimes as phononic crystals. Research has shown that the thermal conductivity depends on the neck size, i.e., the distance between adjacent holes [5, 6]. The reduction in thermal conductivity can be one or almost two orders of magnitude compared to thin film without holes, depending on the neck size and the temperature [10, 14]. In these structures, an optimum design is to have neck sizes in between the electron and the phonon MFP to selectively limit phonon diffusion with minimum effect on electron mobility, enabling zT improvement [10, 11, 12, 13].

Most thermoelectric materials are made out of heavily doped semiconductors. Bulk silicon demonstrates the maximum thermoelectric power factor at high doping levels (around 10^{20} cm^{-3}) [15]. Conventional doping techniques insert dopant atoms into the host materials. These dopants introduce strong Coulomb repulsion and reduce carrier mobility. In comparison, surface charge transfer doping is a clean and effective alternative, where charges exchange across the interface between the surface dopants and the host material due to energy band misalignment [16]. The ionized atoms are therefore distanced from the mobile charge carriers and a space-charge layer is formed at

the interface. As the dopants are outside the host material, the extra space between the dopants and the carriers lowers the ionized impurity interactions significantly. This is similar to the modulation doping idea used in transistors. The electron mobility in GaAs, for instance, has been enhanced by 4 orders of magnitudes using modulation doping strategy at below 10K [17].

The organic molecule, F_4TCNQ (2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane), is a strong electron acceptor with an electron affinity as high as $E_a = 5.24\text{eV}$ [18] and is often used as a p-type surface dopant for organic [19, 20] and inorganic [21, 22, 23] materials. First-principles calculations predict that physisorbed F_4TCNQ monolayer can efficiently dope Si [24], achieving a surface hole concentration as high as 10^{13}cm^{-2} . An experimental study on the transport properties at F_4TCNQ -Si interface demonstrated a resistance reduction by a factor of 10 compared to undoped film and a thermoelectric PF enhancement by 75% [25].

In this work, we extend the surface doping to three dimensions (3D). In a 2D geometry, while the thermoelectric power factor can be extremely large [26], one has to deal with an electron gas with a large thermal conductivity. The modulation doping concept has been extended to 3D in the past and improved zT has been shown in SiGe nanostructures [27, 28]. The improvement, in that case, was limited due to the grain-boundary scattering. Here, we propose the usage of holey silicon thin films to demonstrate 3D surface doping in organic-inorganic structures. The holey silicon films are clean with minimal scattering due to the periodic nature of holes and clean thin-film fabrication process, compared to the nanostructured bulk samples [27, 28] with irregular grain boundaries and impurities. They provide a possible geometry for a 3D network of organic dopants and effective doping not only from the top surface but also from within the film.

We fabricate single crystalline Si thin films with square lattice arrays of nanosized holes of different diameters and surface-dope them with F_4TCNQ . We report improvement in electrical conductivity by a factor as high as 350 and in the thermoelectric power factor by a factor as high as 200 after the deposition of F_4TCNQ , demonstrating the effectiveness of 3D surface doping. This is combined with the low thermal conductivity of the silicon films due to the presence of the holes to enhance the zT by 2 orders of magnitudes.

2. Material and Methods

The holey silicon thin-film devices were fabricated from silicon-on-insulator

(SOI) wafers, which had an active Si layer of 220nm thickness on top of a 3 μ m-thick SiO₂ layer. We used laser lithography and reactive ion etching (RIE) to

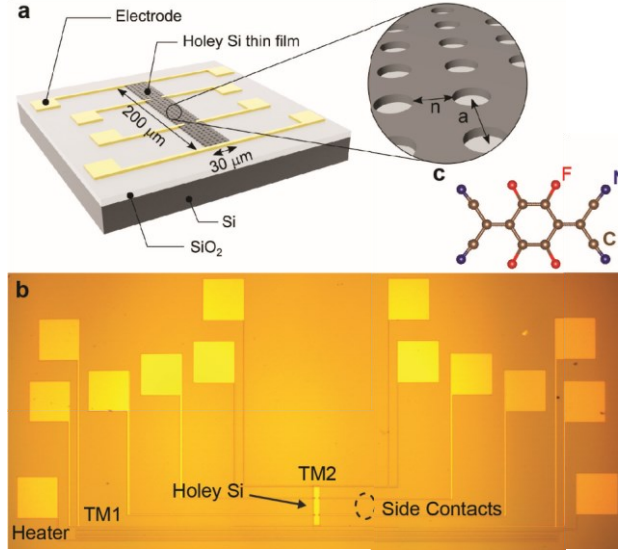


Figure 1: (a) Schematic and (b) optical image of the holey silicon device, which includes one heater, two thermometers (TMs) and four side contacts. The scale bar is 500 μ m. (c) Molecular structure of F₄TCNQ.

define device areas of 200 $\times$ 30 μ m². Subsequently, e-beam lithography and RIE patterned the nano-sized hole arrays onto each device. The holes were kept at a fixed pitch distance of $a = 300$ nm, and the neck size n of each device varied from 22nm to 169nm. Limited by the capability of the e-beam lithography tool, the smallest neck size we could reliably pattern was 22nm. Lastly, electrodes (500nm Al and 50nm Au) were evaporated onto the sample to serve as thermometers, heaters, and voltage probes. The Si layer was mildly boron-doped with a resistivity of 10 Ω ·cm, which corresponds to a hole concentration of $\sim 10^{15}$ cm⁻³. The regions under the contacts were doped to 10²⁰ cm⁻³ to ensure Ohmic contacts. Schematics of the hole configuration, as well as the device configuration, are shown in Fig.1.

F₄TCNQ crystal powder was thermally evaporated in a home-built vacuum chamber with a base pressure of $< 10^{-6}$ Torr. The deposition temperature was maintained at about 140 °C, following the methods described in previous work [25]. The samples were dipped in 10% HF for a few seconds right before being loaded into the evaporation chamber, in order to remove the native oxide and

passivate the Si surface. The structure of the F₄TCNQ molecule is presented in Fig.1(c), with a unit cell of 7.5×11.7×5.9Å³.

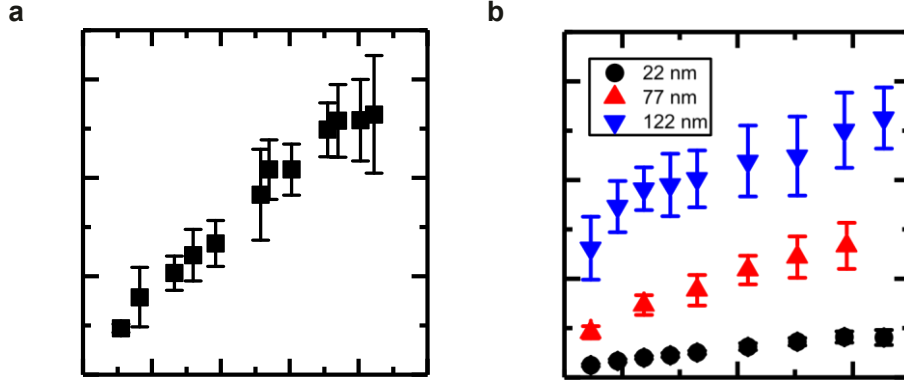


Figure 2: (a) Room temperature in-plane thermal conductivity for neck sizes from 22nm to 169nm and (b) temperature-dependent thermal conductivity from 50K to 350K for neck sizes 22nm, 77nm, and 122nm.

The electrical resistance was measured by the standard 4-point probe method and the conductivity was calculated assuming a solid thin film. The Seebeck voltage was measured by a Keithley 2182A nanovoltmeter and the temperature difference was interpreted from the resistance changes of the two gold thermistors at the two ends of the thin film.

Heat diffusion imaging [14] was used to measure the in-plane thermal conductivity. This is an electrical-pump optical-probe method that provides accurate readings for supported thin films using thermoreflectance-based techniques. A voltage pulse is passed through the thermometer placed directly on top of the thin film. As the injected heat flow propagates along the thin film of interest, a temperature map is calculated from the surface reflectivity changes. The thermal conductivity values are extracted based on how the temperature rise decays over distance. The details of the method and the process of extracting the thermal conductivity values of supported films are described in our previous work [14].

3. Results and Discussion

The in-plane thermal conductivity of the holey silicon thin film depends on the neck size. Figure 2 shows that as the neck size goes down from 169nm to 22nm, the room temperature thermal conductivity decreases from $26.4 \text{ Wm}^{-1}\text{K}^{-1}$

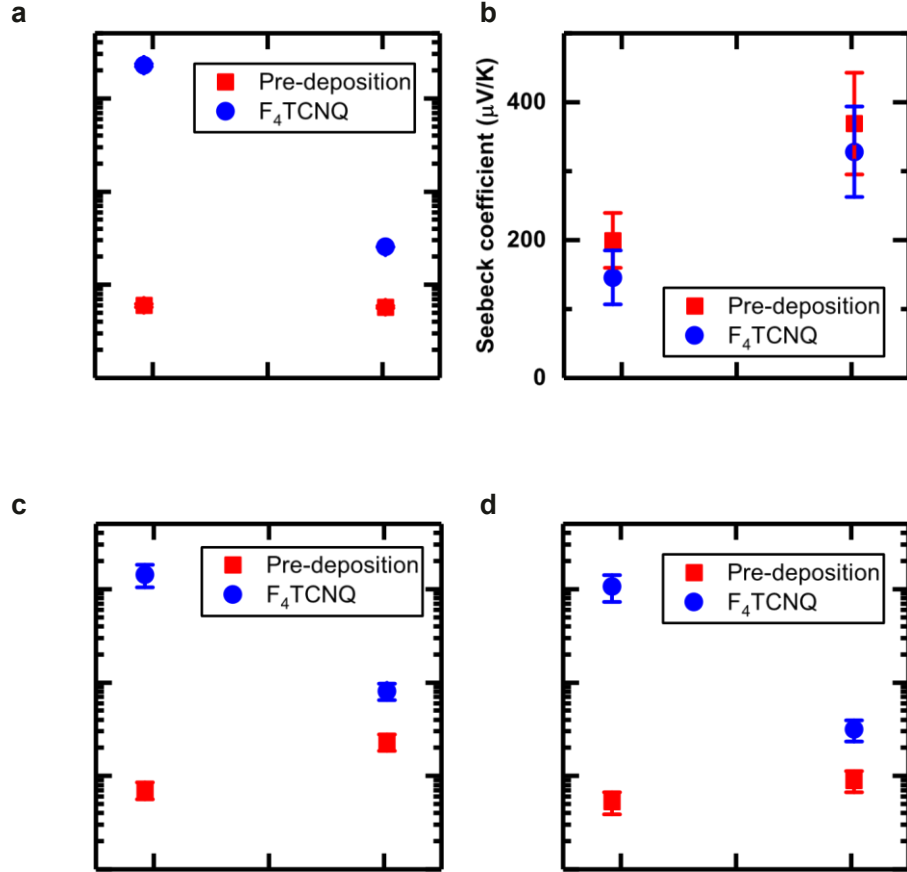


Figure 3: Comparison of the thermoelectric performance of the 77nm neck and 161nm neck devices before and after F₄TCNQ deposition at room temperature, in terms of (a) electrical conductivity, (b) Seebeck coefficient, (c) PFT, and (d) zT .

to $4.7 \text{ Wm}^{-1}\text{K}^{-1}$, nearly 5 times. Smaller neck size suppresses the phonon transport more and leads to smaller thermal conductivity values. The trend is consistent with those summarized in the literature [5, 6]. In comparison, the room temperature thermal conductivity of a silicon thin film of the same

thickness without any holes is about $90\text{Wm}^{-1}\text{K}^{-1}$ [29]. The reduction in thermal conductivity with periodic holes is as high as 19-fold.

The thermal conductivity of three different neck sizes as a function of temperature was also obtained and is plotted in Fig.2. Their temperature-dependent trends are consistent: as the temperature increases from 75K to above room temperature, the thermal conductivity increases, and the rate of change becomes smaller at higher temperatures. The overall change in this range is about 2 to 3 times.

The electrical transport of the thin film with neck sizes of 77nm and 161nm before and after the F_4TCNQ deposition was measured at room temperature. For both samples, their electrical conductivity started at around 60S/m. With F_4TCNQ , the conductivity of the 77nm sample increased by 2 orders of magnitude and reached $2.28 \times 10^4\text{S/m}$, while that of the 161nm sample increased to 255S/m, slightly over 4 times higher. As expected, the Seebeck coefficients of both samples dropped after doping, by about 10–20%. As a result, the power factor times temperature (*PFT*) was improved by 4 times for the 161nm neck sample and by 200 times for the 77nm one. The doping by F_4TCNQ here is more effective compared to the case of silicon thin film without holes[25]. A *PFT* as high as $0.14\text{Wm}^{-1}\text{K}^{-1}$ was achieved for the doped 77nm sample, which is on the same order of magnitude compared to highly-doped Si thin film samples from the literature [10, 30]. Unfortunately, due to electrical contact problems, we were not able to measure the neck-size dependence of the electrical conductivity and the Seebeck coefficient systematically as we did for the case of thermal conductivity. Among the prepared samples, only the 77nm and the 161nm samples had small and Ohmic contact resistances allowing electrical transport measurement.

Considering the two measured samples, several factors are deciding the effectiveness of the F_4TCNQ doping. First is the orientation of the molecules. It has been shown that when the molecules lay parallel to the surface, the charge transfer is small [24]. F_4TCNQ doping is only effective when the molecular long axis is normal to the silicon surface. Second, because the F_4TCNQ molecules tend to form clusters during the deposition process, the holes have to be large enough for the molecules to enter properly and attach to the inner cylindrical walls effectively.

Figure4 shows SEM images taken after 15 minutes of F_4TCNQ deposition on both 77nm and 161nm samples. When the holes are small, the clusters extend over and cover the top surface of the holes. This is the case for the 161nm

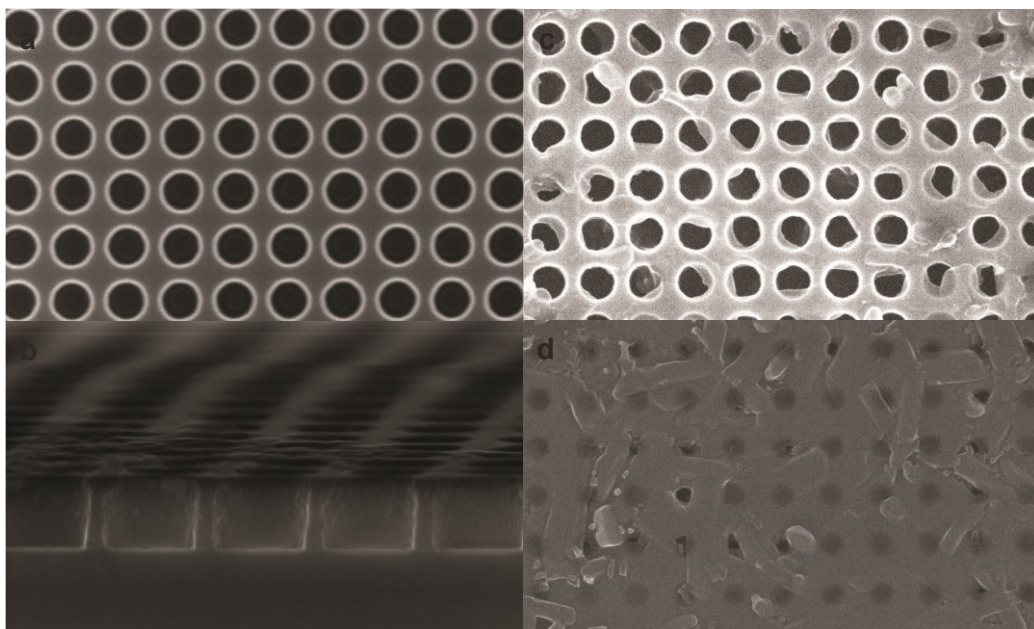


Figure 4: Scanning electron microscope (SEM) images of (a) the hole configuration for the 77nm neck size sample, (b) cross-sectional view of the holes, (c) the 77nm neck size sample after F₄TCNQ deposition and (d) the 161nm neck size sample after F₄TCNQ deposition. The scale bars are 500 μm .

sample with smaller holes (corresponding to 139nm hole diameter) as shown in Fig.4d. We hypothesize that this full coverage occurs before the molecules enter the holes and hence it blocks the pathway to the side walls for the incoming molecules, preventing them from entering the holes. In contrast, the holes of the 77nm sample with larger holes are only covered partially as shown in Fig.4c, allowing molecules to enter the holes. More SEM images and EDS analysis are provided in the supplementary materials.

Finally, F₄TCNQ has a low sticking probability on H-Si(100) [31] and limited wettability making the deposition processes only successful when high flux and long time deposition are used [25]. Considering that the 161nm neck size sample only demonstrates 4 times conductivity improvement compared to the 200 times improvement observed in the 77nm neck size sample (223nm hole diameter), we can infer that in the latter sample, more F₄TCNQ molecules entered the holes and attached normal to the walls. In other words, the 77nm neck size sample has a larger overall surface coverage. However, we note that the difference in the surface area coverage is only a factor of 2.4 and is not enough to explain the large

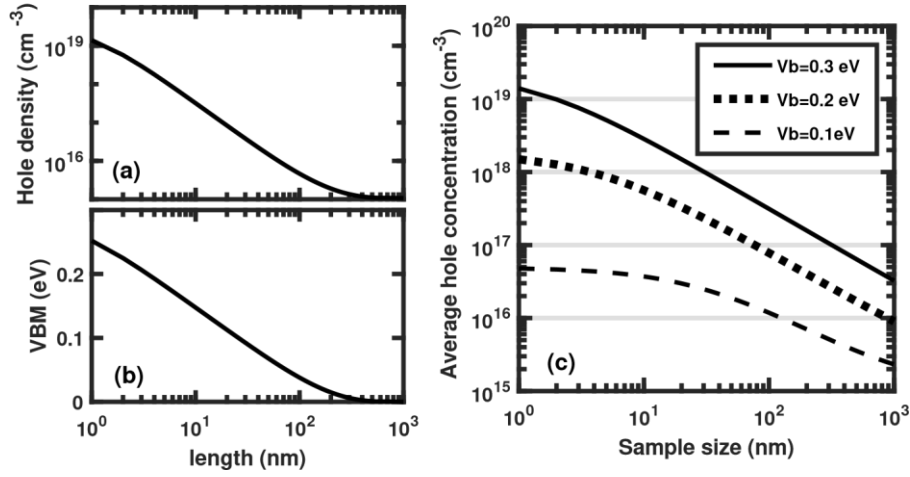


Figure 5: 1D Poisson solver for charge transfer between F₄TCNQ and silicon. (a) Hole density and (b) valence band maximum as a function of the length into the silicon from the surface. (c) Average total hole concentration versus effective sample size, where V_b is the built-in potential.

benefit here.

To explain the large difference, we have developed a 1D Poisson solver to help us better understand the doping effect at the F₄TCNQ-Si interface. The model considers F₄TCNQ as a metal-like source of hole carriers and calculates the charge transfer and the band bending inside the silicon structure, assuming that the Fermi level is pinned by the F₄TCNQ molecules. Parameters of Si, including its effective mass (0.81 for hole and 1.81 for electron density of states effective masses respectively), bandgap (1.12 eV), work function, and dielectric constant (11.7), are well-known [32]. The position of the chemical potential of silicon before F₄TCNQ deposition can be calculated knowing the initial doping density of silicon (10¹⁵ cm⁻³) and it is 0.3 eV below the middle of the gap. Besides the silicon parameters, the relative alignment of the F₄TCNQ energy levels to the bands of silicon determines the amount of charge transfer.

Wang et al.[24] calculated the charge transfer energy of a single F₄TCNQ molecule on a silicon surface using first-principles calculations. They reported that the difference between the electron affinity of the F₄TCNQ molecule and the valence band maxima of silicon is about -0.01 eV and 0.17 eV using PBE and GW calculations respectively. We also note that the levels are modified when studying a single molecule compared to bulk. The electron affinity of F₄TCNQ is reported to be between 5.08–5.24 eV[33] and the work function of Si(100) is

reported to be around 4.91 eV[34]. The difference results in a built-in potential, V_b , between 0.1 to 0.3 eV at the silicon-F₄TCNQ interface, so we have solved for $V_b = 0.1, 0.2, 0.3$ eV using our Poisson model. Charge transfer occurs primarily at the surface and drops rapidly perpendicular to the surface. Hence, we expect a strong size dependence. Figure 5a and b show the charge carrier density and the potential profile (valence band maximum) along a 1D sample respectively. As expected, the doping effect is the strongest at the interface and gradually decreases as we move deeper into the sample. The hole concentration starts from 10^{19} cm^{-3} at the interface (zero length represents the interface of F₄TCNQ and silicon) and slowly drops to the initial doping level of 10^{15} cm^{-3} after over 300nm in length. Figure 5c shows the effect of Fermi level pinning. As the Fermi level is pinned deeper in the valence band, the built-in potential is larger and the charge transfer is also larger.

Let us now map this 1D model onto the 3D geometry. Assuming that in the 161nm neck size (139nm hole diameter) case the dopants either did not enter the holes or if they did, they did not effectively align inside, then only the top surface is doped. The effective size of the sample is the thickness of the film, 220nm. Figure 5c shows that for a size of 220 nm, the carrier concentration can be improved to between 5×10^{15} to $1.1 \times 10^{17} \text{ cm}^{-3}$ depending on the built-in potential. In the 77nm neck size (223nm hole diameter) case, and assuming effective doping from the inner walls, the size is now half of the neck size, 39nm. At this length, the carrier concentration improves to between 2×10^{16} to $7.9 \times 10^{17} \text{ cm}^{-3}$, corresponding to a 20 to 800 times improvement of the conductivity after F₄TCNQ deposition. The overlap of the charges from the top and side surfaces can further increase these numbers.

We conclude that small neck sizes correspond to significantly larger carrier concentrations and enhanced power factors after doping. A smaller neck size also means smaller thermal conductivity, which is advantageous for better zT . In the current study, zT of the 77nm sample reached 0.01 after F₄TCNQ doping, demonstrating 2 orders of magnitude improvement. We, therefore, believe that even smaller neck sizes can further improve the zT .

Here we compare the obtained zT with conventionally doped samples at room temperature. zT of 0.01 in this work is one order of magnitude smaller than that of highly-doped nanocrystalline bulk Si samples ($4 \times 10^{20} \text{ cm}^{-3}$) [35] but is comparable to highly-doped single crystal bulk Si (10^{20} cm^{-3}) [15] and higher than single crystal with mid-level doping ($10^{18} - 10^{19} \text{ cm}^{-3}$) [15, 36]. While our zT is lower than some highly-doped holey Si thin films with smaller thicknesses and smaller neck sizes[10, 12], it is comparable to others[11]. This shows that surface

charge transfer doping via F₄TCNQ deposition is an effective approach to introduce additional charge carriers into Si thin films. The improvement in the thermoelectric performance of holey Si thin films can be further optimized by considering factors including film thickness, neck sizes and surface dopants.

4. Conclusion

In conclusion, we fabricated Si thin films with periodic nm-sized holes from SOI wafers and performed surface charge transfer doping with F₄TCNQ organic molecules. The in-plane thermal conductivity depends on the neck size and changed from 26 Wm⁻¹K⁻¹ to 5 Wm⁻¹K⁻¹ as the neck size decreased from 169 nm to 22 nm. The F₄TCNQ molecules were deposited via thermal evaporation. The sample with a larger hole diameter allowed more space for the F₄TCNQ molecules and the surface doping was more effective. *PF* and *zT* of the 77 nm neck sample improved by 2 orders of magnitude. The large improvement was possible because the holey structure extended the surface doping effect to 3D. This study demonstrates the possibility of building high-performance thermoelectric devices out of an organic-holey Si hybrid structure. Further evaluation of the holey Si geometry, the dopant materials and the manipulation of dopant molecule orientation is expected to bring even more enhancement in the thermoelectric properties. Systems with larger surface-to-volume ratios, such as nanowires, should also benefit from this doping scheme.

Acknowledgments

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Data Availability

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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