Real-time Signal Processing with FPGAs and GPUs for Wideband Interference-resilient Communications

Mark W. Ruzindana, Mitchell C. Burnett, Jakob W. Kunzler, David M. Marsh,
Kayla Lyman, Kyle Evans, Adam Whipple, Karl F. Warnick, Brian D. Jeffs
Department of Electrical and Computer Engineering
Brigham Young University
Provo, USA
ruziemark@gmail.com; warnick@ee.byu.edu; bjeffs@byu.edu;

***Abstract*—For wideband phased array beamforming, multi-port high throughput data acquisition and real time processing systems are required. This paper provides an overview of the development of a phased array receiver system for naval communications. This broadband heterogeneous system enables communication in hostile radio frequency interference (RFI)-rich environments with the aid of a real-time RFI mitigation algorithm currently implemented on graphics processing units (GPUs). The algorithm will be compatible with other phased array and phased array feed (PAF) receiver systems and will enable RFI mitigation in other applications such as radio astronomy. The system will be capable of receiving data from multiple transmitters and employs FPGAs and HPCs with integrated GPUs and FPGAs to process 150 MHz instantaneous bandwidth. This is the first system that we are aware of to demonstrate wideband, real-time RFI cancellation with a heterogeneous, distributed DSP architecture.**

***Index Terms*—phased array, beamforming, signal processing**

I. Introduction

Adaptive phased array beamforming has long been used for anti-jamming and radio frequency interference (RFI) mitigation, but challenges remain for applications that require real-time rejection of interfering signals over a wide bandwidth. Our group has developed wideband array systems for radio astronomy, including the Focal L-band Array for the Green Bank telescope (FLAG) [1]–[3] and the Advanced Cryogenic L-band Phased Array Camera for Astronomy (ALPACA) [4]. These systems process broadband signals (150 MHz or more) from multiple elements or nodes with the help of heterogeneous computing platforms that are comprised of FPGAs and GPUs in HPCs. In this paper, we report on an extension of these heterogeneous signal processing architectures to an adaptive beamforming array for wideband communications for naval applications [5], [6].

II. System Overview

The demonstration system consists of a 16 element phased array and receiver boards which form the front end as well as FPGAs, Ethernet switch, HPCs, and solid state drives (SSDs) which form the back end. A block diagram of the multi-element data acquisition system architecture can be seen in Figure 1. The wireless communication receiver is capable of real-time interference mitigation through adaptive beamforming over a wide bandwidth. Another goal is receiving signals of interest from multiple transmitters. The digital signal processing system performs real-time beamforming, array output voltage correlation, RFI mitigation using subspace projection (SP), and raw voltage capturing. A python interface distributes the processes needed for these functions across multiple HPCs.

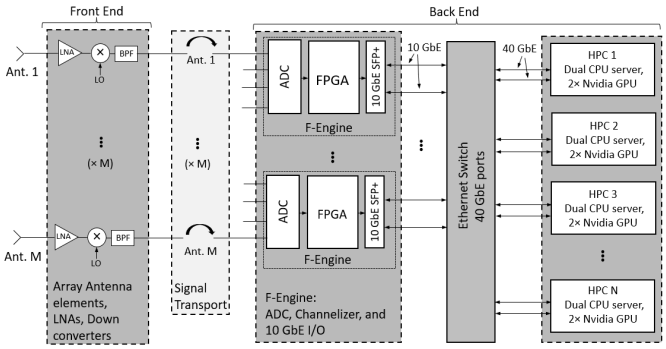

Fig. 1: A block diagram of the standard multi-element data acquisition system implemented in a phased array receiver. The signals are received by the front end which consists of the phased array, amplifiers, mixers, filters, and transported to the back end which is comprised of the heterogeneous computing platform.

The analog front end has an instantaneous bandwidth of 400 MHz and consists of a 16 element patch antenna array with each element connected to a wide-band analog down converter card (also called a receiver board). The card's key features include a first stage low noise amplifier (LNA), real signal chain mixer, and tight final stage band-pass filter to provide signal conditioning before digital sampling.

This research was sponsored by the U.S. Department of the Navy, Office of Naval Research award N00014-18-1-2040.

A receiver board uses a local oscillator (LO) at 10.5 GHz to mix a 10.2 GHz radio frequency (RF) signal down to 300 MHz. The intermediate frequency (IF) signal is then filtered with a 300 MHz band-pass filter that has a bandwidth of 150 MHz (the frequency range is between 225 and 375 MHz). This receiver board has a measured total gain of approximately 66 dB and system noise temperature of approximately 1150 K.

The digital back end is based on that of FLAG which was referenced in the paper. It consists of four Tyan HPCs each containing two GeForce RTX 2080 Ti GPUs and two 10 GbE network interface cards (NIC), three CASPER Smart Network ADC Processor (SNAP) boards each containing three HMCAD1511 ADC analog devices and two 10 GbE cores as well as a Xilinx Kintex7 FPGA (XC7K160T-2FFG676C). The back end also has an Arista DCS-7050QX-32-R data center switch to transfer data from the SNAP boards to the HPCs.

Firmware was developed to break a wideband signal into narrow subbands for frequency domain beamforming [6]. The wideband signal is sampled by ADCs at 400 MHz. The digital signal is then passed to a 256-point FFT. Out of the 128 positive frequency bins, 32 are thrown away to remove the transition band. This results in 96 bins, 1.5625 MHz wide for a total bandwidth of 150 MHz. These 96 bins are then split up into 12 packets containing 8 frequency bins each. Each packet also contains data from each signal input (six per SNAP board in this configuration), 85 time windows, and they are then transferred from the SNAP boards to a port on each HPC and all 12 are processed at the same time.

Currently, there are six receiver boards connected to each SNAP board except for one which is connected to four with this 16 element array configuration. The packets are transferred from the 10 GbE cores of the SNAP boards to the network switch which then transfers the data to the appropriate HPC i.e. the bandwidth is split evenly across the three HPCs.

The data from the network switch is captured and processed in the HPC with software that utilizes the high availability shared pipeline engine (HASHPIPE), and the data is saved to binary files [7]. A net thread is used to capture the packets transmitted by the network switch. A GPU accelerator thread is used to perform one of the operational mode computations in real-time. And finally, a save thread is used to write the data to binary files that are saved to a redundant array of inexpensive or independent disks (RAID) consisting of SSDs. A RAID 0 array was chosen because of the increase in performance, specifically write speed [8].

III. Experimental Results

An example case with two transmitters at different locations radiating tones representing a signal of interest at 10.2185 GHz and RFI at 10.2184 GHz is shown in Fig. 2. The system was configured to operate in two modes, real time beamformer (RTBF) which formed a beam on the SoI but with no RFI mitigation, and real time RFI mitigation mode (XRFI). This plot shows the spectrum of one coarse frequency subchannel of the 96 that make up the total system bandwidth. This demonstrates the capability of the real-time RFI mitigation algorithm

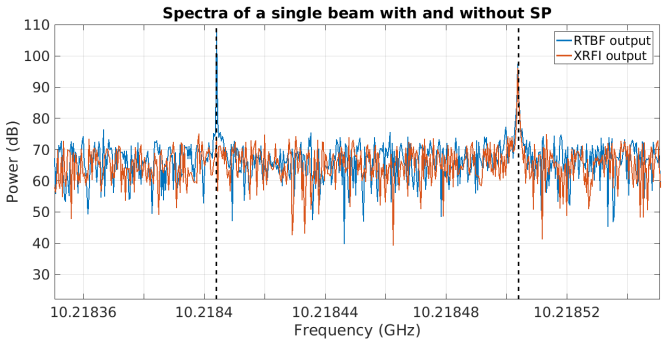

Fig. 2: Real-time beamformer (RTBF) output with no RFI mitigation compared to real time RFI mitigation (XRFI). Vertical lines indicate the frequencies of tones representing SoI and RFI. The RTBF output shows both tones present while the XRFI mode cancels the RFI using subspace projection.

to cancel interference within the same coarse channel with the transmitters located in different positions spatially.

IV. Conclusion

This paper presented an overview of a real-time adaptive beamforming array based on a heterogeneous architecture. The system architecture is currently being used for radio astronomy and wireless communications, and can also be applied to other fields that require real-time beamforming for large antenna arrays. Real-time signal processing including an RFI mitigation algorithm implemented on GPUs will enable wireless communication in hostile-interference rich environments as well as detection of radio sources in the presence of RFI in radio astronomy over a wide operating bandwidth.

References

[1] M. W. Ruzindana, "Real-time beamforming algorithms for the focal L-band array on the Green Bank Telescope," Master's thesis, Brigham Young University, 2017.

[2] R. A. Black, "Phased-array feed instrumentation and processing for astronomical detection, interference mitigation, and transient parameter estimation," Ph.D. dissertation, Brigham Young University, 2017.

[3] M. C. Burnett, "Advancements in radio astronomical array processing: digital back end development and interferometric array interference mitigation," Master's Thesis, Brigham Young University, 2017.

[4] M. C. Burnett, J. Kunzler, E. Nygaard, B. D. Jeffs, K. F. Warnick, D. Campbell, G. Cortes-Medellin, S. Parshley, A. Vishwas, P. Perillat *et al.*, "Design and development of a wide-field fully cryogenic phased array feed for Arecibo," in *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*. IEEE, 2020, pp. 1–4.

[5] M. W. Ruzindana, "Digital signal processing algorithms implemented on graphics processing units and software development for phased array receiver systems," Ph.D. dissertation, Brigham Young University, 2021.

[6] D. M. Marsh, "Phased array digital beamforming algorithms and applications," Master's thesis, Brigham Young University, 2019.

[7] D. MacMahon, "HASHPIPE," https://casper.ssl.berkeley.edu/wiki/-HASHPIPE, 2014.

[8] V. Timcenko and B. Djordjevic, "The comprehensive performance analysis of striped disk array organizations – RAID-0," in *Proceedings of the 2013 International Conference on Information Systems and Design of Communication*, 2013, pp. 113–116.