Compact Inverse Designed Integrated 1 x 3 Silicon Nitride Balanced Optical Power Splitter

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Abstract*— We designed a compact integrated Silicon Nitride 1 x 3 balanced optical power splitter using density-based topology optimization with built-in fabrication constraints. We experimentally validate our design on a commercial foundry process with a splitting ratio of 30-36-33 % and an insertion loss of 2.48 dB across two wafers.** ***Keywords—Silicon Nitride, Integrated Photonics, Inverse Design

Advances in integrated silicon photonics has been a promising direction for developing compact, high bandwidth optical communication systems by taking advantage of silicon-on-insulator (SOI) technology [1]. More recently, Silicon Nitride has been explored due to lower loss, broader wavelength support, and weaker two-photon absorption with devices such as grating couplers [2], 1 x 2 Multi-Mode Interferometers [1], and optical power splitters (OPS) [3], but minimal work has been demonstrated for compact inverse designed structures in SiN.

In this work, we demonstrate a compact, inverse designed 1 x 3 optical power splitter (OPS) fabricated on a foundry process. Our splitter was designed using topology optimization, a gradient-based optimization method that only requires one forward and one adjoint simulation per iteration [4], using MEEP, a 3D electromagnetic Finite-Difference Time-Domain (FDTD) simulation engine with an adjoint solver for inverse design [5]. We optimized 176,400 design variables in a 7 μm x 7 μm region using a minimax algorithm [6] that minimized the error in output power from 33% in each leg across optical C-band (1530 to 1565 nm). Enforcing geometric symmetry due to the balanced splitting ratios reduced the computational cost by a factor of two.

Two objective functions, one for the top leg and one for the center leg (bottom leg is equal to the top leg by geometric symmetry), at five frequency points were evaluated for a total of ten optimized objective functions. The mean transmitter power across frequency, shown in Fig. 1(b), optimizes as the design region evolves with each iteration. The design binarized into a fabricable device by incrementally scaling an inverse tangent projection parameter, β, by 1.5 starting at four, updating at iteration 20, 40, 55, 70, 85, and 115 (seen by large drops in optical power). At iteration 100, we applied fabrication constraints to the optimization problem that enforced linewidth, linespacing, curvature, area, and enclosed-area constraints [7]. The optimization concluded at iteration 135 after 48 hours on 2 nodes, each with 24 processors.

The final simulated device performance, Fig. 1(c-d), exhibited a mean split ratio of 33.8-32.5-33.8 % between the top, center, and bottom legs across 1530 to 1565 nm and a simulated mean insertion loss of 0.91 dB. The steady state fields at 1550 nm are shown on the final design in Fig. 1(a).

We measured two SiN splitters across two different wafers fabricated on the Global Foundries 45CLO process [8]. We used a tunable C+L band laser source (Keysight 8164B) with a 4-channel fiber array to couple light onto silicon-based grating couplers and then to the SiN layer with low-loss transitions. Two s-bends followed the splitter on the top and bottom legs to add more separation, as shown in the inset in Fig. 2(d), and the light was then brought off-chip to three receiving photodiodes. We calibrated the loss of the system with a simple loopback structure.

When measured, the splitting ratio in the top and bottom legs were significantly lower than expected due to lossy s-bends (not included in the design) located directly after the top and bottom legs. To fully characterize the splitter, we subtracted the simulated loss of the s-bends out of the measured data. The final measured data, shown in Fig. 2(a-b), displayed a splitting ratio of 30-36-33 % between the top, center, and bottom, respectively with a maximum variation of 11.1-7.7-13 % (shown in the lighter color for each leg). We measured an insertion loss of 2.48 dB with a maximum variance of 0.67 dB across C-band which was higher than the simulated 0.91 dB, as seen in Fig. 2(c). This loss could be due to abrupt transitions near the interface of the design region and output legs and from surface roughness in the device.

We demonstrated a foundry fabricated novel C-band 1 x 3 optical balanced power splitter in SiN designed using topology optimization and inverse design. Experimental results validated our simulation data across two different wafers with a mean splitting ratio of 30-36-33 % and a mean insertion loss of 2.48 dB. Future work will incorporate inverse-designed s-bends following the splitter to reduce the loss. Furthermore, an implementation of robust topology optimization can be used to optimize over fabrication variability such as over- and under- etching. Finally, a SiN based splitter will enable higher power handling capabilities.

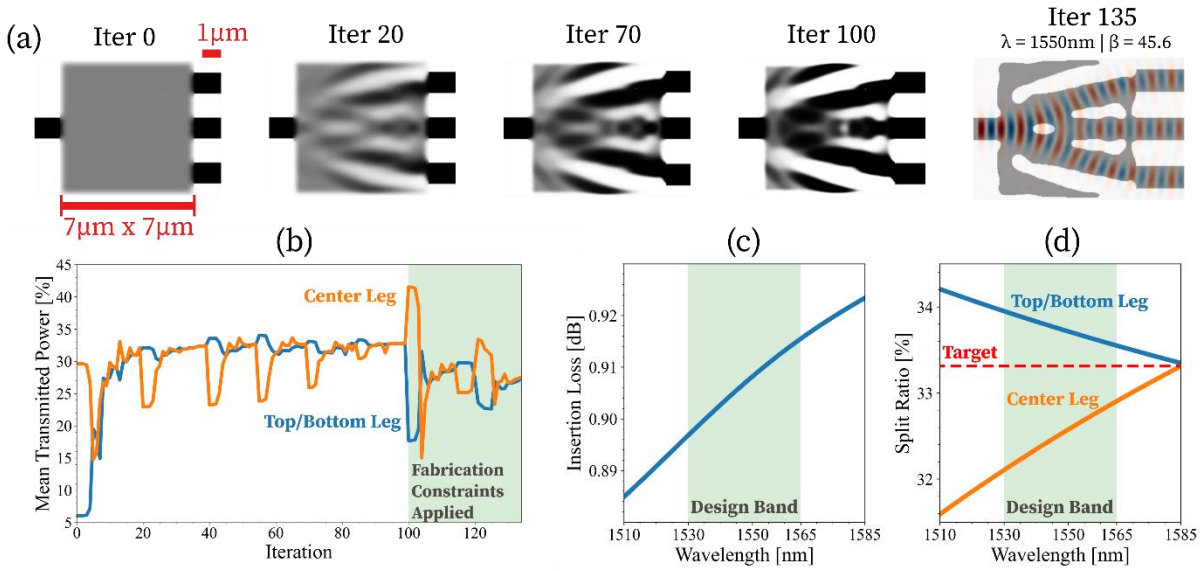

Fig. 1. Design and simulation of 1 x 3 SiN balanced power splitter. (a) The topological evolution of the design region sampled after iteration 0, 20, 100, and 135. The optimization concluded at iteration 135 and the fields are shown overlaying the final binarized design. SiN waveguide (black) and SiO_2 cladding (white). (b) Evolution of the mean transmitted output power through each leg. Geometric symmetry held the top and bottom legs to have identical powers. Each β can be seen by large drops in transmitted power at iteration 20, 40, 55, 70, 85, and 100. At iteration 100, geometric constraints were added to the optimization problem (e.g. linewidth, minimum area, etc.) [7] (c) Simulated insertion loss of the final design. (d) Power splitting ratio between the output legs of the final design. The optimization target was 33.3% over the optical C-band (1530 – 1565 nm).

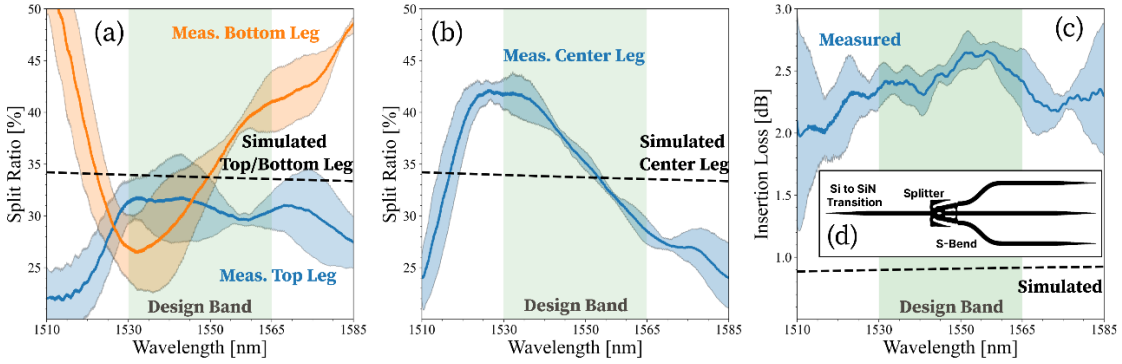

Fig. 2. Experimental measurement and analysis of the SiN splitter. Measurements were taken across two different wafers. Average measured optical splitting ratio between the output legs: (a) top and bottom legs and (b) center leg. The maximum and minimum splitting ratio measured is shown as the lighter colored region. Simulation results are compared with the dashed line. The frequency design band (1530 – 1565 nm) is highlighted in green. (c) Measured insertion loss of the device compared to simulated data. (d) Design layout included Si to SiN transitions and an s-bend on the top and bottom output legs of the splitter. Due to lossy s-bends, the simulated loss of the s-bends was de-embedded out of the measured data to obtain the estimated splitter performance.

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