An 8T/Cell FeFET-Based Nonvolatile SRAM with Improved Density and Sub-fJ Backup and Restore Energy

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***Abstract*—In normally-off instant-on applications, power-gating of the embedded memory is an effective way for higher power efficiency by preventing long-standby-time leakage energy. Recent efforts of nonvolatile SRAM (nvSRAM) design with in-cell NVM element backup provide an efficient way for both normal-mode computing and off-mode backup and restore (B&R) operations. For these efforts, circuit innovations are required to achieve optimal balance between B&R energy and area overheads. In this paper, we report a novel 8T/cell FeFET-based nvSRAM design that outperforms prior FeFET-based designs with higher density, while still maintaining the advantage of only sub-fJ energy for each B&R operation, 363x lower than the existing RRAM-based nvSRAM design. Compared with prior FeFET-based designs, this design reduces the B&R transistor count per cell from 4 to only 2, which leads to a significant total area overhead reduction of 11%.**

***Keywords*—Ferroelectric FET (FeFET), nonvolatile SRAM (nvSRAM), nonvolatile memory (NVM), SRAM, power gating, intermittent computing.**

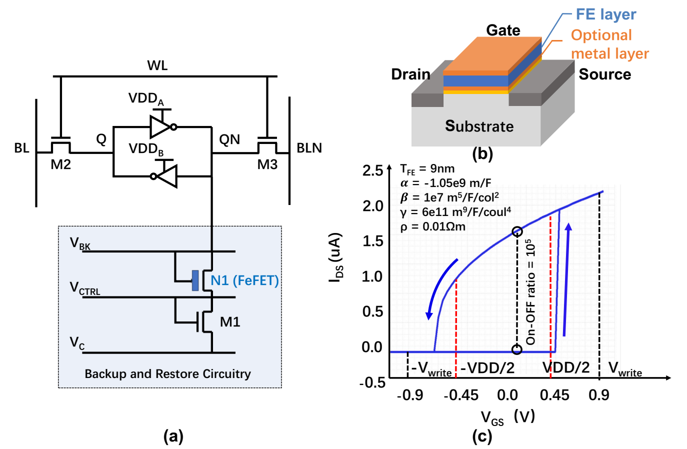


Fig. 1. Proposed FeFET nvSRAM: (a) circuitry; (b) FeFET basic device structure; (c) *I-V* curve of a typical N-type FeFET.

I. INTRODUCTION

In the power-gating and energy-harvesting applications, the data stored in embedded memory arrays need to be properly saved to avoid data loss or computing progress loss during the supply outage, and then restored when the power supply recovers [1][2]. Although some nonvolatile memory (NVM) technologies, such as RRAM, PCM-RAM, and STT-MRAM, have been proposed as candidates to replace the CMOS SRAM, they still face unsolved challenges of high-power consumption or limited lifetime [3]-[6]. As a result, by harnessing the nature of less frequent B&R requests than normal write access, a hybrid memory cell design consisting of CMOS SRAM and emerging NVM, i.e. nvSRAM, has been considered as a preferred option to ensure robust normal-mode read and write memory access and *in situ* parallel B&R operations [7]-[9].

For such nvSRAM designs, it is critical to achieve an optimal balance between the normal mode and B&R mode, especially for the memory density and the B&R energy overheads, i.e. $E_{B\&R}$. Density is critical as it limits the maximum memory capacity, especially when device scaling is becoming more challenging nowadays. $E_{B\&R}$ is also pivotal since it limits the break-even time for power-gating applications and the total power budget in energy-harvesting applications.

Several pioneering nvSRAM designs [7], [10]-[13] have been proposed, showing the promise of nonvolatile parallel state B&R while maintaining the robustness, high speed, and power efficiency advantages of the CMOS SRAM technology [14]. Some of these nvSRAM designs are based on the RRAM technology, leading to cell structures of 7T1R [11], 7T2R [12], etc. Some are based on MTJ [7]. There are also newly proposed nvSRAM designs based on ferroelectric field-effect transistors (FeFETs) [10][13]. The beauty of FeFET-based nvSRAM is the opportunity of DC-power-free B&R operations, which leads to $E_{B\&R}$ improvement by orders of magnitude. FeFETs are also highlighted with excellent compatibility with advanced CMOS process, and improved device variation considering the large on-off ratio. However, existing FeFET-based nvSRAM designs suffer from lowered density due to the extra B&R transistors (8 in [10] and 4 in [13]).

We notice that the symmetry of the differential B&R unit in [13] has redundancy. Inspired by [11], in which the supply for the two inverters of an SRAM is separately controlled, this paper proposes a new 8T/cell nvSRAM shown in Fig. 1(a), which achieves 50% transistor count reduction of the B&R circuitry, from 4 in [13] to only 2 in this work, while still achieving sub-fJ $E_{B\&R}$ by harnessing the FeFET features of DC-power-free backup operations and the ultra-high on-off ratio during restore operations.

This paper presents the operation details and optimization of the proposed 8T/cell nvSRAM. After introducing the FeFET technology in Section II, circuit simulation results and evaluation will be provided in Section III, along with detailed analysis and discussions. Section IV concludes this paper.

II. PROPOSED FEFET NVSRAM OPERATIONS

This section briefly introduces the FeFET device characteristics, and then describes the operations of the proposed FeFET-based nvSRAM in three working modes: the

SRAM mode, the backup mode, and the restore mode. The optimizations and device-circuit co-design are also discussed in this section.

A. FeFET Device Characteristics

The recently emerged FeFET is essentially a field-effect transistor (FET) which has an enhanced gate stack that sandwiches an extra ferroelectric (FE) capacitor, as shown in Fig. 1(b) [15][16]. Benefiting from the newly discovered HfO_2-based Zr-doped material, FeFET has exhibited appealing compatibility with advanced CMOS process down to several nanometer. FeFETs are also reported to be capable of operation down to below 2V [17]. The ferroelectric non-volatility has been presented as a reconfigurable threshold voltage V_T, as shown in Fig. 1(c). The V_T tuning does not consume DC power, thanks to the FE capacitor nature. FeFETs have also shown an ultra-high on-off ratio owing to the embedded transistors [18].

In the proposed nvSRAM, an n-type FeFET is adopted. While a FeFET could exhibit multiple V_T (and thus multiple I_{DS}-V_G curves) [19] [20], its operation in this work is manipulated in a simplified binary manner: the positive and the negative V_T states [21]. In the positive V_T state, the transistor is treated as turned-off. In the negative V_T state, the transistor is treated as turned-on. To switch from the positive V_T state to the negative V_T state, a positive V_{GS} beyond the coercive voltage is needed. Similarly, the transition is triggered from the negative V_T state to the positive V_T state by applying a negative V_{GS} beyond the negative coercive voltage. The coercive voltage could be tuned by the Fe thickness (T_{FE}) and the Fe capacitance matching with the internal gate capacitance. Our experiment reveals the coercive voltage rises from 0.4 to 0.75v as the T_{FE} rises from 8 to 12nm. In the simplified model in Fig. 1(c), when V_{GS} is beyond the falling or rising edge, the FeFET will enter the negative or positive V_T state, respectively. When V_{GS} is within the coercive voltage range, the FeFET polarization state does not change and thus the FeFET operates with the original high or low drain-to-source channel resistance, for positive and negative V_T, respectively.

There have been several FeFET compact models. Based on the model in [22]-[24], quite a variety of FeFET-based circuits have been reported, including nvFA, nvDFF, nvSRAM, NVM, compute-in-memory circuits and FeFET-based CAM [25][27], [29]-[33], [37][38]. Unless otherwise stated, the adopted FeFET parameters are the same as those in [13], as listed in Fig. 1(c).

B. SRAM-Mode Operation

When the proposed nvSRAM shown in Fig.1 (a) is in the SRAM mode, the nvSRAM operates just like a conventional SRAM, with the two supply voltages VDD_A and VDD_B kept at *VDD*. The gate voltage, V_{CTRL}, of the access transistor M1, and V_C are kept at *GND*. As a result, M1 is turned off and the whole B&R circuitry is in a high-resistance turned-off state for the SRAM. Therefore, the B&R circuitry does not affect the SRAM core, and the read and write operations of the remaining circuit could be the same as the traditional 6T SRAM.

Considering the limited endurance of FeFETs, and to prevent unnecessary FeFET polarization switching power consumption, the only mode that may switch the FeFET polarization state is the backup mode. Therefore, in the SRAM mode, the supply

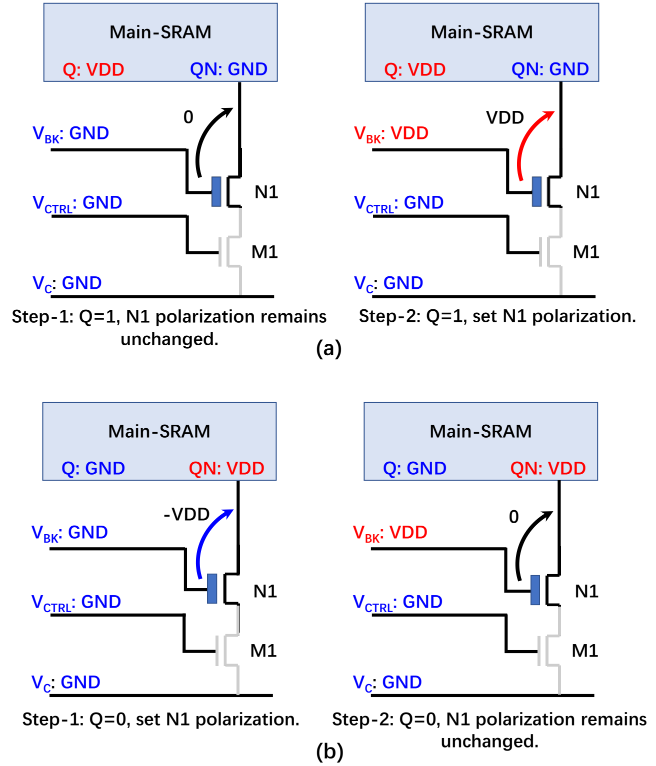


Fig. 2. Steps to back up SRAM data into FeFET in the proposed nvSRAM. (a) Case where Q equals to '1' (*VDD*). (b) Case where Q equals to '0' (*GND*).

voltage and the biasing voltage of the FeFET, i.e. V_{BK}, needs to be optimized (the maximum $|V_{GS}|$ of the FeFET N1 is $VDD/2$, as shown in Fig. 1(c)). In this work, V_{BK} could be set at $\sim VDD/2$, so as to minimize the voltage stress applied to the Fe layer in the gate stack. Depending on the normal-mode operation speed and normal-mode leakage trade-off, the preferred *VDD* could be chosen, and the FeFET polarization switching hysteresis (mainly the hysteresis window width) could be designed accordingly based on T_{FE} and the capacitor matching between the Fe capacitor and the gate capacitor.

C. Backup-Mode Operation

The backup operation, which stores the 1-bit SRAM datum into the polarization state of FeFET, is shown in Fig. 2. In this mode, V_C and V_{CTRL} are kept at *GND* to avoid DC power consumption. The access transistors of SRAM, i.e. M2 and M3, are turned off by setting *WL* to *GND*. V_{BK} was initially set at $VDD/2$, as mentioned above in Section II.B. When the backup operation starts, V_{BK} is set to *GND* first in step-1, *VDD* subsequently in step-2, and then back to its original value of $VDD/2$, as illustrated in Fig. 2.

There are two SRAM data backup cases: '0' backup and '1' backup. The backup of bit '0' and bit '1' occurs at different steps (step-1 or step-2). As shown in Fig. 2, if Q and QN equal '1' and '0', respectively, lowering V_{BK} to *GND* makes V_{GS} of the FeFET be zero, leading to no polarization state change in step-1. Next, in step-2, raising V_{BK} to *VDD* makes V_{GS} of the FeFET be *VDD*, which triggers beyond-coercive voltage at the internal Fe layer. Thus, the FeFET could be polarized to the positive polarization state with a negative V_T, leading to low drain-source channel resistance.

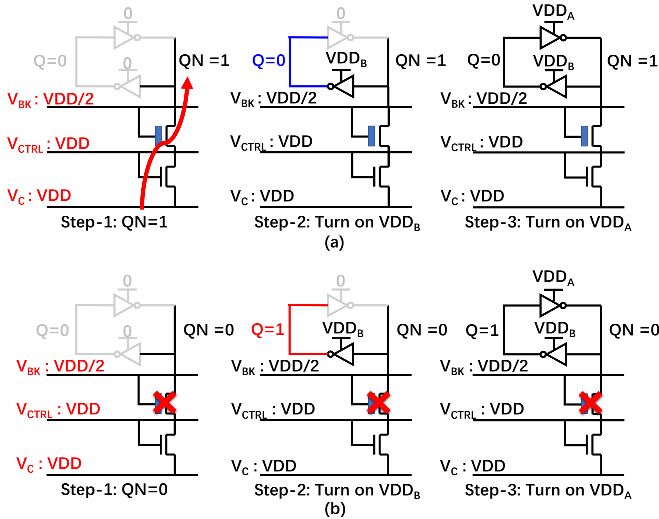


Fig. 3. Steps to restore SRAM data in the proposed nvSRAM. (a) Case when FeFET has a low drain-source resistance state. (b) Case when FeFET has a high drain-source resistance state.

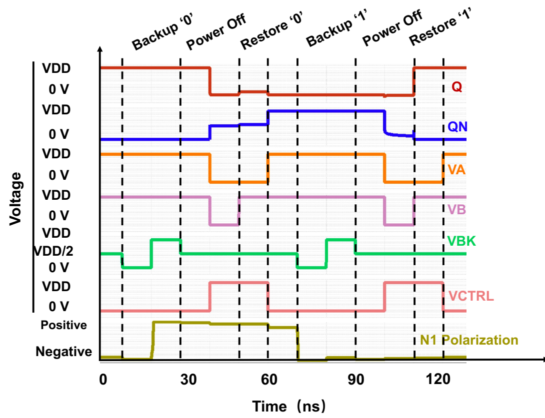


Fig. 4. Simulated transient waveforms of the proposed nvSRAM.

If Q and QN equal to '0' and '1', respectively, lowering V_{BK} to GND in step-1 makes V_{GS} of the FeFET be $-VDD$, which is beyond the negative coercive voltage. Thus, the FeFET will be polarized negative with a positive V_T, leading to high drain-source channel resistance. Next, in step-2, raising V_{BK} to VDD leads to zero V_{GS} and no FeFET polarization state change.

After the two steps, V_{BK} returns to $VDD/2$, and the SRAM data backup operation is finished. Fig. 4 shows the transient waveforms in SPICE simulations, including the backup operations for both '0' and '1' at $VDD = 0.9$V.

D. Restore-Mode Operation

The restore-mode operation includes three steps, as illustrated in Fig. 3. It is noted that V_C and V_{CTRL} are initially kept at VDD, and V_{BK} is kept at $VDD/2$. Before the restore operation starts, both supplies of the two inverters in the SRAM core, i.e. VDD_A and VDD_B, are grounded. In the first step, if the FeFET has been set to positive polarization with a negative V_T, the VDD voltage of V_C could reach the node QN through the FeFET N1 and the MOSFET M1, leading to charged QN to $VDD - V_T$. Otherwise, QN will remain at GND due to the previous power off phase. In the second step, VDD_B is turned

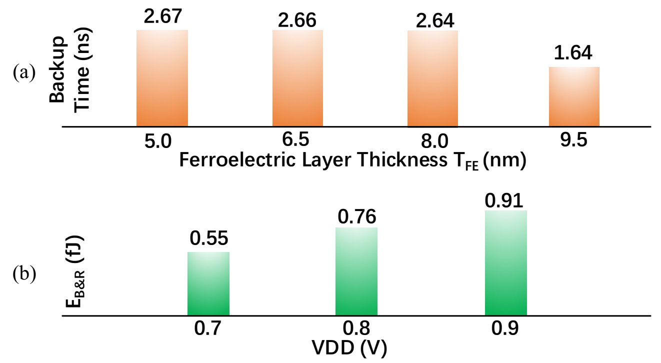
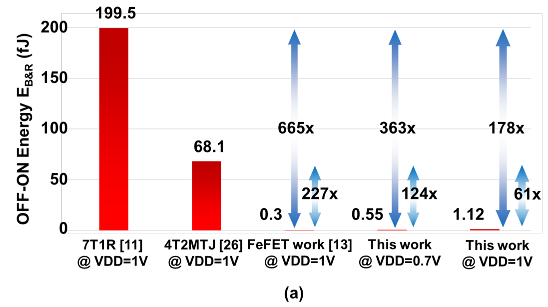


Fig. 5. (a) Impact of T_{FE} on backup time. (b) Impact of $E_{B\&R}$ on VDD.



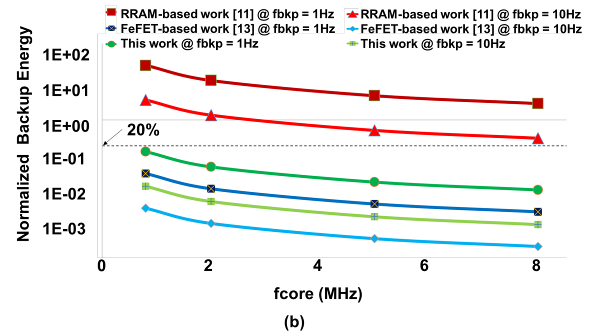


Fig. 6. $E_{B\&R}$ benchmark: (a) comparisons with prior MTJ, RRAM, and FeFET-based nvSRAM; (b) comparisons at a varying SRAM access frequency (100% indicates equal energy for B&R and normal access).

on while VDD_A remains grounded. As a result, Q is driven by the inverter powered by VDD_B. In the third step, VDD_A is also turned on, and the two inverters form a stable loop. Transient waveforms in Fig. 4 include the restore operations for both '0' and '1' at $VDD = 0.9$V.

It should be noted that (i) the restore operation does not change the FeFET polarization state, and that (ii) the restored bit to the SRAM is opposite to the original bit that was backed up into the FeFET, as QN = '0' at the backup phase will enable positive FeFET polarization with a negative V_T, which leads to the low-resistance path from VC=VDD to the finally retored QN=VDD. To compensate such an effect, an indicator bit for the nvSRAM array could be used during the SRAM read operation to ensure correct data read.

E. Device-Circuit Co-Design

The design of the proposed nvSRAM includes several key features, including the backup and restore energy $E_{B\&R}$, endurance, and backup time. Generally, a tradeoff could be

applied between the endurance and backup time by adopting a different *VDD*, as increasing *VDD* helps to reduce the polarization switching time but harms the FeFET device lifetime (as well as consuming higher $E_{B\&R}$). To work under a given *VDD* range, tuning of the FE layer thickness (T_{FE}) could be applied, as mentioned earlier. Fig. 5 provides simulated $E_{B\&R}$ and backup time as a function of *VDD* and T_{FE}, respectively, in which the trends could be observed to guide the circuit design.

III. Performance Evaluation and Discussions

This section begins with some performance evaluations of the proposed nvSRAM and compares with previous works. Then, some other device-related features are discussed to get more comprehensive evaluations.

A. Performance and Area Evaluations

Several recent nvSRAM works are compared, including the 7T1R RRAM-based nvSRAM from [11], 4T2MTJ nvSRAM from [26], and the 10T FeFET-based nvSRAM [13]. In the evaluations, the proposed 8T nvSRAM design achieves 1.12fJ and 0.55fJ $E_{B\&R}$ at *VDD*=1.0V and *VDD*=0.7V, respectively. Fig. 6 compares $E_{B\&R}$, in which the 7T1R RRAM-based nvSRAM, 4T2MTJ nvSRAM consumes >178x and >61x higher energy than this work, respectively. Such energy improvement is mainly the result of the DC-free power-consumption characteristic of FeFET.

To evaluate these works in a practical scenario, we take the low-power Narrowband Internet of Things (NB-IoT) for low-cost devices as an example [28]. The eDRX mechanism in NB-IoT specifies the timers to deactivate monitoring so that the power can be turned off periodically to save battery [34]. We obtain the total $E_{B\&R}$ in different backup frequency (fbkp) with a varying normal-mode read and write frequency (fcore). As shown in Fig. 6 (b), with significantly reduced $E_{B\&R}$, this work achieves ultra-high backup energy efficiency (normalized by the normal memory access energy) to lower than 0.75% at a typical scenario of fcore = 2MHz and fbkp = 10Hz. Compared with the prior 10T FeFET-based nvSRAM [13], which has normalized efficiency of 0.20%, little energy performance difference could be observed (only 0.5%) at the system level for many low-power IoT applications.

More importantly, compared with the prior 10T FeFET-based nvSRAM [13], the area overhead of the B&R unit is reduced with a halved number of B&R transistors. A layout comparison of the nvSRAM is shown in Fig. 7. The overall area reduction is also significant, about 11% considering the additional control and voltage supply wires. The area comparison is summarized in Table I. The reduction of area overhead increases the nvSRAM density, which is beneficial to reduce the overall area cost or to support a larger embedded cache.

B. Endurance, Voltage Control Strategy, and Design space

The FeFET programming lifetime is currently reported to be as high as 10^9-10^{12} [35], limited by the gate stack degradation of charge trapping and trap generation. The FeFET technology is also being improved with prolonged data retention time and

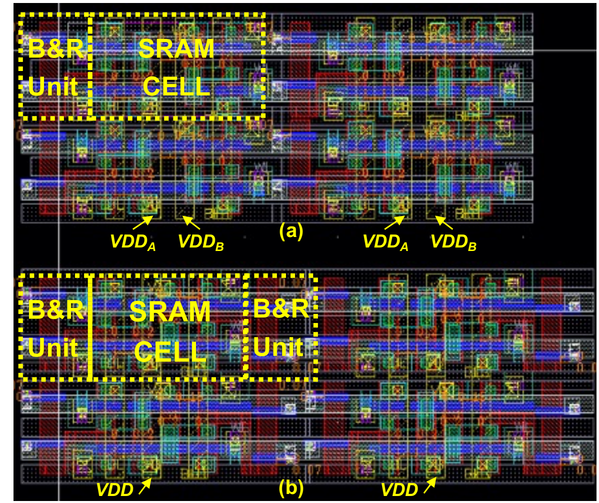


Fig. 7. 2×2 layout of (a) proposed nvSRAM and (b) prior 10T-nvSRAM.

TABLE I
Area comparison between the proposed nvSRAM, normal SRAM and previous 10T-nvSRAM.

Structure	Area/cell (μm^2)	Normalized area
6T-SRAM	1.09	1
10T-nvSRAM [13]	1.56	1.429
This work	**1.39**	**1.278**

endurance [36]. The ultra-high on-off ratio makes the functionality plausible even if the *I-V* degrades with a lower on-off ratio due to overuse. In addition, the voltage supply in the restore operation requires additional control separately to ensure that the SRAM loop is built step by step. Further layout optimizations of reducing the area overhead of the separated VDD_A and VDD_B supply is meaningful for denser layout footprint. Even the endurance of reported FeFETs is sufficient for energy harvesting and power-gating systems where the B&R operation is much less frequent than the SRAM access. The increased data density by this work can further improve the on-chip cache capacity to reduce the activity of energy-consuming off-chip data transfer, showing its potential for data-intensive low-power IoT devices.

IV. Conclusion

This paper has presented a new nvSRAM design based on FeFET. While the device retains the SRAM structure to support SRAM-preferred applications, the backup and restore circuit has been constructed by only two transistors for intermittent computing. In the proposed nvSRAM, the area for B&R functionality is significantly reduced and the B&R energy is also kept low by harnessing the unique FeFET characteristics.

V. Acknowledgment

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