On the Write Schemes and Efficiency of FeFET 1T NOR Array for Embedded Nonvolatile Memory and Beyond

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***Abstract*—Ferroelectric field-effect-transistor (FeFET) 1T NOR Array is promising for multiple applications yet not well studied on its write mechanism and schemes. In this work, we demonstrate: i) A comprehensive model which reflects two FeFET write mechanisms – one to ground Source (S), Drain (D) & Body (B) nodes and use Gate (G) to write, and the other to float S/D and use G & B to write; ii) 3 write schemes for conventional FeFET 1T NOR arrays and another one for the diagonal array, the latter of which shows the advantages of low write energy and high write efficiency but with the penalty area cost; iii) A study of parasitic parameters, particularly gate resistance (R_g), gate capacitance (C_g) and word line resistance (R_{WL}), in FeFET 1T NOR array, which is critical for further prospective 1T NOR array design; iv) An implementation of FeFET 1T NOR array in the Ising machine system to evaluate the feasibility of our write scheme and array structure for embedded nonvolatile memory (NVM) applications.**

I. Introduction

Ferroelectric-HfO_2 based FeFETs have become a competitive candidate for embedded NVM [1]. It shows many promising characteristics such as excellent write energy efficiency, high scalability and CMOS-compatibility [2], which can be utilized in a variety of fields and significantly helps to improve the performance of related applications. There are 2 main single transistor FeFET array structures widely considered in applications. The structure of 1T AND array (Fig. 1(a)) is characterized by parallel bit lines (BL) and source lines (SL), running in perpendicular to the word lines (WL). Due to this structure, 1T AND array has been well explored [3] and widely used in the fields of memory, such as 1T memory array and ternary content-addressable memory (TCAM) [4]. Another common structure is the NOR array (Fig. 1(b)), where the BL and SL run in perpendicular and one of which is parallel to the WL. 1T NOR array also has a wide range of applications [5]. For example, it can be used as routing switches for FPGA [6] (Fig. 1(c)), as weight cells in a crossbar array to accelerate multiplication-accumulation computations in neural network accelerators [7] (Fig. 1(d)), and as interaction controller between artificial spins in Ising machines (Fig. 1(e)). Though many interesting applications exist, the write operations and efficiencies in 1T NOR array have not been well studied, unlike the 1T-AND array counterpart.

In this work, we propose four write schemes for FeFET 1T NOR array. Three of them are based on conventional 1T NOR array structure and each comes with its own advantages and issues. To solve the issue of poor write performance and potentially large power consumption in the three schemes, we propose a novel array structure where the WLs run in diagonal. It is the goal of this work to perform a comprehensive experimental and theoretical evaluation of different write schemes and impact of parasitics on the write efficiency.

II. Write Mechanisms and Modeling of Single FeFET

The conventional FeFET write mechanism is to ground S, D, & B (Fig. 2(a)). When applying a positive write pulse to G, the screening electrons in the channel are provided by S/D so that the voltage on the ferroelectric layer (V_{FE}) can switch the polarization (P_{FE}) and set the device. Similarly, when applying negative write pulse to G, the hole supply from B enables P_{FE} switching for reset process. Another possible mechanism is to float S/D and use G & B to write. The reset operation is the same as the conventional one while the negative charge required by the set operation is from the depletion charge in the substrate. In summary, set is determined by V_{GS} & V_{GD} while reset by V_{GB} for conventional mechanism, while for float S/D mechanism both set and reset are by V_{GB}. To show this possibility, we adapt our previously developed FeFET model [8] and include the floating S/D write mode, (Fig. 3(a)). The ferroelectric is composed of independent domains where the switching probability for each domain can be computed at each time step (Fig. 3(b)). Then, Monte Carlo simulations of polarization switching are executed. P_{FE} and the electric field on the ferroelectric layer are solved. To study two different write mechanisms, the charge equation in the interlayer/ semiconductor layer is modified to include the float S/D situation (Fig. 3(c)). When writing through B, the charge equation is like one of a Metal-Ferroelectric-Semiconductor (MFS) Junction. Both (Fig. 3(d)) simulation and (Fig. 3(e)) experimental results show a memory window (MW) loss when float S/D. Due to the reduced charge supply from B's depletion compared to S/D, V_{FE} is lower and P_{FE} switch is insufficient (Fig. 3(f)).

III. Proposed Write Schemes For FeFET 1T NOR Array

A. Conventional 1T NOR Array

The first proposed write scheme separates the write operation into two stages: the erase stage and program stage. The 1T-NOR array architecture and set/reset voltage applied on each line for this write scheme is shown in Fig. 4(a). During the

erase stage, all the FeFETs in a block are set to the low-VTH state (LVT) by the ground S/D mechanism. Then, in the program stage, only target cells are reset to the high-VTH state (HVT) by applying $-V_W$ on G and ground B. Since other cells' V_{GB} are either $-V_W/2$ (half-selected) or 0 (disturb-free), their states will not be reset to HVT. As a result, individual reset is achieved. The implementation of this write scheme is simple, but due to the block set process, any set on a single cell will result in an abundant block set and individual reset process. The second scheme is the local body contact scheme, whose architecture and detailed applied voltage is shown in Fig. 4(a). Its reset process is the same as the first one and it can also set the FeFET to LVT individually because other cells' V_G and V_{GD} are either $V_W/2$ (half-selected) or 0 (disturb-free) during set. However, the cells in the same column with the target cell will have large write currents due to large V_G & V_{DS}, causing high write power consumption. The third scheme utilizes float S/D mechanism to write, in which case FeFET's state is determined only by V_{GB}. Its architecture and detailed voltage is shown in Fig. 4(b). All cells in the array except the target cell are either half-selected or disturb-free, so the scheme provides individual set/reset. However, the write scheme will face the aforementioned MW loss problem due to insufficient P_{FE} switch. The floating node is realized by using a tristate buffer in the circuit. Our experimental results (Fig. 5) indicate that for the target cell, the proposed 3 write schemes can set/reset it successfully, without disturbing half-selected cells and disturb-free cells.

B. Diagonal 1T NOR Array

Besides the 3 write schemes based on the conventional 1T NOR array, one scheme with the diagonal architecture is proposed. The diagonal 1T-NOR array architecture and set/reset voltage applied on each line are shown in Fig. 6(a). All WLs in the array are diagonal instead of horizontal so that the voltage on the word line (V_{WL}) is not shared in the same row. During set, only the target cell's V_{GS} & V_{GD} is V_W and others' are $\pm V_W/2$ (half-selected) or 0 (disturb-free), ensuring no write disturbance. And since all FeFETs are turned off, no large write current is generated. Similarly, for reset only the target cell's V_{GB} is $-V_W$ for correct write. The proposed diagonal scheme is verified by set (Fig. 6(d))/ reset (Fig. 6(e)) experiments. The diagonal write scheme can achieve both low write energy and high write efficiency, but compared to the layout of conventional 1T NOR array (Fig. 4(b)), the diagonal array (Fig. 6(b)) is 3.5 times of the area.

IV. Study of Parasitic Parameters in FeFET 1T NOR Array

In order to explore the feasibility of our proposed schemes in reality, the delivery of V_{WL} on each cell in the FeFET 1T NOR array is investigated. The simulation waveform shows that V_{WL} will drop gradually as the cell approaches towards the end of WL (Fig. 7(a)), which will cause write failure in large arrays. Thus, it's necessary to investigate the impact of parasitic parameters for our write schemes. In our study, main parameters with regard to leakage current (I_L), displacement current (I_{dis}) and R_{WL} are studied (Fig. 7(b)).

The simulation results demonstrate that V_{WL} drops with the increasing array size (Fig. 8(a)) due to larger parasitic RC. To mitigate this issue, we provide one solution of applying an additional control bias (V_{WL}) on the other end of the selected WL (Fig. 8(b)). In this way, the reduced voltage will be raised up and finally obtain the same V_{WL} drop as that for the half array size case (Fig. 8(c)).

In this study, as Fig. 9(a) illustrates, we investigate the impact of I_L and I_{dis} by considering R_g and C_g respectively. Fig. 9(b) demonstrates the transient waveform of V_{WL} on different cells. As we can see, the write time is mostly affected by I_{dis} (C_g), especially the last cell on WL. In addition, we find out that I_L is the largest when all FeFETs are in LVT due to larger tunneling current in LVT of FeFET (Fig. 9(c)). Therefore, we take this as the worst case and use this condition for the rest of the study. We also explore the relationship between I_L and the array size. With the array size increasing, I_L is increasing and become saturated finally. This is because the large voltage decreasing near the end of WL will cause a negligible I_L per cell, leading to the I_L saturation after array size larger than 2^{24}. Moreover, we find out that the reduction of oxide thickness would increase I_L and cause a larger V_{WL} drop along the line (Fig. 9(e)).

The parasitic parameter of R_{WL} is also critical and should be considered in practice. Fig. 10(b) shows a large impact of R_{WL} on V_{WL} towards the end of WL. As R_{WL} gets larger, V_{WL} will drop accordingly. When considering the condition of R_{WL}=5Ω, the V_{WL} drop for the diagonal array is almost 2 times as that for the conventional array (Fig. 10(c)). However, in our case, the resistance of interconnect ($R_{interconnect}$~10Ω) is negligible compared to the R_{WL} (~250 Ω), thus the V_{WL} drop is similar for these 2 types of arrays (Fig. 10(d)).

Our experimental results demonstrate that the FeFET fails to be set when $V_{WL} < 3.25$ V (Fig. 11(a)) and reset when $V_{WL} < 3.5$ V if assuming MW needs to be above 1 V.

Besides, we successfully implement our FeFET 1T NOR array in one Ising machine system built using bistable latches (Fig. 11(c)-(h)). The simulation results show that the system with the proposed FeFET 1T NOR array write scheme can solve the MaxCut problem effectively and the solution is stable.

V. Conclusions

In summary, we have proposed 4 write schemes for FeFET 1T NOR array. From the perspective of area density, power consumption, write efficiency and circuit complexity, they show different advantages and challenges (Fig. 12). The best write scheme is application specific. The study of parasitic parameters provides critical metrics to consider when designing a FeFET 1T NOR array. Our work is a fundamental approach for prospective FeFET 1T NOR array implementations as embedded NVM and beyond.

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References: [1] S. Salahuddin et al. , "Nature Electronics 2018; [2] S. Dünkel et al., IEDM 2017; [3] K. Ni et al., IEEE EDL 2018; [4] X. Yin et al., TCAS II 2019; [5] M. Ullmann et al., Integrated Ferroelectrics 2001; [6] X. Chen et al., IEEE TCAS I 2019; [7] M. Jerry et al., IEDM 2017; [8] S. Deng et al., VLSI Symp. 2020

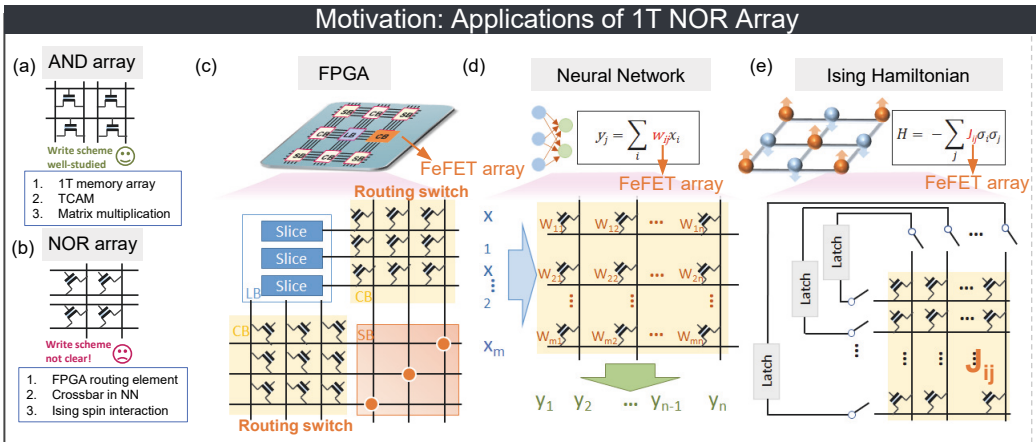

Fig.1. Structures and applications of 1T-FeFET (a) AND array and (b) NOR array. FeFET 1T NOR array is promising for (c) connection box in FPGA, (d) crossbar memory in neural networks and (e) spin interaction in the Ising model. However, the write scheme of 1T NOR array is not so well studied as for 1T AND array.

Fig.2. FeFET can be set and reset with (a) ground S/D/B or (b) float S/D.

Study of S/D Write and B Write using model simulation

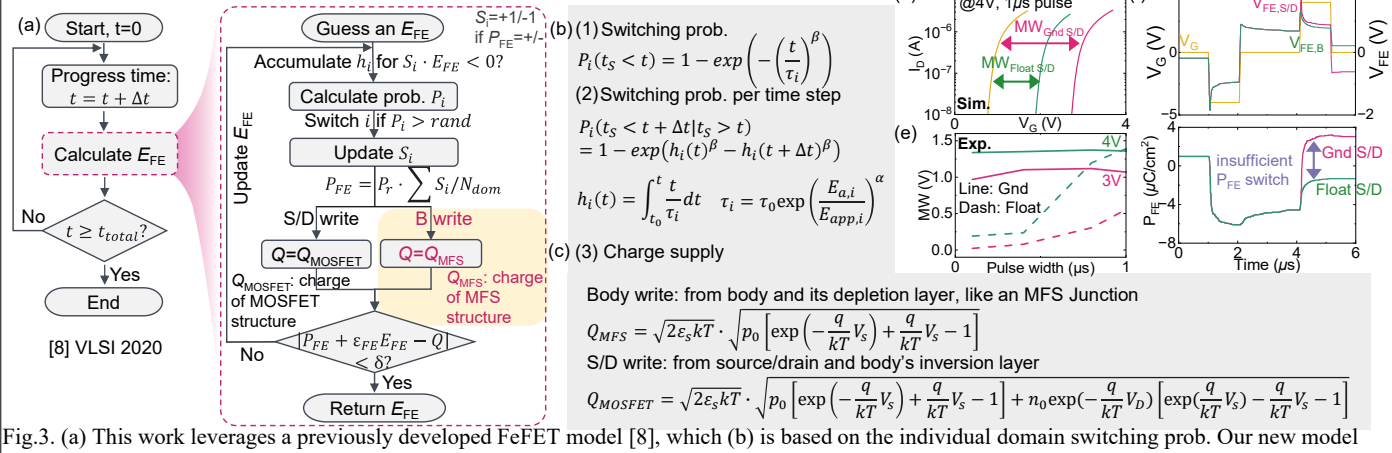

Fig.3. (a) This work leverages a previously developed FeFET model [8], which (b) is based on the individual domain switching prob. Our new model modifies (c) the charge equation in the IL/Semiconductor layer when using B to write. Both (d) simulation and (e) experimental results show a MW loss when float S/D. It is because (f) V_{FE} is lower and polarization switch is insufficient when float S/D due to the reduction of charge supply from B write.

Proposed Write Schemes of Conventional FeFET 1T NOR Array

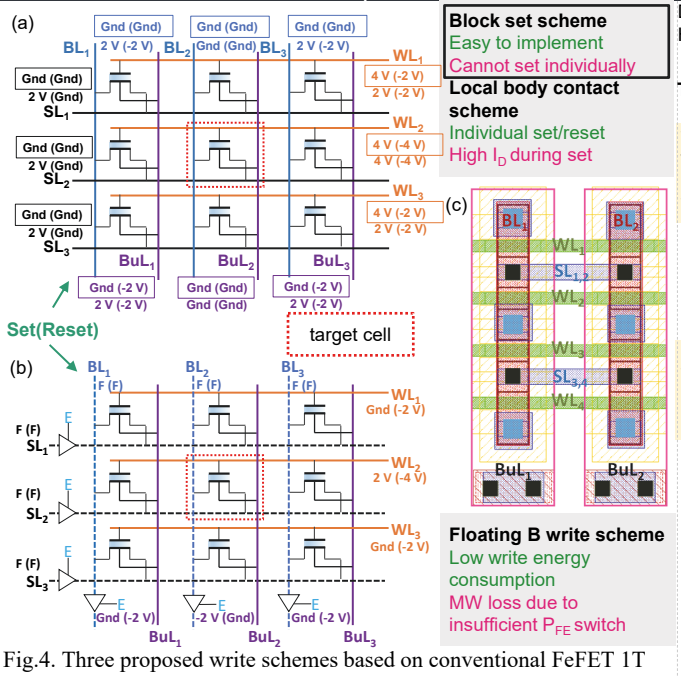

Fig.4. Three proposed write schemes based on conventional FeFET 1T NOR array: (a) erase-program scheme and local body contact scheme, (b) floating B write scheme. (c) The layout of these three write schemes.

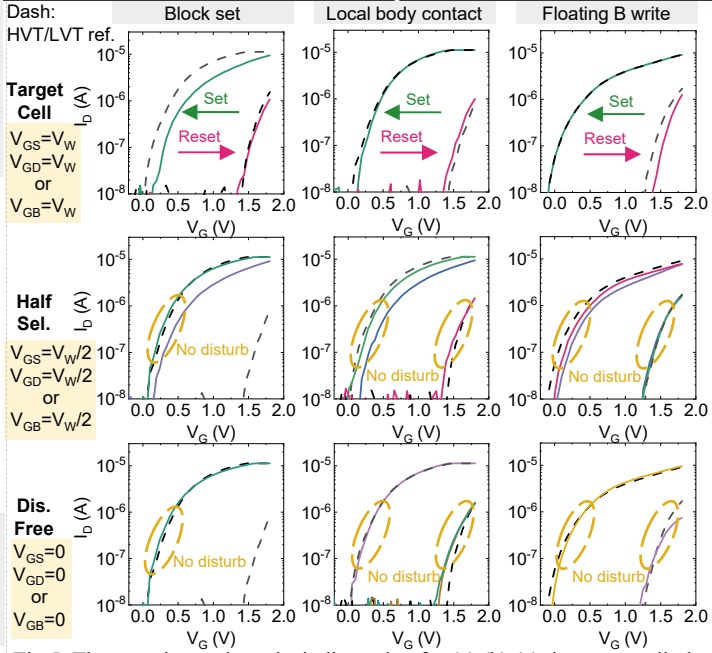

Fig.5. The experimental results indicate that for (a) (b) (c) the target cell, the proposed three write schemes can set/reset it successfully, without disturbing (c) (d) (e) half-selected cells and (f) (g) (h) disturb-free cells.

Proposed Write Scheme of Diagonal FeFET 1T NOR Array

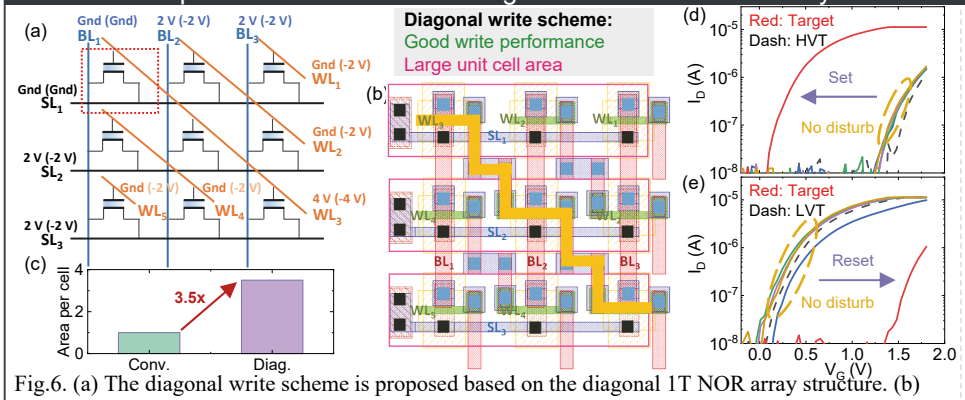

Fig.6. (a) The diagonal write scheme is proposed based on the diagonal 1T NOR array structure. (b) The layout of the diagonal array shows that (c) it has 3.5x area cost than the conventional array. The proposed diagonal scheme is verified by (d) set/ (e) reset experiments.

Motivation of Parasitic Study

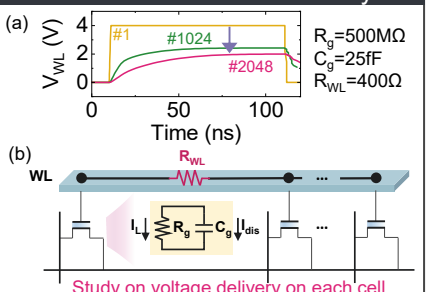

Fig.7. For large circuits, (a) parasitic RC along WL will cause large voltage drop, resulting in write failure, so the parasitic study is necessary for write schemes. The main parameters: (b) leakage current, displacement current and parasitic resistance on WL are studied here.

Study of Parasitic Parameters on Voltage Delivery in FeFET 1T NOR Array

Array Size Study

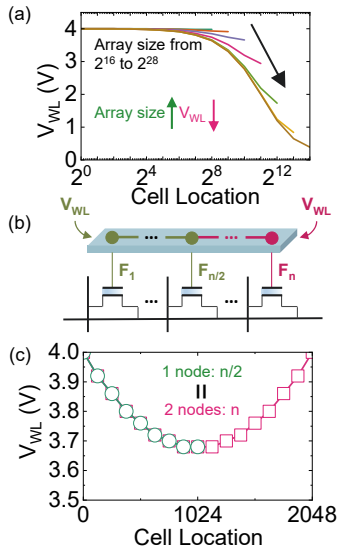

Fig.8. The results show (a) more V_{WL} drop for larger array due to larger parasitic RC. To mitigate the downward trend, (b)V_{write} is also applied on the other end of selected WL, so (c) V_{WL} drop will be the same as for the half array size case.

Default: Size=2048x2048 R_g=1GΩ C_g=0 R_{WL}=250Ω

Gate RC Study

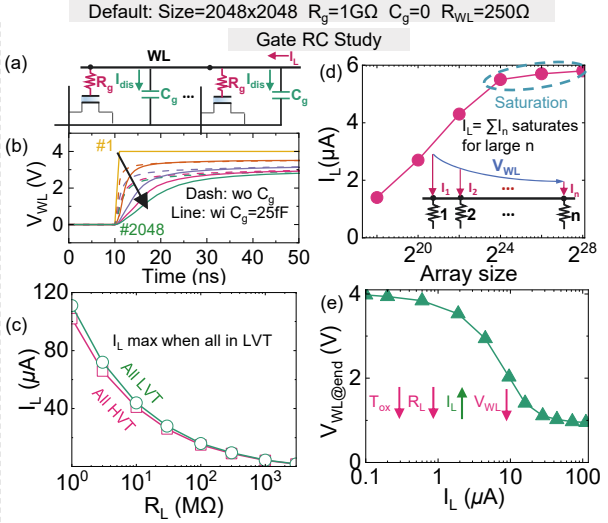

Fig.9. (a) R_g and C_g are used to study the leakage current (I_L) and displacement current (I_{dis}). (b) I_{dis} affects the write time of the last cell the most. Due to larger tunneling current in LVT state of FeFET, (c) I_L is the largest when all FeFETs are in LVT state (worst case). The large voltage decreasing near the end of WL will cause a negligible I_L per cell, leading to (d) the I_L saturation after array size>2^{24}. If I_L increases as the oxide thickness scales down, (e) a large V_{WL} drop will appear at the end of WL.

R_{WL} Study

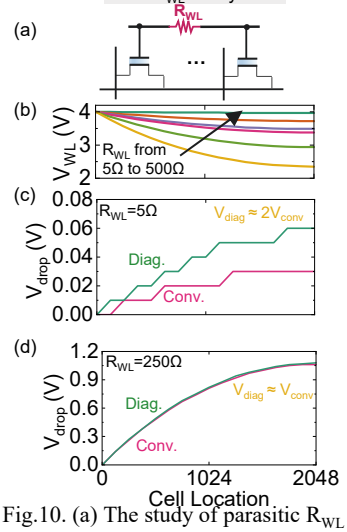

Fig.10. (a) The study of parasitic R_{WL} (b) shows a large impact over V_{WL} towards the end of WL. The difference of V_{WL} drop for conventional and diagonal array is very large (b) for small R_{WL} . In this study, $R_{interconnect}$ is negligible compared to R_{WL}, so (c) V_{WL} drop is similar for these two arrays.

Case Study of Applying FeFET 1T NOR Array on Ising Machine

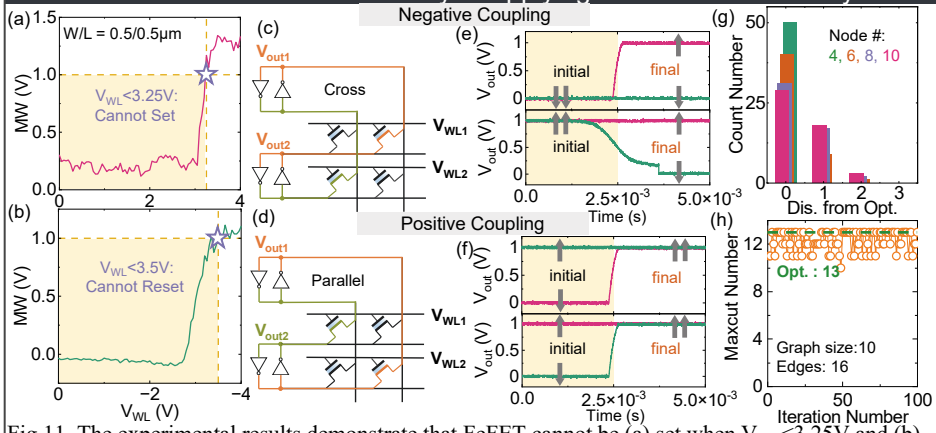

Fig.11. The experimental results demonstrate that FeFET cannot be (a) set when V_{WL}<3.25V and (b) reset when V_{WL}<3.5V for >1V MW. A FeFET 1T NOR array is dedicated as (c) negative and (d) positive coupling among latches in the Ising machine circuit. The two-latch system is settled (e) out-of-phase and (f) in-phase by FeFET respectively. The simulation results show that (g) the Ising machine can solve the MaxCut problem effectively and (h) the solution by the circuit is stable.

	Erase-program scheme	Local body contact scheme	Floating B write scheme	Diagonal write scheme
Set Mechanism	S/D	S/D	B	S/D
Reset Mechanism	S/D+B	B	B	B
Area density	✓	✓	✓	✗
Power	✓	✗	✓	✓
Write efficiency	✓	✓	✗	✓
Write time	✗	✓	✓	✓
Circuit complexity	✓	✓	✓	✗

Fig.12. A comparison among all proposed 4 write schemes of FeFET 1T NOR array. These schemes show different advantages and challenges. The best scheme is determined by the demand of applications.