

# Dynamic Predictive Sampling Analog to Digital Converter for Sparse Signal Sensing

Xiaochen Tang, *Member, IEEE*, Mario Renteria-Pinon, and Wei Tang, *Member, IEEE*

**Abstract**—This paper presents a dynamic predictive sampling (DPS) based analog-to-digital converter (ADC) that provides a non-uniform sampling of input analog continuous-time signals. The processing unit generates a dynamic prediction of the input signal using two prior-quantized samplings to compute digital values of an upper threshold and a lower threshold. The digital threshold values are converted to analog thresholds to form a tracking window. A dynamic comparator compares the input analog signal with the tracking window to determine if the prediction is successful. A counter records timestamps between the unsuccessful predictions, which are the selected sampling points for quantization. No quantization is performed for successfully predicted sampling points so that the data throughput and power can be saved. The proposed circuits were designed as a 10-bit ADC using 0.18 micro CMOS process sampling at 1 kHz. The results show that the proposed system can achieve a data compression factor of 6.17 and a power saving factor of 31% compared to a Nyquist rate SAR ADC for ECG monitoring.

**Index Terms**—Analog to Digital Converter, Dynamic Predictive Sampling, Low Power Circuits

## I. INTRODUCTION

LOW-power sensing hardware and algorithms for data acquisition systems are critical for wearable and miniaturized devices and have been actively studied. The primary goal is to convert the input analog signal into digital data while extracting the critical information from the input signal and avoiding unnecessary data generated from the conventional Nyquist sampling. As shown in Fig. 1 (A), the conventional Nyquist sampling uses a fixed sampling clock and converts each sampling point into digital values. Such a method generates too much data for the following digital signal processing circuits and systems, which introduces high power consumption for both signal processing and communication. In particular, since many signals in Internet-of-Things (IoT) and biomedical applications are sparse in the time domain, only the active portion or the spikes in the signal are of interest. Thus, Nyquist sampling consumes too much power in sampling and quantization while generating unnecessary data.

To address this issue, nonuniform sampling methods are proposed. The most popular solution is the event-based level-crossing sampling [1] that samples using amplitude thresholds instead of a constant clock [2]–[7] as shown in Fig. 1 (B). In

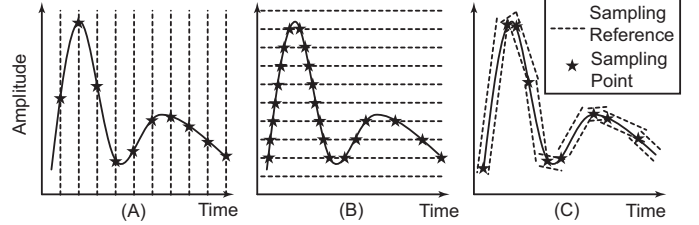


Fig. 1. Comparing different sampling methods: (A) Nyquist sampling, (B) Level-crossing sampling, and (C) Dynamic predictive sampling (DPS). The proposed DPS selects the least number of sampling points compared to other sampling methods.

this method, if the input analog signal's amplitude variation is below a certain threshold, no sampling and quantization are performed. This is an efficient way to save power and sampling data when the input signal is sparse in the time domain. However, it suffers from insertion/deletion errors of the pulse sequences [8] and is susceptible to high-amplitude low-frequency baseline wandering and low-amplitude high-frequency noise, which also lead many unnecessary samplings and generate nonessential data. Furthermore, it is not good at identifying turning points (fiducial points) of the input signal, such as the onset, peak, and endpoint of a peak, since it is only sensitive to the slope but not the slope variation. Slope-tracking sampling methods [9], [10] remove sampling points if the slope variation between segments of sampling points is under a certain threshold. However, it may discard important sampling points in the reconstructed signal [9].

In this paper, we report a novel sampling method based on dynamic prediction, which selects only the important sampling points for quantization. As shown in Fig. 1 (C), the proposed method applies two tracking threshold voltages that update their value based on the prediction of prior samplings. The system performs quantization only when the input signal is crossing the thresholds. This method can achieve data and power reduction as well as feature extraction during the sampling process. The sampling algorithm can be integrated into the analog-to-digital conversion process in a fully digital fashion without calculating the slopes.

## II. DYNAMIC PREDICTIVE SAMPLING

The dynamic predictive sampling method uses two prior sampling points to decide if the next sampling point is selected for quantization. The proposed system records the timing values and digital amplitude values of only the selected sampling points. This is performed in real-time during the sensing process to alleviate unnecessary quantization to save data and power. The following subsections describe the basic

Manuscript received XXX XX, 2022; revised XXX XX, 2022. This work was supported by the United States National Science Foundation under Grants. ECCS-1652944, and ECCS-2015573. The support granted by CONACYT through a graduate fellowship for Mario Renteria-Pinon is acknowledged.

Authors are with the Klipsch School of Electrical and Computer Engineering, New Mexico State University, Las Cruces, NM, USA. (Xiaochen Tang and Mario Renteria-Pinon contributed equally to this work)

Corresponding author: Wei Tang, e-mail: wtang@nmsu.edu

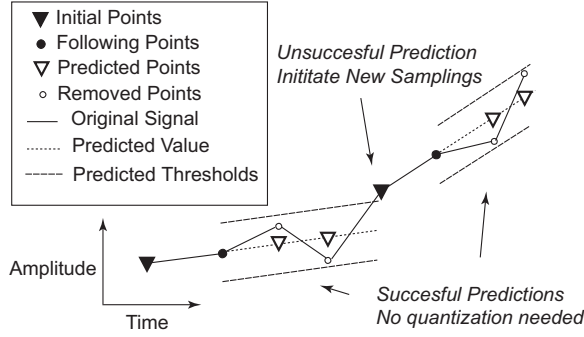


Fig. 2. DPS selects sampling points and calculates predictions. method of dynamic predictive samplings and hardware system implementation.

#### A. Prediction and Thresholds

As shown in Fig. 2, when the prediction process begins, the system performs analog-to-digital conversions for the first two sampling points. Then the digital prediction of the next sampling point is generated using linear extrapolation of the two prior sampling points. Specifically, the digital prediction value is calculated using twice the digital value of the last sampling point minus the digital value of the second last sampling point, as shown in (1):

$$P_D = 2 \times L1_D - L2_D \quad (1)$$

Here  $P_D$  is the predicted digital value;  $L1_D$  is the digital value of the last sampling point;  $L2_D$  is the digital value of the second last sampling point. Since in binary data format, multiplying by two can be achieved using a left shift of the bits, (1) does not involve an actual multiplication operation. The predicted digital value is then applied to generate the upper and lower threshold digital values by adding and subtracting a pre-defined digital Delta value using (2):

$$\begin{cases} UT_D = P_D + \Delta_D \\ LT_D = P_D - \Delta_D \end{cases} \quad (2)$$

Here  $UT_D$  is the digital value of the upper threshold,  $LT_D$  is the digital value of the lower threshold, and  $\Delta_D$  is the digital Delta value.

#### B. Sampling Decision

The upper and lower threshold values are then converted into analog values using a digital-to-analog converter (DAC). The analog values of the thresholds are compared with the actual analog input in the next sampling. Analog comparisons are made between the analog input signal, the upper threshold value, and the lower threshold value using a comparator operating in sequential or two comparators in parallel. The comparison results decide if the analog input signal is between the upper threshold value and the lower threshold value shown in (3).

$$LT_A < Input_A < UT_A \quad (3)$$

Here  $LT_A$  is the analog value of the lower threshold,  $Input_A$  is the analog value of the input signal, and  $UT_A$  is the analog value of the upper threshold.  $LT_A$  and  $UT_A$  are generated by the DAC based on digital values  $LT_D$  and  $UT_D$ , respectively.

The comparison result of (3) decides whether the prediction is successful. If the input analog value is between the two thresholds, i.e., (3) is valid, the prediction is correct and no quantization is performed for the input analog signal. In the

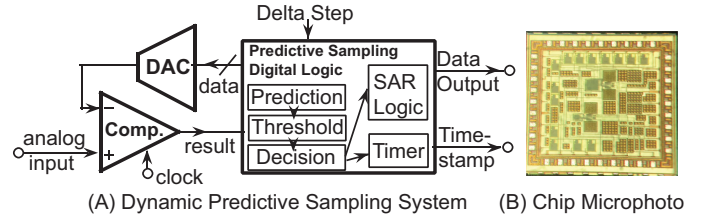


Fig. 3. (a) Block diagram of the Dynamic Predictive Sampling ADC. (b) Chip microphoto.

next prediction,  $L1_D$  is then replaced by the current  $P_D$  while  $L2_D$  is replaced by the current  $L1_D$ . Then the new  $P_D$  is calculated using (1). In such a case, the system doesn't record the data and no data are sent to the output. On the other hand, if the input analog value is not between the two thresholds, i.e., (3) is not valid, the prediction is incorrect. This means the input analog waveform is higher than the upper threshold or lower than the lower threshold. Then quantization is performed using Successive Approximation Register (SAR) logic for the next two sampling points to generate new digital values for prediction. In such a case, the two digital values are temporarily stored and applied as  $L1_D$  and  $L2_D$ . Then the next predicted digital value is calculated using (1).  $L1_D$  is sent as an output of the system. A clocked timer starts counting the timestamp between the timing of the current sample value and the next time when a prediction is incorrect. The timestamp is also a digital output of the system.

#### C. Hardware Implementation

A block diagram of the proposed dynamic predictive sampling system is shown in Fig. 3 (A), which consists of a comparator, a DAC, and a Predictive Sampling Digital Logic. The analog input signal is compared with the analog value generated from the DAC. The comparison result is sent to the digital logic for prediction and threshold calculation. The predictive sampling digital logic generates the digital data of the upper and lower threshold voltages using the predicted digital value and the Delta values. The digital data of the upper and lower thresholds are then sent to the DAC to compare with the analog input signal. The system can use one comparator to first compare the input with the upper threshold, and then compare the input with the lower threshold. It can also use two comparators to compare the input with both the upper and lower threshold simultaneously. The cost would be additional comparator circuit and power consumption. If the prediction is not successful, a full SAR logic is performed to obtain the digital value of the analog input. In such a case, the digital value of the analog input is sent as the Data output while a timer starts counting the clock cycles to obtain the Time-stamp output, which measures the timing difference between two unsuccessful predictions for signal reconstruction. The DAC in the system should meet the requirement of a DAC in a regular SAR ADC in terms of sampling rate and nonlinearity. To better evaluate the power savings of the proposed DPS method, an integrated ADC circuit is designed and fabricated using a  $0.18\mu\text{m}$  CMOS Process. The circuit is designed using a 1.8 V power supply and the sampling rate is set at 1 kHz targeting monitoring ECG signals. The internal clock is 16

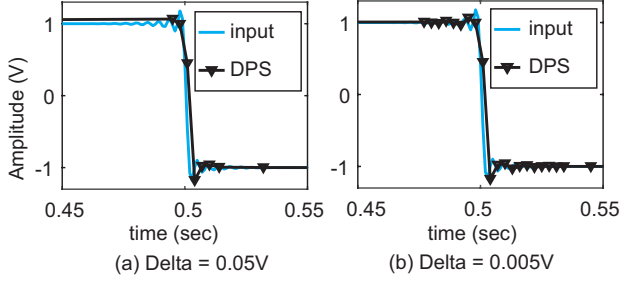


Fig. 4. Selected sampling points in low-pass-filtered square waveform with different Delta values.

kHz for the DPS and SAR logic. The overall chip is 1.5mm by 1.5mm including the pad frame. The microphoto of the integrated circuit is shown in Fig. 3 (b).

### III. PERFORMANCE EVALUATION

The primary goal of the dynamic predictive sampling method is to identify the key sampling points in the waveform to perform quantization. By doing so, the digital data throughput from the sensor can be reduced to alleviate processing or communication power for the following circuits in the system. In addition, the selected key sampling points also represent important features of the original waveform, which are more friendly for signal processing. Power saving is another important feature of the system especially when the input signal is sparse. In summary, the performance of the dynamic predictive sampling includes (1) data saving, (2) error introduced by reducing the number of sampling points, and (3) power saving from the analog to digital conversion steps.

Fig. 4 illustrates the simulation results of the selected sampling points using DPS with an input signal as a low-pass filtered square waveform. Such a waveform has linear portions in both the time domain and the amplitude domain, while it also contains small ripples and overshoots during the transition. As shown in Fig. 4, the DPS method selects a small number of sampling points when the input signal is linear in both amplitude and time domain, which saves a lot of data compared to Nyquist sampling and level-crossing sampling when the input signal is linear. More importantly, with a smaller Delta value, DPS automatically selects more sampling points in the fine structure of the waveform, which preserves the key information. Both Nyquist sampling and level-crossing sampling do not have such a feature. Comparing Fig. 4 (a) and (b), DPS can control the trade-off between errors and data savings by using different Delta levels, which provides more flexibility for a data acquisition system. The overall performance of DPS depends on specific input signals in terms of time domain sparsity, amplitude, and the selection of the Delta value. The following subsections analyze the performance trade-offs with specific signals.

#### A. Data Savings

The performance of data saving can be evaluated by the compression factor, which is defined as the ratio of the total data amount generated by Nyquist rate sampling to the data amount from the proposed DPS method [9]. The compression factor depends on the amplitude of the signal, the signal sparsity, and the Delta value. If the Delta value is too large, the

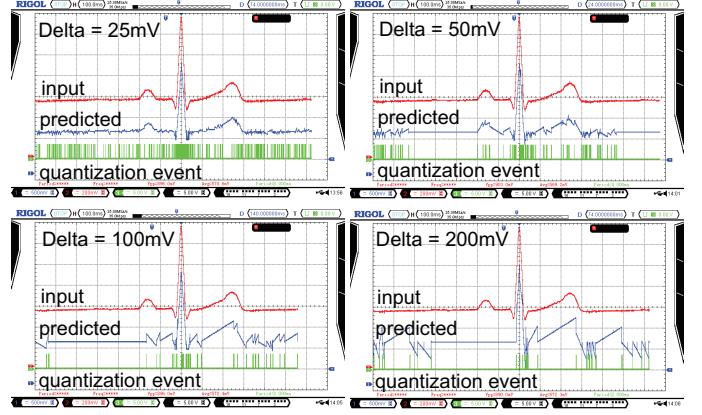


Fig. 5. Measured ECG waveform by the chip with different Delta values.

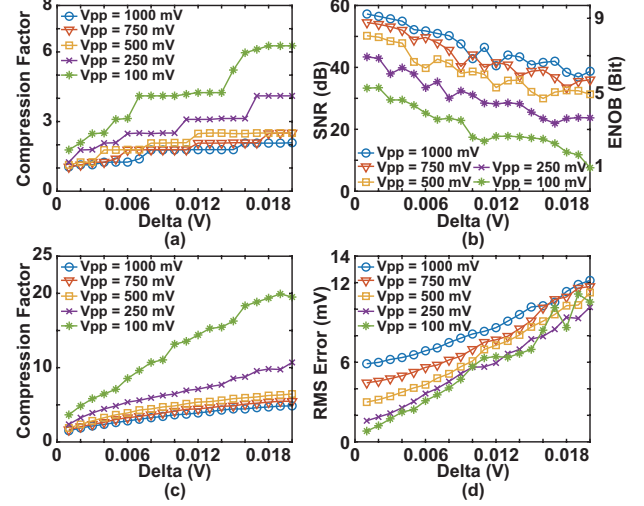


Fig. 6. Compression Factor and SNR at different Delta values for sinusoidal signal (a) (b) and Compression Factor and RMS error of ECG signal (c) and (d) with different amplitudes.

reconstructed signal may be distorted. In practical application, we can use an example signal to test the system to adjust parameters such as the Delta value of the proposed ADC until it meets desired performance. To evaluate data-saving performance on biomedical signals, ECG data from the MIT-BIH Arrhythmia database is applied as the input signal. In such an application, all fiducial points must be recorded for ECG arrhythmia classification. The measured time domain response of the ECG signal using the fabricated chip is shown in Fig. 5 using different Delta values, where the sampling rate is 1 kHz, which is enough for recording the ECG signal since most of the ECG spectrum is under 100 Hz. The DPS can achieve a compression factor of 6.17 while the reconstructed waveform is acceptable for arrhythmia classification. An example simulation using the MIT-BIH arrhythmia database (record 233) shows that the premature ventricular contraction beat (PVC) classification accuracy can achieve 97.16%, 94.01%, 90.71%, and 75.48% with Fig. 5's Delta of 25 mV, 50 mV, 100 mV, and 200 mV, respectively.

The reconstructed signal from the Dynamic Predictive Sampling method may introduce extra error since it contains fewer sampling points than Nyquist sampling. The timestamp data provides a timing difference between adjacent key sampling points. The amplitude value and the timestamp value of all the key sampling points can be plotted in the time domain



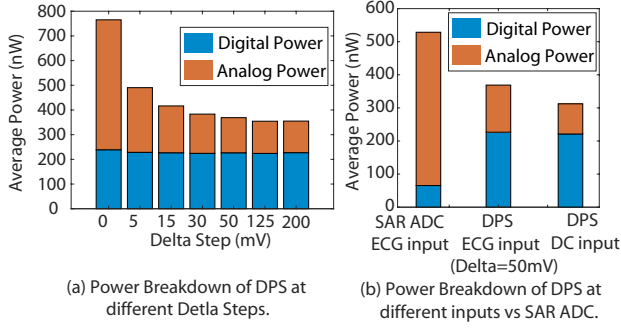


Fig. 7. (a) power breakdown of the DPS ADC at different Delta value. (b) Comparing power breakdown between the SAR ADC and DPS ADC with the same ECG input, and the DPS ADC with a DC input.

as a series of scattering points of the recorded data in the time domain. The most simple way of reconstruction is to connect adjacent points using segments, which is the piecewise linear method. Advanced methods could be applied to make the reconstruction signal more smooth. Reconstruction of the analog signal can be achieved using linear or polynomial interpolation. In this study, we assume the reconstruction is done by the first-order piece-wise-linear method by simply connecting the selected sampling points using straight lines. Both ECG signals and sinusoidal signals are studied as inputs to evaluate the performance of the proposed DPS method. Fig. 6 (a) and (b) show data saving and signal-to-noise ratio (SNR) as a function of Delta values at different signal amplitudes for the sinusoidal signal, while Fig. 6 (c) and (d) illustrate performance for the ECG signal in terms of data saving and RMS error. Since the DPS system requires extra timestamp output, we assume the data output of each sample is 10-bits and the timestamp between two samplings is also 10-bits. The ADC resolution (10-bit) is chosen for evaluating the system's performance. From simulation results, a 10-bit timestamp with a 1-kHz sampling rate is a very safe estimation for recording ECG signals. Thus, each sampling from DPS needs 20-bits while each sampling from Nyquist rate ADC needs only 10-bits. Thanks to the signal sparsity, the proposed DPS method can achieve a high compression factor while keeping the RMS error acceptable.

#### B. Power Savings

The DPS ADC achieves power saving when the input signal is sparse. The power cost of the DPS ADC depends on both the input signal sparsity and the Delta value. Fig. 7 (a) shows the simulated power breakdown of the DPS ADC at different Delta levels. The analog power comes from the comparator and the DAC. The digital power comes from the predictive sampling digital logic including the SAR logic, the timer, the calculator of prediction and threshold, and the digital decision-making circuits. While the digital power remains constant, the analog power can be saved with a larger Delta value. This is because with a larger Delta value, more predictions are successful. So that the analog power can be greatly saved due to the reduced frequency of performing quantization, which draws power from the comparator. Compared to a conventional SAR ADC, the DPS ADC pays extra effort in selecting sampling points by adding two more comparisons (comparing the input signal

TABLE I  
NONUNIFORM SAMPLING ADC PERFORMANCE COMPARISON

|                         | This Work          | TBCAS 2013 [4] | JSSC 2013 [5]  | TCASI 2020 [9] |
|-------------------------|--------------------|----------------|----------------|----------------|
| Method                  | Dynamic Prediction | Level Crossing | Level Crossing | Slope Sampling |
| Need Division           | No                 | No             | No             | Yes            |
| Turning Point Detection | Yes                | No             | No             | Yes            |
| Sampling Value          | Real               | Fixed Level    | Fixed Level    | Real           |
| Technology              | 180nm              | 180nm          | 130nm          | 180nm          |
| Sampling Rate           | 1 kHz              | Async          | Async          | 1 kHz          |
| Power                   | 368 nW             | 313 nW         | 6.5 uW         | 1700 nW        |
| Resolution              | 10-bit             | 6-bit          | 8-bit          | 12-bit         |
| Core Area (mm)          | 0.39 x 0.44        | 0.22 x 0.20    | 0.65 x 0.55    | 0.5 x 0.27     |
| Compression Factor      | 6.17               | N/A            | N/A            | 6.1            |

with the upper and lower thresholds) and extra calculation of the prediction in the control logic. Power saving is achieved when the prediction is successful so that no further quantization and comparison are required. Therefore, when the Delta value is very small, the DPS ADC may consume more power than a conventional SAR ADC due to the extra comparison and digital operation as shown in Fig. 7 (b). Although a DPS ADC has a larger digital power compared to a SAR ADC, it could be reduced by using advanced fabrication technologies. Since a conventional SAR ADC performs quantization at each sampling, its analog power from the comparator makes its total power higher than a DPS ADC when the input signal is sparse. A power-saving factor can be calculated by comparing the DPS ADC over a conventional SAR ADC at the same sampling rate and input signal.

#### IV. DISCUSSION

The proposed DPS ADC provides a unique method to separate the sampling and quantization processes to reduce the number of quantization in data acquisition systems. A comparison between the dynamic predictive sampling method, the level-crossing sampling method, and the slope-based signal-dependent sampling method is summarized in Table I. The level-crossing sampling ADCs [4], [5] can only record limited signal amplitude values while DPS reports accurate digital values for each selected sampling point. DPS is more efficient and accurate in terms of localizing turning points in the analog input waveform. More importantly, when considering the reconstruction of the input signal, the DPS method avoids the shifting error due to the insertion and deletion of pulses from the level-crossing sampling system. Furthermore, the level-crossing sampling system often requires the comparator to run in an "always-on" mode, while the DPS system can use a dynamic comparator and turn off the comparator to save power thanks to synchronous operation. Theoretical analysis of nonuniform sampling systems could be found in [11].

Both DPS and slope-based signal-dependent sampling [9] achieves data saving for sparse signal and both are able to record accurate value of turning points. The difference is

that in [9], the slope-based signal-dependent method discards sampling points if the slope variation between segments of sampling points is under a certain threshold. However, the slope calculation is processed in the analog domain including calculating divisions. Such a design may suffer from noise in the analog circuits. Moreover, if the slopes of consecutive segments between sampling points have variations small enough but accumulative to one direction, the system may unnecessarily discard important sampling points, which would introduce distortion in the reconstructed signal. Therefore, additional efforts have to be made to limit the maximum number of consecutive samples that can be dropped, which increases the computing complexity. The main difference between the dynamic predictive sampling method and [9] is that the DPS method performs prediction in the digital domain that avoids analog divisions and slope calculation. DPS method also avoids the problem of unnecessary drops of samplings in [9] since DPS doesn't compare slope values. Moreover, the DPS system achieves a low computing overhead since multiplying by 2 can be realized easily using shift registers. The DPS system can be implemented by simply modifying the digital logic in a conventional SAR ADC. However, DPS method may consume more digital power than [9] since most of the calculations in DPS method are done digitally.

Conventionally, the Figure-of-Merit (FOM) for SAR ADCs [12]–[14] does not consider other circuits in the system. The conventional FOM focuses on power consumption, sampling rate, area, and resolution of the ADC. However, the power cost and area from an ADC are usually a small portion of the whole system. Also, a high sampling rate and resolution may lead to a large amount of data that overloads the following processing, storage, and communication systems. In the proposed system, only critical turning points are recorded to reduce the output data amount. Moreover, the turning points identified during analog-to-digital conversion contain important features of the input signal, which further reduces the signal processing workload. Therefore, the advantages of the proposed system are not evaluated using the conventional FOM of ADC.

## V. CONCLUSION

This paper presents a dynamic predictive sampling method that selects key sampling points in the analog waveform for quantization. The proposed method utilize the sparsity of the input signal to achieve data saving and power saving. An integrated circuits was designed to simulate and analyze power consumption using 0.18  $\mu\text{m}$  CMOS process. The results show that the proposed system achieves a compression factor of 6.17 and a power saving factor of 30% for ECG signal. The performance was compared to the conventional SAR ADC, the level-crossing sampling ADC, and the slope-based signal-dependent sampling ADC. Compared to the level-crossing sampling ADC, the proposed system has the advantage of recording accurate digital value of key sampling points. It avoids complicated slope calculation circuitry in the slope-based signal-dependent sampling ADC. The proposed system can be implemented by modifying digital logic of a conventional SAR ADC while greatly reduces data throughput and power consumption in data acquisition and processing system.

## REFERENCES

- [1] Y. Zhao and Y. Lian, "Event-driven circuits and systems: A promising low power technique for intelligent sensors in aiot era," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 7, pp. 3122–3128, 2022.
- [2] B. Schell and Y. Tsividis, "A Continuous-Time ADC/DSP/DAC System With No Clock and With Activity-Dependent Power Dissipation," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 11, pp. 2472–2481, 2008.
- [3] W. Tang, A. Osman, D. Kim, B. Goldstein, C. Huang, B. Martini, V. A. Pieribone, and E. Culurciello, "Continuous time level crossing sampling adc for bio-potential recording systems," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 6, pp. 1407–1418, 2013.
- [4] Y. Li, D. Zhao, and W. A. Serdijn, "A Sub-Microwatt Asynchronous Level-Crossing ADC for Biomedical Applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 2, pp. 149–157, 2013.
- [5] C. Weltin-Wu and Y. Tsividis, "An Event-driven Clockless Level-Crossing ADC With Signal-Dependent Adaptive Resolution," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2180–2190, 2013.
- [6] Y. Hou, K. Yousef, M. Atef, G. Wang, and Y. Lian, "A 1-to-1-kHz, 4.2-to-544-nW, Multi-Level Comparator Based Level-Crossing ADC for IoT Applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 10, pp. 1390–1394, 2018.
- [7] S. Sirimasakul and A. Thanachayanont, "A logarithmic level-crossing adc," in *2017 14th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON)*, 2017, pp. 576–579.
- [8] Q. Hu, C. Yi, J. Kliewer, and W. Tang, "Asynchronous communication for wireless sensors using ultra wideband impulse radio," in *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2015, pp. 1–4.
- [9] E. H. Hafshejani, M. Elmi, N. TaheriNejad, A. Fotowat-Ahmady, and S. Mirabbasi, "A low-power signal-dependent sampling technique: Analysis, implementation, and applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 12, pp. 4334–4347, 2020.
- [10] E. Hadizadeh Hafshejani, N. TaheriNejad, R. Rabbani, Z. Azizi, S. Mohin, A. Fotowat-Ahmady, and S. Mirabbasi, "Self-Aware Data Processing for Power Saving in Resource-Constrained IoT Cyber-Physical Systems," *IEEE Sensors Journal*, vol. 22, no. 4, pp. 3648–3659, 2022.
- [11] H. Naaman, S. Mulleti, and Y. C. Eldar, "Fri-tem: Time encoding sampling of finite-rate-of-innovation signals," *IEEE Transactions on Signal Processing*, vol. 70, pp. 2267–2279, 2022.
- [12] D. Zhang and A. Alvandpour, "A 3-nw 9.1-enob sar adc at 0.7 v and 1 ks/s," in *2012 Proceedings of the ESSCIRC (ESSCIRC)*, 2012, pp. 369–372.
- [13] Y. K. Yang, X. Liu, J. Zhou, J. H. Cheong, M. Je, and W. L. Goh, "A 0.5v 16nw 8.08-enob sar adc for ultra-low power sensor applications," in *2013 IEEE MTT-S International Microwave Workshop Series on RF and Wireless Technologies for Biomedical and Healthcare Applications (IMWS-BIO)*, 2013, pp. 1–3.
- [14] K. Yadav, P. Patra, and A. Dutta, "A 43-nw 10-bit 1-ks/s sar adc in 180nm cmos for biomedical applications," in *2015 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia)*, 2015, pp. 21–25.