

Deposition-last lithographically defined epitaxial complex oxide devices on Si(100) F

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M. Chrysler,¹ J. C. Jiang,² G. Lorkowski,¹ E. I. Meletis,² and J. H. Ngai^{1,a)}

AFFILIATIONS

¹Department of Physics, University of Texas-Arlington, Arlington, Texas 76019

²Department of Materials Science and Engineering, University of Texas-Arlington, Arlington, Texas 76019

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a) Author to whom correspondence should be addressed: jngai@uta.edu

ABSTRACT

The epitaxial growth of SrTiO₃ on Si(100) substrates that have been lithographically patterned to realize deposition-last, lithographically defined oxide devices on Si is explored. In contrast to traditional deposition-last techniques which create a physical hard mask on top of the substrate prior to epitaxial growth, a pseudomask is instead created by texturing the Si substrate surface itself. The Si is textured through a combination of reactive ion etching and wet-etching using a tetramethylammonium hydroxide solution. Desorbing the native SiO_x at high temperatures prior to epitaxial growth in ultrahigh vacuum presents no complications as the patterned substrate is comprised entirely of Si. The inverted profile in which the epitaxial oxide device layer is above the textured pseudomask circumvents shadowing during deposition associated with conventional hard masks, thereby opening a pathway for highly scaled devices to be created.

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I. INTRODUCTION

Multifunctional oxides exhibit a range of material properties that promise to expand the functionality of electronic device applications.^{1,2} Perovskite structured oxides are of particular interest as they can be epitaxially integrated on Si, and the wide array of oxides with this crystal structure allows artificially layered heterostructures to be created. Device fabrication typically involves selectively removing material using wet- or dry-etch techniques starting from a grown film or multilayer heterostructure. Wet-etch techniques are simpler in set-up, though etching is generally isotropic and high selectivity between the mask material and the oxide layers to be etched is required. In contrast, dry-etch techniques can be anisotropic; however, dedicated equipment and the development of different recipes for different compositions of oxides may be necessary.^{3,4} For both wet- or dry-etch approaches, etching may adversely affect material quality along lateral sidewalls defining the boundary between the device and etched regions.

As an alternative to postgrowth patterning, deposition-last techniques first define the device region by depositing a hard mask on top of the substrate prior to epitaxial growth. The hard mask enables (inhibits) epitaxial growth in regions that are interior

(exterior) to the boundary of the device. Accordingly, candidate materials for hard masks must be able to withstand the high temperatures and oxidizing conditions at which the epitaxial growth of oxides typically occurs. For example, devices based on La_{1-x}Sr_xMnO₃, which exhibits colossal magnetoresistance, were created on SrTiO₃ substrates using amorphous TiO₂ as a hard-mask layer.⁵ Similarly, hard masks comprised of amorphous AlO_x and CeO₂ have been utilized to create devices that exploit the electron gas found at the interface between LaAlO₃ and SrTiO₃.^{6,7} For epitaxy on semiconductors, SiO₂ was used as a hard mask to create capacitor devices comprised of epitaxial BaTiO₃ grown on Ge(100).⁸ As oxides themselves, TiO₂, AlO_x, CeO₂, and SiO₂ naturally withstand typical growth conditions in oxidizing conditions.

Among substrates, though, Si stands apart as the dominant platform for device technologies. Developing deposition-last approaches to create lithographically defined epitaxial oxide devices on Si would open additional pathways for exploiting complex oxides in applications. However, adapting SiO₂, TiO₂, etc., as hard-mask materials poses challenges for a deposition-last approach to Si. Epitaxially integrating multifunctional oxides on Si first requires growing a layer of SrTiO₃ (STO) which subsequently acts as a

platform for the growth of other compositions of oxides. In general, the epitaxial growth of STO first requires the removal of the thin native layer of SiO_x on a substrate to achieve the formation of a dimerized $\text{Si}(100)$ surface either by directly desorbing the SiO_x or via the formation and desorption of an intermediary oxide, such as SrO .⁹ This is of particular importance for applications that require an atomically abrupt, structurally coherent interface between the epitaxial oxide and semiconductor, free of any SiO_x interfacial layer.¹⁰ However, removal of the native SiO_x layer requires temperatures near or in excess of $\sim 900^\circ\text{C}$ in ultrahigh vacuum (UHV), which would cause a hard mask comprised of SiO_2 , TiO_2 , or Al_2O_3 to breakdown, react with Si, and/or potentially induce migration of cations to regions of “clean” Si where the device is to be grown. We note that even if a material that withstands the high temperatures for desorbing SiO_x can be identified, shadowing from the sidewalls of the mask ultimately limits the lateral scale of device features, which is a problem that is universal to all hard masks that sit on top of the substrate used in deposition-last approaches.

To realize deposition-last epitaxial complex oxide devices, we explore growth on $\text{Si}(100)$ substrates that have been lithographically patterned using dry- and wet-etch techniques. Instead of depositing a physical hard mask on top of the Si substrate before epitaxial growth, we texture the surface of the Si substrate itself to create a pseudomask, in which epitaxial growth on the textured surface is limited or inhibited. The Si is textured through a combination of reactive ion etching (RIE) and wet-etching using a tetramethylammonium hydroxide (TMAH) solution. We show that despite significant processing of the wafer, a clean dimerized surface of $\text{Si}(100)$ can be subsequently achieved in UHV prior to epitaxial growth using oxide molecular beam epitaxy (MBE). Desorbing the native SiO_x at high temperatures prior to epitaxial deposition in UHV presents no complications, as the patterned substrate is comprised entirely of Si. Furthermore, the inverted profile in which the epitaxial oxide device layer is above the textured pseudomask circumvents

shadowing during deposition associated with conventional hard masks, thereby in principle enabling devices with highly scaled lateral dimensions to be created.

II. EXPERIMENT

A two-layer mask comprised of SiO_2 and photoresist is first created on the Si substrate, as schematically illustrated in Fig. 1(a). For this study, we use (100)-oriented, 4-in. diameter, nominally undoped, Czochralski (CZ) grown Si wafers (Virginia Semiconductor) that are diced (Disco DAD3220) into smaller squares that are 2-in. in length along the diagonal (i.e., 1.414×1.414 -in. in dimensions). Following dicing, the square Si substrates are then washed in an ultrasonic bath of acetone, followed by methanol, and finally isopropanol for 10 min each. A 120 nm layer of SiO_2 is then deposited on the Si substrate using plasma enhanced chemical vapor deposition (Trion Orion II PECVD system) at a temperature of 360°C and a deposition rate of 70 nm/min. Conventional photolithography is used to create a mask (Shipley 1813) covering the device regions (e.g., such as a Hall bar). The wafer is then dipped into dilute 10:1 HF: H_2O solution (JT Baker) for ~ 30 s, etching away the surrounding SiO_2 that is not covered by the photoresist.

We then subject the substrates to RIE (Technics Macro series 8800) in a 150 mTorr mixture of 96% CF_4 with 4% O_2 under a capacitively coupled, radio-frequency induced plasma (400 W, 30 kHz), which etches away the exposed Si at a rate of ~ 120 nm/min. The wafer is then subjected to a second etching process in a solution of 5% TMAH/10% isopropyl alcohol/85% H_2O which is heated to a temperature of 80°C . The isopropyl alcohol is intended to act as a surfactant.¹¹ The TMAH solution readily etches the photoresist and the exposed Si but etches the SiO_2 much more slowly.¹² The substrates are then dipped in de-ionized water and then dried with high-pressure flowing N_2 . Finally, the substrates are again etched in 10:1 HF: H_2O solution to remove the residual SiO_2 mask prior to

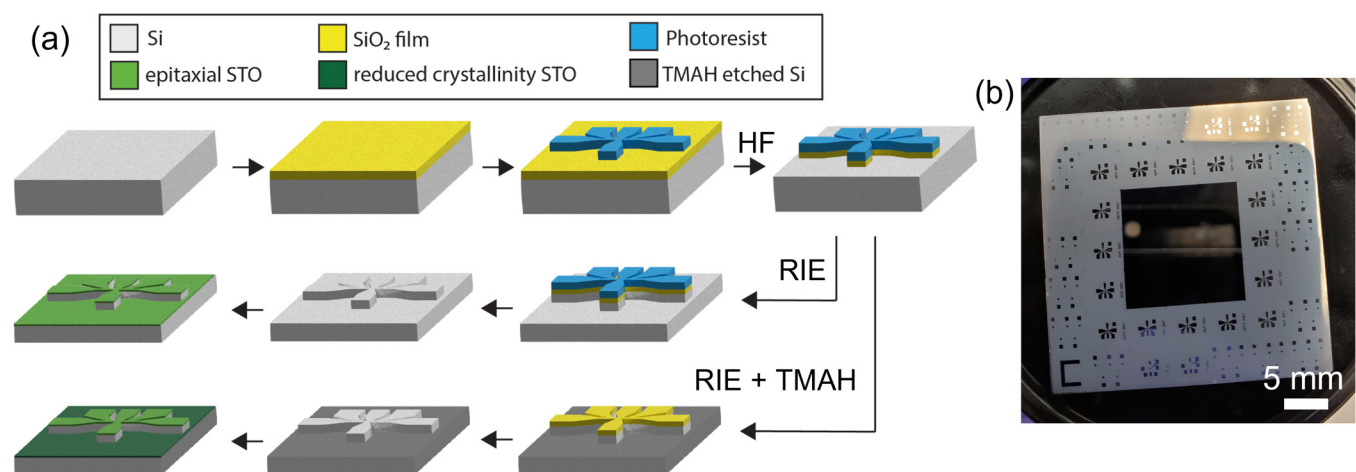


FIG. 1. (a) Schematic of the deposition-last substrate preparation process. (b) Optical image of a RIE and TMAH etched substrate.

loading into the oxide MBE chamber. The substrate is initially subjected to an oxygen plasma that is generated by an RF source (Veeco) operating at ~ 250 W for 10 min at room temperature in the growth chamber to remove any residual organics.

Here, we report results for 12 nm thick STO films as well as 15 nm thick $\text{Sr}_{1-x}\text{La}_x\text{TiO}_3$ (La-STO) films ($x=0.10$) grown on the patterned Si substrates. Details on the process of epitaxial growth using MBE can be found elsewhere.¹³

While our approach to patterning the Si wafer to create a pseudomask can be applied to any device design, here our pseudomask is designed to be compatible with reflection high-energy electron diffraction (RHEED). Figure 1(b) shows a picture of a patterned Si substrate subjected to RIE + TMAH processes. A large area in the center facilitates *in situ* RHEED measurements during growth, while Hall bar and capacitor devices are situated on $5 \times 5 \text{ mm}^2$ “lots” surrounding the center window. After growth, the substrate is diced into the $5 \times 5 \text{ mm}^2$ lots to facilitate the characterization of the individual devices.

X-ray diffraction (XRD) in θ - 2θ geometry is performed using a diffractometer with a standard $\text{Cu K}\alpha$ source (Bruker D8 Advance). Note that the etched pseudomask covers the entirety of some of the $5 \times 5 \text{ mm}^2$ lots, thereby facilitating XRD measurements. Similarly, $5 \times 5 \text{ mm}^2$ pieces from the center area enable XRD to be performed on films grown on nonetched, epi-polished portions of the substrate.

To elucidate the surface morphology induced by RIE etching alone, atomic force microscopy (AFM) is performed in standard contact-mode (Park XE 70). For substrates subjected to both RIE and TMAH etching, the surface is too rough for AFM. Instead,

scanning electron microscopy (SEM) is performed (Hitachi S-4800 FE-SEM).

Cryomagnetic electrical transport measurements on a Hall bar are performed in a commercial physical property measurement system (PPMS, Quantum Design) using a DC technique (Keithley 2400 Sourcemeter). Electrical contacts to the Hall bar are established by wedge-bonding Al wires directly to the oxide layer (Westbond 7476E-79).

III. RESULTS AND DISCUSSION

We first examine the effect of RIE alone on the morphology of the Si(100) surface. Figure 2 shows AFM images comparing the surface morphologies of the unetched epi-polished substrate [Fig. 2(a)] to substrates that have been etched for 5, 10, and 15 min [Figs. 2(b)–2(d)]. Line scans taken across the epi-polished substrate, and the substrate that has been etched for 15 min are compared in Fig. 2(e). We find that the Ra roughness saturates after ~ 10 min of etching, as summarized in Fig. 2(f). Despite the significantly rougher morphology, however, we show that epitaxial growth can still be achieved on the substrates that have been etched for 15 min. As our RIE conditions etch the Si at a rate of ~ 120 nm/min, etched regions are situated below the epi-polished surface that will eventually become the device layer.

Subsequent etching in the TMAH solution further enhances the texture of the Si, which results in the creation of a pseudomask. Figure 3(a) shows an SEM image of a Hall bar comprised of 15 nm La-STO grown on a substrate that is subjected to RIE for 15 min, followed by etching in TMAH solution for 6.5 min. The difference

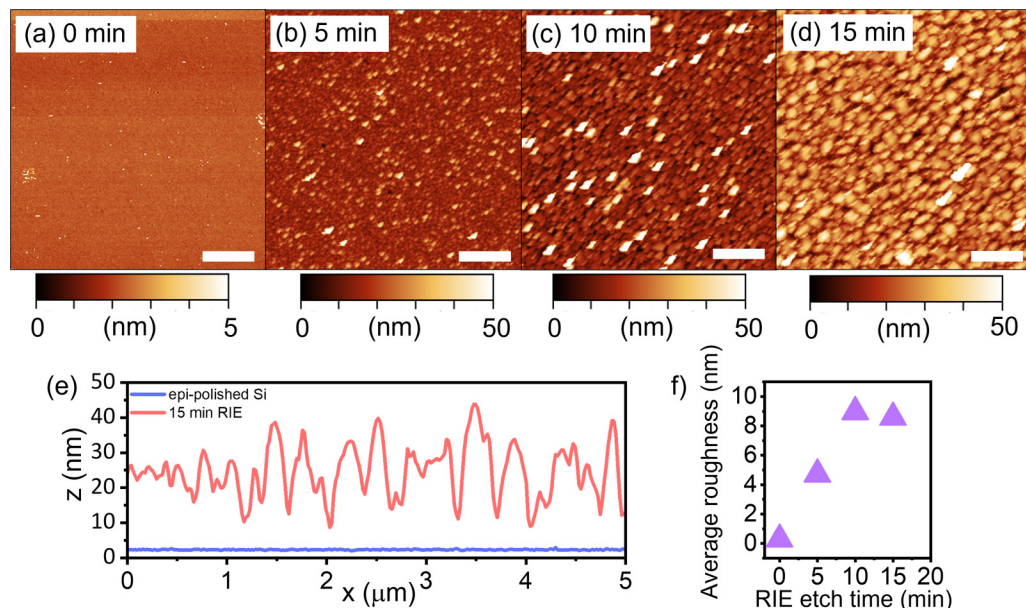


FIG. 2. AFM images of (a) pristine epi-polished Si, (b) Si after 5 min RIE, (c) Si after 10 min RIE, and (d) Si after 15 min RIE. Scale bar is $1 \mu\text{m}$. (e) AFM line profiles of epi-polished Si and 15 min RIE Si. (f) Ra surface roughness with duration of RIE.

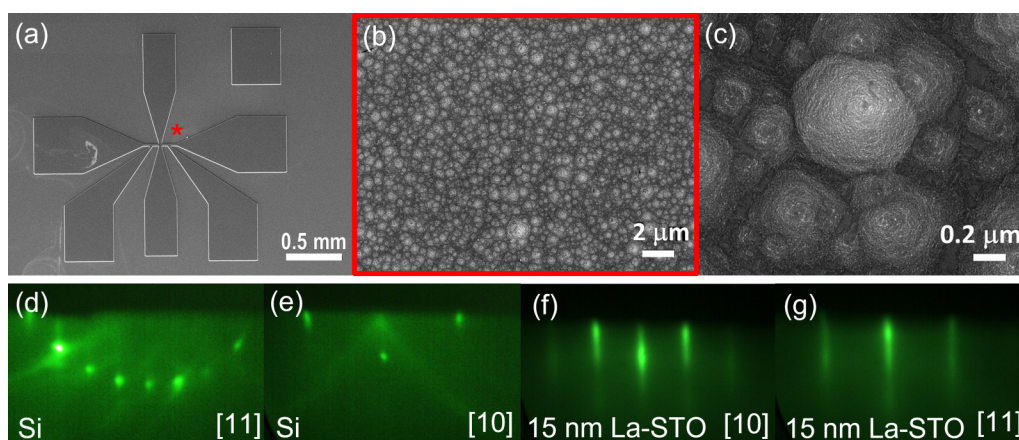


FIG. 3. (a) SEM of a finished Hall bar device with 15 nm La-STO grown thereon. (b) and (c) show high magnification SEM images of the RIE + TMAH etched region labeled with an asterisk in (a). (d) and (e) RHEED patterns taken on a Si substrate subjected to RIE + TMAH processes at high temperatures. (f) and (g) RHEED patterns on a 15 nm La-STO film grown on the substrate subjected to RIE + TMAH processes.

in height between the top La-STO device layer and the pseudomask below is $\sim 3.3 \mu\text{m}$, as determined by profilometry (KLA-Tencor P-6), in which we estimate the TMAH etches at a rate of $\sim 250 \text{ nm/min}$. The difference in height between the device and pseudomask layers can be adjusted by changing the duration of RIE and TMAH etching. Figure 3(b) shows an SEM image of the RIE + TMAH etched region adjacent to the Hall bar [asterisk in Fig. 3(a)], while a further magnified image of the surface morphology is shown in Fig. 3(c).

Critical to epitaxially integrating SrTiO_3 on Si with atomically abrupt interfaces is first obtaining a reconstructed, dimerized (100)-surface on the Si substrate in UHV at high temperatures. Despite significant processing of these substrates through RIE and in TMAH solution, a clean surface is obtained in UHV, as shown in the RHEED pattern of Fig. 3(d), taken at 870°C along the [11] direction of the Si(100) surface. Note the prominent $2\times$ reconstructions in the RHEED, consistent with a dimerized surface. Figure 3(e) shows RHEED taken along the [10] direction of the Si surface, in which no secondary features associated with SiC are present. Figures 3(f) and 3(g) show final RHEED patterns taken on a 15 nm thick La-STO film along with the [10] and [11] directions, respectively, indicating single-crystalline quality growth.

XRD reveals the crystallinity of STO grown on various portions of the patterned substrates. Figure 4 shows θ - 2θ data taken on a 12 nm thick STO film grown on a substrate that is subjected to RIE for 15 min, in which curve (i) is data from a portion of the substrate that remains epi-polished, while curve (ii) is data from a portion of the substrate that is etched (the data has been arbitrarily offset for clarity). Note the latter still shows a robust peak associated with the (002) planes of STO despite aggressive RIE treatment. The aggressive RIE treatment does, however, reduce the crystallinity of the STO grown thereon, as indicated by rocking curve analysis taken about the STO (002) peak [Fig. 4, inset, curves (i) and (ii)], in which the full-width-at-half-maximum (FWHM) is $\sim 1.03^\circ$ for the STO grown on the portion of the substrate exposed to RIE, as

compared to 0.66° for the STO grown on a portion of the substrate that remains epi-polished.

In comparison, epitaxy is significantly suppressed on portions of substrates exposed to both RIE and TMAH processes. Figure 4 shows θ - 2θ data of a 15 nm thick La-STO film grown on a substrate that is subjected to RIE and TMAH solution for 15 and 6.5 min, respectively, in which curve (iii) is data from a portion of the substrate that remains epi-polished, while curve (ii) is data from a portion of the substrate that is etched. The STO (002) peak is barely discernible from the background in the latter, indicating degraded epitaxial growth, which is ideal behavior for a pseudomask.

The La-STO grown on Si provides an ideal model system to test electrical transport in the Hall bar devices. As shown in prior studies, the lateral electrical transport in doped SrTiO_3 grown on CZ-Si involves both electron transport in the former and hole transport in the latter.^{13,14} One explanation for this combined transport behavior is the formation of a heterojunction between STO and CZ-Si, in which electrons from the latter transfer to the former to create space-charge and a built-in electric field.^{13,14} The electrons in the Si stem from the presence of O-impurity donors, which originate from diffusion into the Si during epitaxial oxide growth as well as the CZ-grown Si itself.¹⁴ The depletion of Si due to the transfer of electrons to STO leads to type-III band alignment and inversion at high temperatures [Fig. 5(a), inset band diagram], as manifested by a hole gas that forms at higher temperatures and conducts in parallel with the electrons in the La-STO film. The hole gas manifests as a sudden drop in sheet resistance with increasing temperature [Fig. 5(a), arrow], accompanied by a crossover in sign in the Hall voltage from negative to positive, in which the holes dominate the Hall signal due to their higher mobilities [Fig. 5(b)].¹³ We attribute the upturn in sheet resistance and the low mobility at low temperatures ($\sim 12 \text{ cm}^2/\text{Vs}$ at 30 K) to the weak localization of carriers in the La-STO, which are confined near the interface due to a built-in electric field.¹³ The electrical transport in

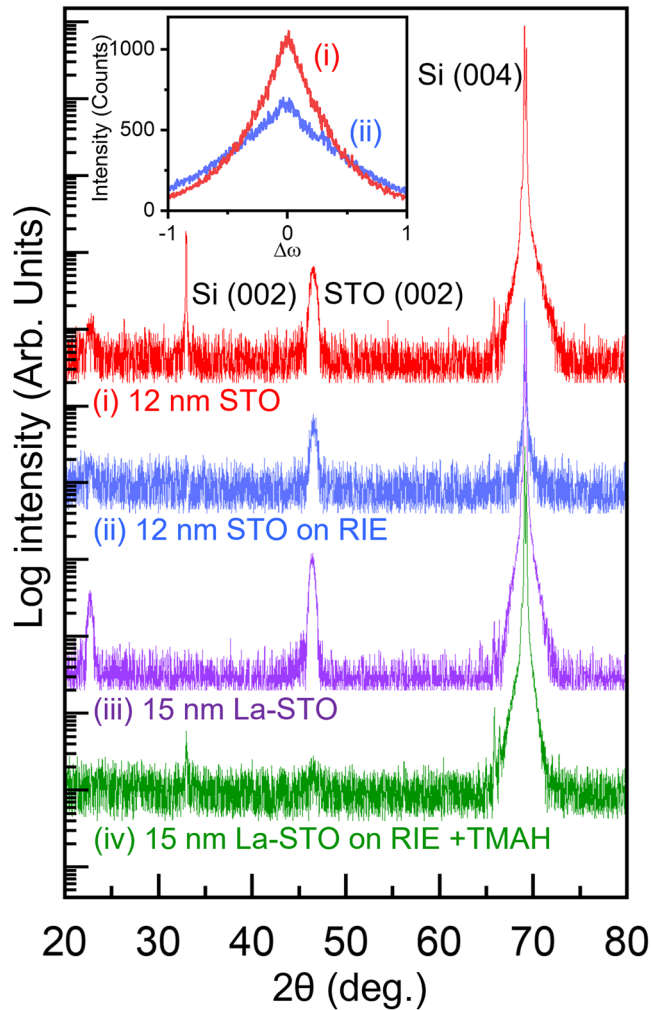


FIG. 4. XRD survey scans for 12 nm STO and 15 nm La-STO grown on patterned Si substrates subjected to just RIE and RIE + TMAH processes, respectively. (i) STO on an epi-polished portion of a substrate subjected to RIE. Associated rocking curve is found in the inset. (ii) STO on a portion of substrate exposed to RIE. Associated rocking curve is found in the inset. (iii) La-STO on an epi-polished portion of a substrate subjected to RIE + TMAH. (iv) La-STO on a portion of substrate exposed to RIE + TMAH.

our La-STO/Si Hall bar devices is consistent with having an interface free of SiO_x , as the latter would block electron transfer from Si to La-STO. The demonstration of electron transfer and the formation of a heterojunction demonstrate that high-quality, deposition-last, lithographically defined devices can be realized on Si substrates that have been subjected to dry- and wet-etch processing.

We found that the etching of Si in TMAH solution alone without prior dry etching in $\text{CF}_4 + \text{O}_2$ results in sparse mosaic structures that coexist with smoother regions for the same temperature and duration of etching as discussed above. We surmise the

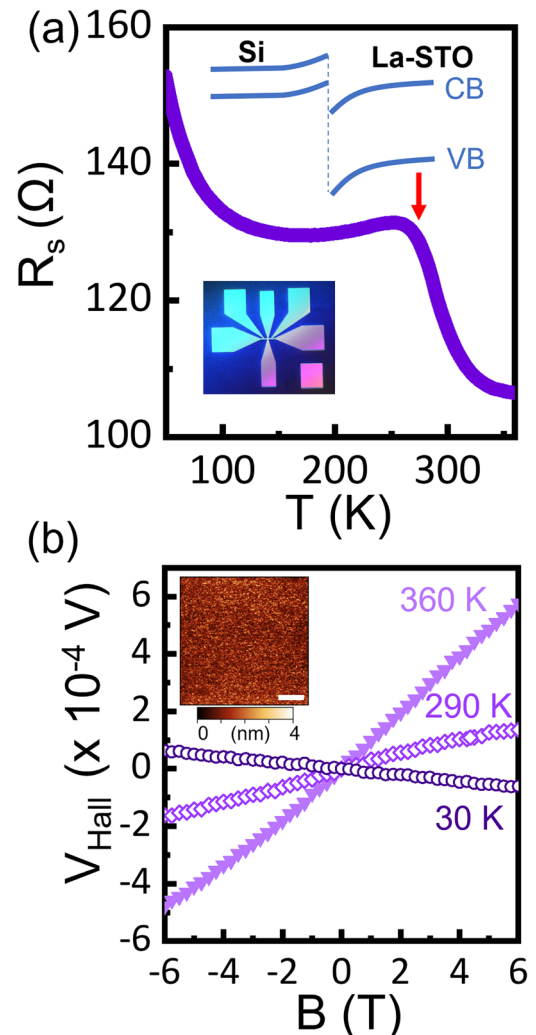


FIG. 5. (a) Sheet resistance of a Hall bar device comprised of 15 nm La-STO on Si. The insets are a band diagram of the heterojunction and an optical image of a Hall bar device. (b) Hall voltage for the 15 nm La-STO on Si heterojunction Hall bar device showing a crossover in sign of the Hall voltage indicating the formation of a hole gas at higher temperatures that conducts in parallel with electrons in the La-STO layer. AFM imaging of the La-STO device (inset; scale bar is 1 μm .) indicates a largely featureless surface, consistent with a smooth film that is comparable in roughness to the epi-polished substrate.

facets created by the initial RIE facilitate the subsequent texturing by TMAH.

The electrical isolation between adjacent devices on a patterned Si substrate is limited by the electrical conductivity of the degraded epitaxial oxide layer deposited between the devices, as well as the bulk conductivity of the Si substrate. For the former, highly degraded or amorphous forms of nominally metallic oxides, such as $\text{La}_{1-x}\text{Sr}_x\text{MnO}_3$, are generally very insulating.⁵ Bulk conductivity of the Si substrate can vary widely, though, even for undoped

Si, depending on the method used to grow the ingot (i.e., float-zone or Czochralski methods). Here, we used heterojunctions between La-STO and CZ-Si as a model system, in which electrical coupling between the oxide and the substrate was of interest. We note that for situations in which electrical coupling between the epitaxial oxide device and the Si substrate is not necessary, or if enhanced electrical isolation between adjacent oxide devices on a patterned substrate is desired, a layer of SiO_x can be intentionally created at the interface through growth at higher oxygen pressures, after initial nucleation of an epitaxial layer on a reconstructed Si(100) surface.

While the inverted profile in which the device layer is situated above the pseudomask facilitates the lateral scaling of devices by eliminating shadowing, lateral scaling in our present process is limited by the TMAH step, which can undercut a mask layer. We note, however, that TMAH etches Si in an anisotropic manner, in which the ratio between etching {111} and {100} planes has been reported to be as low as <0.04 .¹⁵ Thus, undercutting could be minimized by aligning features along, for example, the $\langle 110 \rangle$ direction, if devices are grown on a (100)-oriented substrate.

The ability to achieve epitaxy even on substrates subjected to relatively aggressive RIE (e.g., 15 min duration) suggests that non-planar or tiered device structures of epitaxially grown complex oxides could be realized on Si. Here, the two-step RIE + TMAH texturing process was used to create a pseudomask. Instead, tiered epitaxial oxide structures could be realized on substrates that have been less aggressively etched by RIE with no subsequent etching in TMAH solution.

In place of TMAH, potassium hydroxide (KOH) was also explored as a wet-etchant to texture the Si surface in conjunction with RIE. However, despite being able to desorb the native SiO_x and achieve a dimerized Si(100) surface, subsequent crystallization of 2.5 u.c. of STO was not achieved on a KOH patterned substrate. We attribute the inability to crystallize STO to residual K atoms that remain on the patterned substrate. Hence, it appears that only metal-free organic etchants, such as TMAH, are compatible with subsequent crystallization and epitaxial growth of STO.

IV. SUMMARY AND CONCLUSIONS

In summary, we have explored the epitaxial growth of STO on dry- and wet-etched Si substrates to realize deposition-last, lithographically defined oxide devices on Si(100). Our approach of defining a pseudomask using RIE and etching in TMAH solution circumvents shortcomings associated with traditional hard masks used in deposition-last approaches. As the substrate is comprised entirely of Si, desorbing residual native SiO_x at high temperatures in UHV poses no challenges, and the inverted profile between the pseudomask and device layer circumvents shadowing during epitaxial film growth. Finally, epitaxial growth on substrates that are partially etched by RIE without subsequent etching by TMAH could be exploited to realize tiered oxide structures on Si. Lithographic patterning of the substrate prior to deposition can be exploited in place of or in conjunction with post growth oxide

etching to open new pathways to realize epitaxial oxide devices on Si.

ACKNOWLEDGMENTS

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

M. Chrysler: Data curation (lead); Formal analysis (lead); Investigation (lead); Writing – original draft (equal); Writing – review and editing (equal). **J. C. Jiang:** Data curation (equal); Formal analysis (equal); Investigation (equal). **G. Lorkowski:** Investigation (supporting). **E. I. Meletis:** Funding acquisition (equal). **J. H. Ngai:** Conceptualization (lead); Formal analysis (equal); Funding acquisition (lead); Methodology (lead); Project administration (lead); Resources (equal); Supervision (lead); Writing – original draft (lead); Writing – review and editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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