Advanced Methods of Detecting Physical Damages in Packaging and BEOL Interconnects

Jorge Mendoza, Jimmy-Bao Le, Choong-Un Kim
Materials Science and Engineering
University of Texas at Arlington
Arlington, TX
Phone: (817)- 875-7251, choongun@uta.edu

Hung-Yun Lin
Texas Instruments, Inc., Dallas, Texas 75243
h-lin2@ti.com

This paper reports new methods of detecting damages and failures in packaging interconnects in fully packaged devices with sufficient sensitivity and selectivity for damages in interconnects. Exploration on various electrical methods leads to the conclusion that a few electrical measurement techniques, especially one using a low frequency AC signal, may provide effective mechanism of detecting the damages under interest. Impedance and derived parameters such as capacitance and inductance show sensitivity to silicon-package-interaction damages, with satisfactory immunity to parasitic signals present in fully assembled/packaged test chips such as the probe/pad contact resistance and stray capacitance from various sources. Two highlighting examples based on the "open circuit test pattern" are introduced in this paper to demonstrate the effectiveness of developed methods. The first is the damage detection in the high resistance open circuit pattern, which consists of small metal serpentines strategically placed on the failure prone places in BEOL of Si chip. Small damage develop in the metal serpentine makes the circuits to produce LC resonance-like signals useful in detecting presence of damage and its location. The second is the impedance method sensitive to the damage/failure in low resistance open circuit pattern like solder interconnects. The method measures the impedance as a function of frequency and design to detects the crack and/or void trapped/developed at the solder joints mainly using the skin effect in AC resistance. The technique is with its own limitations but can enable effective characterization of damages in package interconnects.

Index Terms **- silicon-package-interaction, chip-package-interaction, interconnect failures, low-frequency impedance spectroscopy, nondestructive damage detection.**

INTRODUCTION

The continuing demand for smaller, yet higher performance devices has resulted in many revolutionary changes in device and packaging assemblies in recent years, including the change in BEOL interconnect structures, package form factors, and the type of materials used for the packaging assembly. Such changes have brought various benefits, but they are not without their drawbacks. With reduced redundancy in structural design and material stability, the devices are becoming far more susceptible to failures instigated by various sources. Of particular concern in recent years is the emergency of the damages in interconnects caused by Silicon-Package-Interaction (SPI) or Chip-Package-Interaction (CPI) because of its role in inducing new damages in various places in the chip and the package [1]. In such structure, the typical assumption that the failure mechanisms of components in the silicon chip (mechanical, thermal, and electrical) are no longer valid because they are not mutually exclusive. This makes reliability assessment of each failure mechanisms challenging as the source of the failure can be rooted to anywhere within the package assembly or the back-end-of-line interconnects (BEOL). Since such failure is not easy to characterize, failure analysis demands extensive time and resources, delaying development of new packaging technologies. There is a growing desire to develop suitable metrologies that have both sufficient sensitivity and selectivity for characterizing failures both in the package assemblies and interconnects and thus enable more effective failure analysis of SPI failures and design of new packing structure with needed reliability [2].

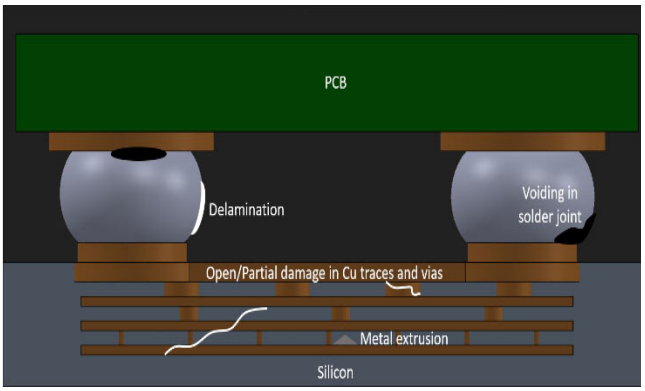

Figure 1. A schematic representation of damage in Cu traces/vias, dielectric layer damages, and cracks in solder joint

In the SPI, several damages can occur in any combination. Several examples of these are: metal extrusion, complete or partial openings in the BEOL metal interconnects (traces and/or vias), cracks or voids in the solder joint interfaces, or delamination of the molding compound, shown in Fig. 1 [3]. The ideal method of detecting such damages would not require extensive characterization efforts and be overly invasive to reduce time and resources. The common practice is to use

simple test circuit and employ DC based electrical characterizations such as the measurement on DC resistance and leakage current paralleled with invasive failure analysis. The main issue with this form of measurement is that it does not have sufficient selectivity and damage sensitivity, thus, requiring a reference to be of use and sometimes leading to a false conclusion.

The method being developed in our research involves the technique fundamentally based on the low frequency impedance spectroscopy (LFIS). LFIS displays evidence of being able to detect the listed damages that are otherwise difficult to locate by alternative methods. This method has yielded compelling evidence that it is able to accurately detect and characterize damage in the dielectric layer, BEOL interconnects, and the solder joints. This paper presents two example cases of LFIS taken from the open circuit test pattern, displaying its sufficient sensitivity and selectivity to accurately assess failure and damage signals within an SPI.

Samples and Measurements

Two "open circuit" test patterns are designed and used to develop techniques of damage detection in BEOL and package interconnects. One of the open circuit test patterns used in our study is a low resistance pattern to isolate physical damages in the solder joints. Connecting two solder joints by a short metal interconnect patterned on a Si chip, this pattern is designed to test failures within the solder joints by isolation. Without the resistance of the BEOL interconnects, the resistance and any failure signal are assumed to be damages within the solder joints. In fact, the solder joint in this pattern is the most damage prone by SPI thermo-mechanical load. The other open circuit test pattern is a high resistance pattern that includes the interconnects in BEOL. The multilevel Cu or Al lines in serpentine structure is produced in BEOL and connected to Cu leadframe via solder joint. Multiple serpentine patterns are serially connected in one circuit, and each serpentine is located at the place of SPI damage potential, including the area underneath UBM. The high resistance from serpentine overwhelms the resistance of the test circuit, so the failure can be detected only by a near perfect open in the circuit. Partial damage is not easy to detect, motiving the use of LFIS technique.

Impedance measurements of each test circuit are conducted using a HP4284A Precision LCR meter. The probes are placed on the lead frame pins that correspond to each of the failure test circuit patterns. Test AC voltage and measurement settings are determined from initial trial and errors. Measurements are typically conducted at room temperature with AC frequencies ranging from 20 to 1 MHz. The samples are subjected to thermal cycling to induce SPI damage within the circuit. Then, in-situ measurements are conducted to correlate damage signals to the amount of thermal cycles and amount of physical damages. The thermal cycling process consists of cooling and heating of samples from -55°C to 150°C. Throughout the LFIS measurements and thermal cycling samples are selected and subjected to cross-sectional SEM imaging to further provide evidence of internal damages to measured signals.

Results and Discussion

A. Characterization of BEOL damage by SPI

The purpose of this investigation is to understand the impact of the structure and assembly processes of solder joint on the stability of BEOL interconnects under thermal stress loads. To this end, a test chip with two-level interconnects is designed to produce a serially connected multiple serpentine patterns placed under a Cu-UBM pad/solder bump and finally leadframe via solder joints. The serpentines are in M1 layer while they are connected to M2 layer pads. The starting idea behind the design is that the serpentines are placed at places subjected to failure inducing SPI induced thermal stresses. With multiple segmented serpentines, a large area of SPI damage potential can be studied without losing structural proximity to the condition of BEOL interconnects in real device. The test chip with these patterns embedded at various location enables study of SPI induced interconnect failures from the measurement on the electrical continuity. The limitation is that damage detection is not possible until the resistance change by damage is at a sizable level. Also problematic is the fact that the failure location is nearly impossible to determine in web of serpentines.

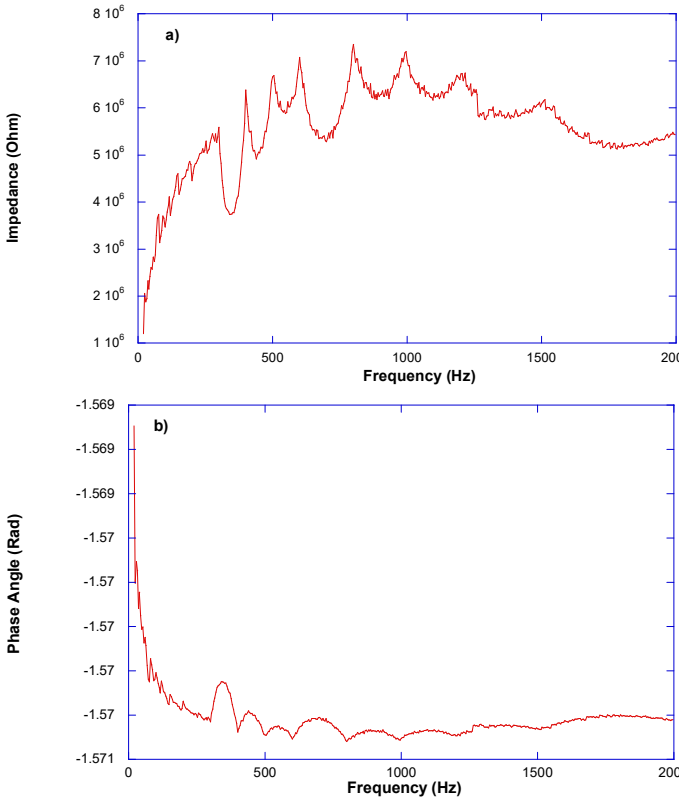

Figure 2. plots showing the impedance (a) and phase angle (b) as a function of AC frequency up to 2KHz of as-received test chip. Amplitude of ac voltage was ~1V.

The employment of LFIS shows that detection of the damage is possible even when DC resistance is almost unchanged. A typical LFIS behavior of the test pattern is shown in Fig. 2, where the measured impedance and phase angle is displayed as a function of 1V AC frequency up to 2KHz. At first glance, the measured impedance and phase angle appears to be meaningless with various noises. However, extraction of AC resistance (R) and inductance (L) using a simple equivalent circuit consisting of parallel connection of a resistor and inductor indicates that the data is not a random noise but is related to the test structure. The data shown in Fig. 3 displays the fit result of the case with an equivalent circuit of a simple parallel connection of a resistor and an inductor. The fit result taken from the circuit assumed to a serial connection is essentially the same. Note the fact that the AC resistance is reasonably constant over frequencies and does not change much with AC voltage amplitude used for the measurement. Interestingly, the inductance plot shows 7 humps, matching with 7 serpentines in the test pattern. This means that what appears to be a random noise in impedance is rooted to the coupled effect of resistance and inductance of the circuit. It should be noted that the inductance shown in these plots is not correct because the circuit is much more complex than a simple serial or parallel connection of resistor and inductor. The circuit is with a considerable level of capacitance

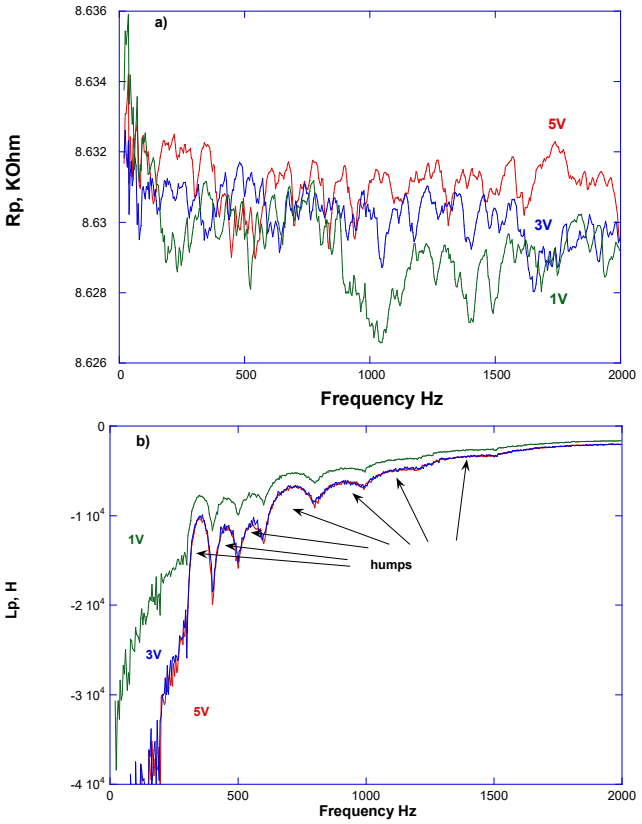

Figure 3. plots showing the AC resistance and inductance as a function of frequencies extracted from the data shown in Fig.2 using a simple equivalent circuit made of parallel connection of a resistor.

because of interlevel dielectric layer producing coupling effect between M1 serpentines and M2 pads. Because of the capacitive coupling, the extracted value of inductance is shifted to the negative value domain, indicating that the circuit property under AC signal is affected by capacitive component.

An extraction of the AC circuit components requires a construction of correct equivalent circuit and significant

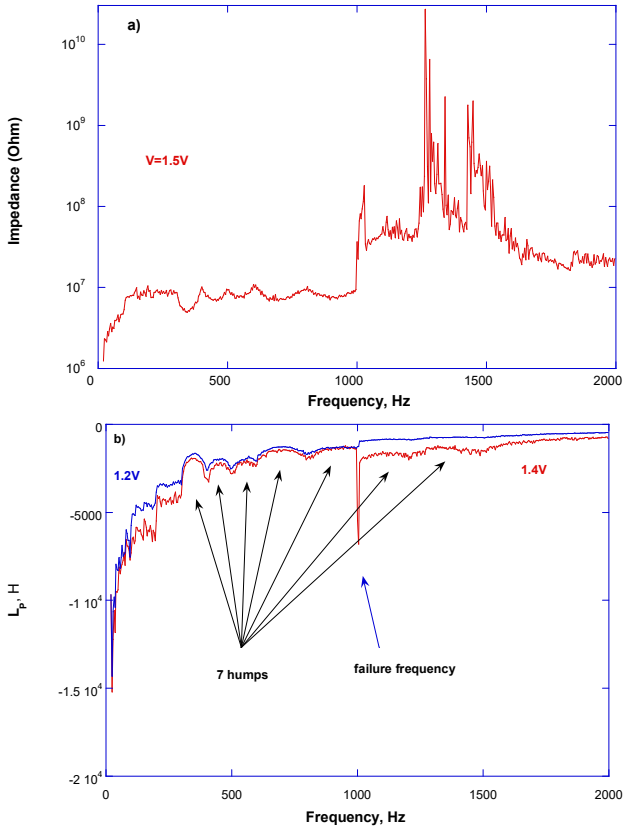

Fig. 4 plots showing the impedance (a) and inductance (b) as a function of AC frequency taken from samples subjected to 1000 thermal cycles.

computational simulations. However, the detection of failure is possible from a simple measurement of impedance at a few AC amplitudes. Where there is no physical damage, the circuit produces results essentially the same as the ones in Figs. 2-3. With existence of damage, the impedance at a voltage above the critical exhibit a dramatic change. Fig. 4 presents an example of such behaviors. The data shown in these plots are taken from the chip subjected to 1000 thermal cycle. The DC resistance of these samples are measured to be almost unchanged by the thermal cycling. However, when the impedance is measured at 1.4V or higher, it increases by several orders of magnitude at higher frequencies. As shown in Fig. 4-b, where parallel inductance taken from the data measured at slightly lower AC amplitudes (1.2 and 1.4V), the inductances show the usual 7 humps. Note the presence of a sharp spike appearing at ~1kHz, which is located in 5th humps. Our analysis indicates that the spike is related to the breakdown of the dielectrics, making the circuit to be less capacitively coupled and dominated more by inductance

component. The exact mechanism by which the circuit behavior changes to Fig. 4-b with the breakdown needs further studies, but the data alone is sufficient to conclude that there exists a SPI damage at the 5th serpentine. Each hump corresponds to the serpentine, and it is a result of LC resonance linked to a serial component of R in the circuit. It is therefore possible to locate the serpentine responsible for the failure seen in the impedance measurement. In this way, the impact of solder bump induced stress on the BEOL interconnect failure and most failure prone location can be effectively studied without complexity in measurement method and expensive equipment.

B. Characterization of solder joint damage

Solder joints are prone to reliability failure by SPI induced damaging mechanisms such as thermal fatigue, becoming one of the main challenges against the advances in device packaging technologies. The concern on the reliability demands resource intensive testing of various kinds. The burden of conducting failure analysis can be reduced when a simple and effective method of quantifying the damage level in the solder joint becomes avaiable but such method is not presently avaiable. The simplest may be to design an open circuit test pattern and measure DC resistance. The main limitation of this method is that the circuit contains very low resistance and resistance is not very sensitive to the damage size. As an alternative, we have explored the possibility of using LFIS technqiue in characterization of damage in solder joints. The technique needs further refinement and development of theoretical support, but our exploration indicates that it is with promising potential of providing an effective solution to the characterization challenge.

Our approach is based on the simple theory of the skin effect, which suggests that the impedance of a conductor increases with frequency, that is

$$\delta = \sqrt{\frac{\rho}{\mu f}} \qquad (1)$$

where δ is the skin depth, ρ is the resistivity of conductor, μ is the permeability, and *f* is the frequency. The skin effect arises because the conducting electrons tends follow the surface under AC conditions. When a defect along the outer edge exists, such as cracks or Kirkendall void clusters, the current is forced to conform and change its path around the damages, amplifying the AC resistance with frequency.

In applying the skin effect to the detection of solder joint damage, it is important to realize that the AC resistance measured in a real test pattern reflects various factors. The most influential factor is the dimension of various components in the circuit including Cu leadframe, solder joint, intermetallic component, and Cu trace on Si chip. With an aim of understanding the AC resistance, we have developed FEM model that computes the resistance for given geometry. This analysis suggests that the frequency dependence of AC resistance is a sensitive function of the cross-sectional area of a component. Fig. 5 shows an example of AC resistance computed for a Cu cylinder with varying diameter. Note that AC resistance (or skin effect) is sensitively affected by the diameter of the Cu cylinder. The AC resistance rises because current becomes concentrated at the surface layer at high frequency. In cases when the diameter of conductor is too small, the skin effect does not appear in the low frequency regime because the skin depth is too large to affect resistance at those frequencies. What this result suggests is that damage analysis using LFIS does not need to consider the impact of a component with a small cross-sectional area. The solder joint is usually the largest or second largest conductor in the open circuit test structure common in industry, making impedance data easier to analyze than expected. Any change in the impedance with frequency can be safely related to the signal rooted to the microstructural features in the solder joint or adjacent component. For the usual open circuit test pattern containing solder joint, the AC resistance can be expressed as linear sum of component resistance, namely

$$R(f) = R_{LF}(f) + R_{Solder}(f) + R_{Tr}(f) \qquad (2)$$

where R_{LF}, $R_{solder,}$ and R_{Tr} denote the AC resistance of leadframe, solder joint, and Cu trace in Si chip, respectively. According to the mechanism shown in Fig. 5a, $R_{Tr}(f)$ would have negligible influence on frequency dependent part of the total AC resistance at nominal frequencies we use for LFIS. On the other hand, $R_{LF}(f)$ would show the most sensitive to the

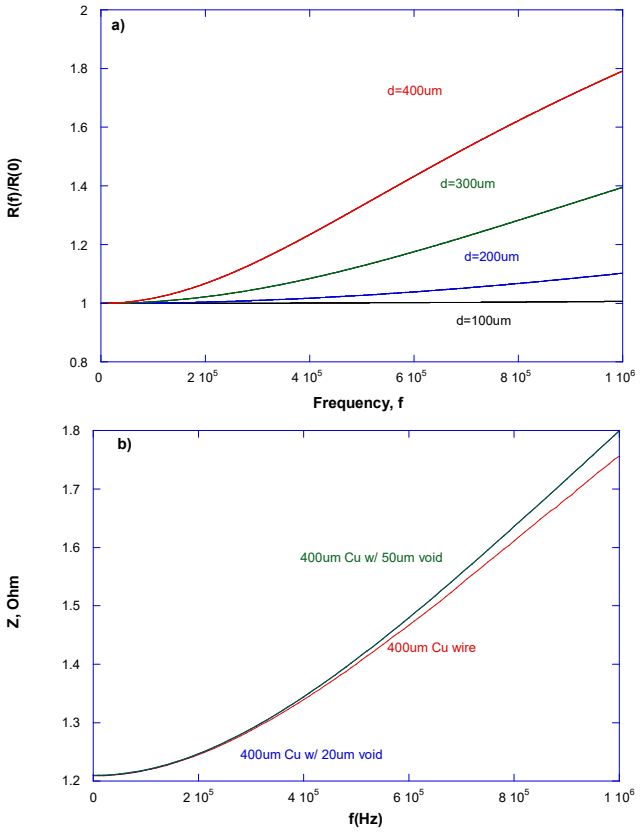

Figure 5. Plots showing AC resistance as a function frequency for ideal Cu with 4 different wire diameters (a) and FEM computed impedance of 400 um Cu wire with various sizes of a spherical

frequencies but its impact can be negligibly small to the total resistance because $R_{LF}(f)$ itself is very small in magnitude. Therefore, it can be assumed that

$$\frac{dR(f)}{df} \sim dR_{Solder}(f)/df. \quad (3)$$

The damage at the solder joint can make the frequency dependence to be even further increased because it amplifies the skin effect. FEM analysis on the surface damage effect is shown in Fig. 5b where an impedance of long 400um diameter Cu cylinder is calculated with introduction of 2 different size of voids at the Cu surface. It can be seen that the surface damage makes the AC resistance to be more dependent on the surface damage.

Fig. 6 shows an example data collected from our early exploration of the LFIS technique in studying damage development in solder joint. The sample used for this experiment contains patterns with the low resistance open circuit test structures with ~100mm diameter solder joint. Notice that the samples subjected to 1000 thermal cycles exhibit increased sensitivity of AC resistance to the frequency, adding to the evidence that the skin effect is affected by damage in the solder joint. The difference in AC impedance, which is almost the same as the AC resistance with negligibly small phase angle, between the as-prepared and the thermal cycled increases with an increase in the test signal frequency.

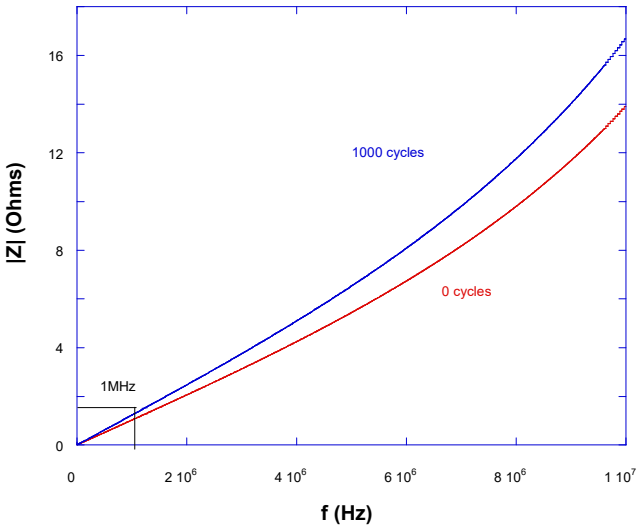

Figure 6. A plot comparing the impedance of test pattern before and after 1K thermal cycling. Measurement is conducted up to 10MHz

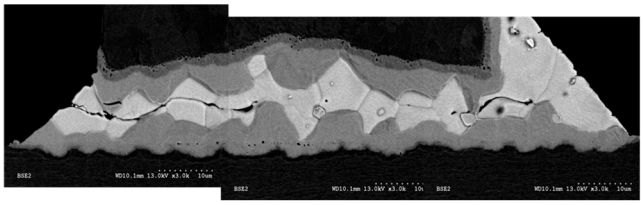

Figure 7. A SEM micrograph showing the typical microstructure of solder joint after subjecting it to thermal cycle treatment. Note the formation of fatigue crack developed along the solder matrix.

At 1MHz, the difference in the impedance is less than 0.5 Ohm, but it increases to over 2 Ohms at 10MHz. The samples showing the large increase in the impedance usually shows the joint microstructure with a visible sign of cracking as displayed in Fig. 7. These results may provide evidence to the fact that LFIS can be an effective tool for characterizing the damage developing at the solder joint. It will be especially effective for a solder joint that is large in size such as the BGA assembly. With the large ball diameter, the skin effect would be sizable even at low frequencies.

The detection of damage within the solder joint using LFIS is with a promising potential as demonstrated in Figs. 6-7. However, it is not without limitations that demand careful consideration in practice. The most challenging is the fact that damage quantification cannot be done in a simple manner. As presented in Eq. (1)-(3), the solder joint is not the only component that affects the frequency dependence of the impedance. Any component in the test circuit can make a sizeable impact on the impedance especially when the component is with comparable dimension to the solder joint. A method of isolating and quantifying damage in the solder joint with reasonable immunity to the errors from AC resistance of other components needs to be developed. For this, various attempts have been made to define the damage factor. Among the methods that have been attempted, is the damage factor defined as

$$D = Z(1MHz)/Z(0Hz) \quad (4)$$

where Z(0Hz) represents the impedance at 0 frequency, which is determined from the linear extrapolation of the impedances measured at high frequencies. One of the examples of the damage factor measured as a function of thermal cycling is shown in Fig. 8. It can be seen that the damage factor increases with the number of thermal cycles, suggesting that the damage factor in Eq. (4) may properly represent the damage developed in solder joint. The data presented in this figure is taken from the impedance measured up to 1MHz. The accuracy would increase when the measurement frequency is expanded to

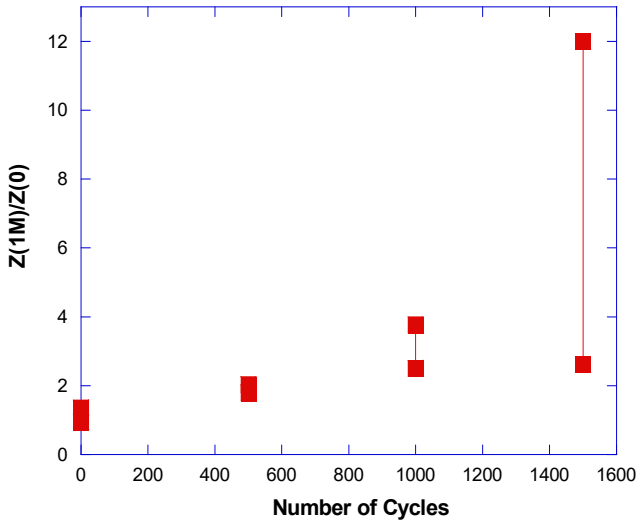

Figure. 8 A plot showing the change in the damage factor, Z(1MHz)/Z(0Hz), of solder joint as a function of thermal cycling.

10MHz. Higher frequency measurements would be especially beneficial since the circuit is made of micro-solder joints. In addition, it is also desirable to determine the impedance signal unique to the damage in the solder joint. Such signals have not been found yet, but a few candidates have been determined. If any of these signals can be related to the physical damage in solder joints, it can enhance the confidence of the quantification. The search for the unique signal continues in our labs and the result will be available in future publications.

CONCLUSIONS

This study demonstrates the promising potential of the low-frequency AC response of an interconnect test circuit in assessing damages in the packaging interconnects, especially those caused by SPI. We have shown the possibilities available in detecting the damages specifically in the BEOL interconnects and solder joint using fairly simple non-destructive characterization measurements. Presently, there is still much to learn in regard to the full meaning of certain signals and mechanisms in place in SPI. Future work will involve enhancement in the detection effectiveness by better understanding the underlying mechanisms and fine tune the excitation signal and response frequency ranges.

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