

Electro-optical characterization of arsenic-doped CdSeTe and CdTe solar cell absorbers doped in-situ during close space sublimation

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ABSTRACT

Most contemporary device models predict that an acceptor concentration of at least 10^{16} cm^{-3} is required to reach an open circuit voltage of 1 V in polycrystalline CdTe-based solar cells. While copper has traditionally been used as the *de facto* p-type dopant in polycrystalline cadmium telluride (CdTe) and cadmium selenide telluride (CdSeTe), reaching high acceptor concentrations has proved to be challenging in such devices due to significant dopant compensation. The acceptor concentration in copper-doped CdTe and CdSeTe typically ranges from 10^{13} to 10^{15} cm^{-3} and routinely exhibit low external radiative efficiencies below 0.01%, limiting their implied voltage (i.e., quasi-Fermi level splitting) to approximately 900 mV. As an alternative to copper, this work explores the use of arsenic as a p-type dopant for CdTe and CdSeTe. Using a novel technique in which a thin layer of arsenic-containing material is deposited and used as a reservoir for arsenic to diffuse into a front layer of previously undoped material, this contribution demonstrates that high external radiative efficiencies are achievable, a direct result of combined high acceptor concentrations and long minority-carrier lifetimes in the absorber. This leads to improved implied voltages, and indicates that As-doping represents a promising pathway towards improving the external voltage of CdSeTe/CdTe solar cells.

1. Introduction

Solar cells based on cadmium telluride (CdTe) and its alloy cadmium selenide telluride (CdSeTe) are the most commercially successful thin-film solar technology today. With more than 6 GWp of annual production, Cd(Se)Te is second only to crystalline-silicon-based technologies in annual production and global deployment [1]. With a direct bandgap at 1.4–1.5 eV, Cd(Se)Te exhibits a sharp band edge with absorption spanning a large portion of the AM1.5G spectrum [2]. As a result, only a few micrometers of material are required for near-total absorption of above-bandgap light, and this—paired with CdTe's relative defect tolerance—makes rapid deposition technologies such as Close-Space Sublimation (CSS) and Vapor Transport Deposition (VTD) cost-effective fabrication methods of polycrystalline material [3,4]. These attributes facilitate the rapid manufacturing of relatively efficient modules, driving down costs and contributing to the commercial success of the technology.

However, Cd(Se)Te technology also faces challenges which must be addressed to ensure its continued viability in the global market. The steady cost reductions of commercially available silicon modules as well as the extremely rapid improvement of research-scale perovskite cells creates pressure for Cd(Se)Te-based modules to advance as well. Most of the recent progress in photovoltaic conversion efficiency for CdTe can be attributed to improvements in the electron contact layer—sometimes referred to as the “buffer” layer in the CdTe community—as well as the alloying of selenium into the front portion of the absorber [5,6]. These modifications have significantly improved the short-circuit current density (J_{SC}) and fill factor (FF) but have had little impact on the open-circuit voltage (V_{OC}), which has remained below 900 mV [7]. Maintaining V_{OC} while reducing the bandgap through selenium alloying has somewhat reduced the voltage deficit—defined as the difference between the ideal, radiative-recombination-limited $V_{OC,rad}$ and the measured V_{OC} —yet it still remains high when compared to competing technologies. Given a bandgap of 1.4–1.5 eV, depending on selenium

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content [8], J_{SC} and FF are now roughly 94% and 88% of their respective single-junction theoretical limits whereas V_{OC} is only ~70–78% of its 1100–1230 mV theoretical limit [9,10]. With a voltage deficit of over 200 mV, improving the voltage of Cd(Se)Te-based devices remains both the single greatest challenge and the biggest potential path toward exceeding the current record efficiency of 22.1% [7].

One of the long-standing strategies for improving the open-circuit voltage of Cd(Se)Te devices has been improving the acceptor concentration through doping. CdTe, when deposited via CSS, contains approximately 10^{12} – 10^{14} free holes per cubic centimeter without the addition of an impurity dopant [11,12]. This is predominately due to cadmium vacancies (V_{Cd}) which act as a p-type dopant in CdTe [13]. Copper has historically been used to dope CdTe, but despite its widespread use, it is only capable of increasing the free hole density to 10^{13} cm^{-3} to low- 10^{15} cm^{-3} . This is due to the incomplete ionization of Cu — which is a relatively deep acceptor located 220 meV above the valence-band maximum [14]—and self-compensation [15,16]. In recent years, multiple modeling studies of Cd(Se)Te-based devices have been published with the goal of predicting what parameters will be necessary to achieve 25% [17,18] or even 28% efficiency [19]. While they examine different combinations of carrier lifetime, doping density, interface recombination and n-type material properties, they agree that an acceptor concentration of approximately 10^{16} cm^{-3} or more is required for p-type polycrystalline CdTe to reach an open-circuit voltage of 1 V.

To achieve such high acceptor concentrations while avoiding the deleterious effects of copper doping, numerous studies have explored the use of group-V elements to dope CdSeTe and CdTe. In recent years, P, Sb, and As have all been proposed as potential candidates [20]. Utilizing molecular beam epitaxy, Farrell et al. reported arsenic incorporation of up to 10^{17} cm^{-3} and hole concentrations of up to 5×10^{16} cm^{-3} when a cadmium flux was supplied to encourage cadmium-rich growth conditions during in-situ arsenic doping [21]. Using arsenic to dope single-crystal CdTe, Nagaoka et al. reported hole concentrations of up to 10^{17} cm^{-3} and dopant activation as high as 50% when at an arsenic concentration of 3×10^{16} cm^{-3} , with the activation rate falling when the arsenic concentration was further increased. This resulted in an open circuit voltage of 900 mV [22]. Burst et al., using phosphorus to dope single-crystal CdTe, achieved a hole density of 10^{17} cm^{-3} , 50% dopant activation, and minority-carrier lifetimes of hundreds of nanoseconds, leading to samples with an open-circuit voltage above 1 V [23]. Using Vapor Transport Deposition (VTD), McCandless et al. demonstrated successful in-situ dopant incorporation and activation in polycrystalline CdTe, with P, As, and Sb as the dopant species [20]. Utilizing sputtered CdSe, sublimated CdTe, and low-temperature ex-situ AsCl₃ treatments, Li et al. showed improved hole concentrations, carrier lifetimes, and device performance compared to copper-doped baselines [24]. Furthermore, Metzger et al. reported hole concentrations above 10^{16} cm^{-3} in VTD-deposited CdSeTe/CdTe bilayer structures with a conversion efficiency of greater than 20%, the highest reported to date for any sample doped with group V elements [25]. Finally, Krasikov et al. found that arsenic-doped CdSeTe cells exhibited far more stable hole concentrations during accelerated lifetime testing compared to copper-doped samples. This in turn led to virtually no device performance degradation in arsenic-doped samples, whereas copper-doped samples showed significant degradation over the course of the study [16].

In this contribution, we explore in-situ arsenic doping of CdTe and CdSeTe devices using co-sublimation of Cd(Se)Te:As and cadmium to optimize arsenic incorporation and dopant activation. We compare the electro-optical properties of copper-doped absorbers with arsenic-doped ones. Furthermore, we compare arsenic-doped structures where arsenic is deposited throughout the absorber with structures where only a thin layer of arsenic-containing material is deposited and the arsenic diffuses into the bulk of the absorber post-deposition during the CdCl₂ activation treatment. Utilizing capacitance-voltage (CV) and time-resolved photoluminescence (TRPL), we show that arsenic-doped devices exhibit

significantly higher carrier concentrations and carrier lifetimes than copper-doped samples. Secondary ion mass spectrometry (SIMS) provides evidence for the diffusion of arsenic atoms during CdCl₂ processing and the possibility of a graded doping profile. Finally, photoluminescence (PL) and external radiative efficiency (ERE) measurements indicate that arsenic-doped CdSeTe samples have the potential to lead to voltages approaching 1 V, far exceeding what has been accomplished to date using copper doping.

2. Device structure

Three distinct device structures were utilized over the course of this study. Fig. 1 provides a visual comparison of these structures. The first structure, in Fig. 1a, shows a “non-diffused” arsenic-doped structure where several microns of arsenic-doped CdSeTe or CdTe are deposited directly on the MgZnO electron contact layer. In this case, the entire absorber contains arsenic as it is deposited. A second “diffused” arsenic-doped structure is shown in Fig. 1b. Here, a layer of un-doped CdSeTe with a thickness of 1–4 μm is deposited on the MgZnO layer, followed by a 1 μm thick layer of doped CdSeTe:As or CdTe:As and a 500 nm CdSeTe capping layer. In this structure, doping of the bulk of the absorber is achieved through diffusion of As from the back to the front of the device during the CdCl₂ activation treatment. That is, the front portion of CdSeTe remains undoped until arsenic diffusion occurs during the chlorination process. Although both CdSeTe:As and CdTe:As were explored, this work focuses on the results of using CdSeTe:As due to its drastically improved luminescence, radiative efficiency, and TRPL-measured lifetimes. Finally Fig. 1c shows a conventional copper-doped structure which represents Colorado State University’s CdSeTe/CdTe bilayer baseline structure. In this final structure, doping is achieved through an ex-situ post-deposition CuCl diffusion process described below.

3. Experimental methods

3.1. Sample fabrication

In this study, both CdSeTe:As and CdTe:As absorber materials were explored. All films were deposited on Pilkington TEC10 substrates, which are commercially available glass substrates coated with approximately 400 nm of fluorine-doped tin oxide (FTO) with a sheet resistance of 10 Ω /square. 100 nm of MgZnO was deposited by magnetron sputtering onto the FTO to serve as a buffer layer/electron contact. The MgZnO was deposited at 140 W RF power across a 4” diameter target in an environment maintained at 5 mTorr by relative flow rates of 3% O₂/97% Ar process gas. The oxide target was composed of 11 wt% MgO and 89 wt% ZnO at 99.99% purity. After a vacuum break, the substrates were transferred to the absorber-deposition chamber, where they were preheated to 500 °C and immediately transferred to one of several deposition stations within the chamber, as described in Ref. [26]. Films were deposited in a 40 mTorr nitrogen environment. CdSe_{0.4}Te_{0.6} with an As concentration of 10^{20} cm^{-3} was used as the source material for the deposition of CdSeTe:As. The CdTe:As source material also had an arsenic concentration of 10^{20} cm^{-3} . The temperatures of the source material heater and the substrate heater for all materials are shown in Table 1. All arsenic-containing source materials were deposited using cadmium co-sublimation with a cadmium source maintained at 210 °C to provide cadmium overpressure using co-sublimation hardware as described previously [27]. The cadmium source temperature was chosen based on vapor pressure calculations, aiming to achieve a 20% Cd overpressure, similar to the conditions shown in Ref. [21]. The CdTe:As and CdSeTe:As source materials were prepared by the High Pressure Bridgman (HPB) growth technique to melt CdTe, CdSe, and Cd₃As₂ with Cd overpressure as described in Ref. [28]. Following deposition, the “non-diffused” samples and the copper-doped samples (identified in Fig. 1a and c, respectively) received a 600 s CdCl₂ treatment with the

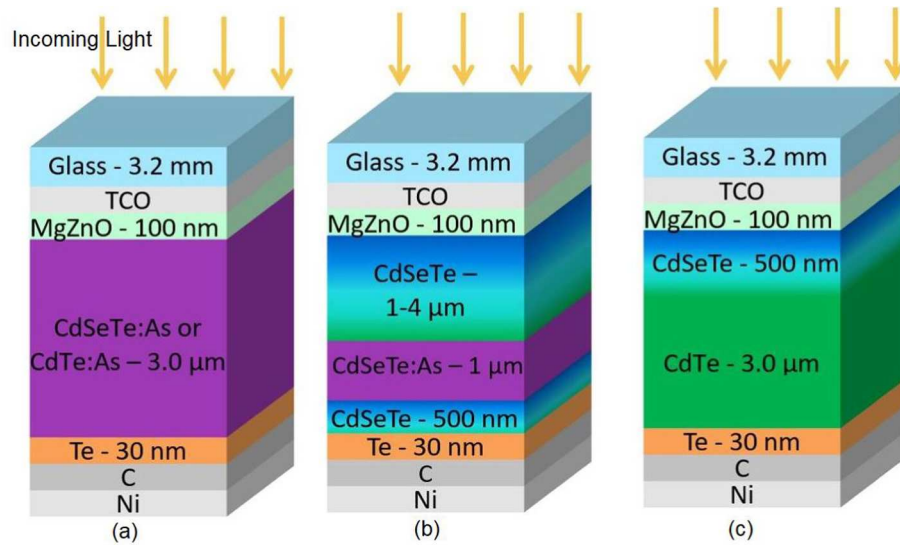


Fig. 1. Device structure for (a) “non-diffused arsenic” samples, (b) “diffused arsenic” samples where the majority of the absorber contains no arsenic prior to the CdCl_2 heat treatment during which the arsenic diffuses towards the front, and (c) copper-doped baseline samples which received a post-deposition CuCl treatment. Not to scale.

Table 1
Absorber deposition temperatures.

	CdSeTe	CdTe	CdSeTe: As	CdTe: As
Substrate Heater Temp ($^{\circ}\text{C}$)	420	500	420	500
Source Temp ($^{\circ}\text{C}$)	575	555	575	555
Cadmium Overpressure Source ($^{\circ}\text{C}$)	–	–	210	210

source and substrate heaters maintained at 450°C and 420°C respectively. The samples were then annealed at 400°C for 1200 s. The CdCl_2 treatment and anneal were performed immediately after absorber deposition and without breaking vacuum. “Diffused” samples, identified in Fig. 1b, received a more aggressive 900 s CdCl_2 treatment where the temperatures of the source and substrate heaters were maintained at 480°C and 430°C respectively. One sample, identified and discussed in the section titled “Acceptor concentration improvement” received two CdCl_2 treatments. Once cooled, and following a vacuum break, all samples received 40 nm of evaporated 5N-pure Te to form the back hole contact. The back electrode was formed by consecutive spray coating of carbon and nickel paints suspended in a polymer binder. A mask was overlaid on the samples and glass bead-blasting was used to delineate small-area devices of approximately 0.6 cm^2 . For comparison, copper-doped CdSeTe/CdTe samples were also fabricated, with ex-situ copper doping achieved through CuCl treatment performed after deposition of the absorber and the CdCl_2 process, as described in Ref. [29].

3.2. Characterization

3.2.1. Capacitance–voltage measurements

Capacitance–frequency measurements were performed with voltage bias from -2 to 0.2 V to confirm that capacitance was independent of bias and frequency in the range of 100 kHz, where CV measurements were taken. Using the standard analysis technique which assumes an abrupt junction [30], capacitance was measured from -1 to 0.75 V . An assumed permittivity of $8.32 \times 10^{-13}\text{ F cm}^{-1}$ was used for calculations of carrier concentrations.

3.2.2. Time-resolved photoluminescence

Single-photon time-resolved photoluminescence (TRPL) measurements were performed at NREL using the time-correlated single-photon

counting (TCSPC) technique. Glass-side excitation of samples was performed with a 300 fs pulsed laser at a wavelength of 640 nm. The 44 nm bandpass filter was centered at 819 nm, which is at the high energy side of the PL emission (PL emission maximum was at 890 nm) By measuring charge carrier lifetimes at energy slightly higher than the bandgap, we minimize potential trapping effects.

3.2.3. Photoluminescence emission spectroscopy

Steady-state photoluminescence emission spectra were measured at NREL with a Princeton Instruments HR300 spectrograph and a Pixis400 Si CCD camera. Using a HeNe laser, samples were photo-excited at room temperature with 632.8 nm laser light. Prior to measurement, the instruments were calibrated for spectral sensitivity using manufacturer-provided calibration lamps.

3.2.4. External radiative efficiency measurement

ERE measurements were performed at Arizona State University using a Thorlabs DET10N2 InGaAs photodetector. Samples were illuminated with a steady 1-sun-equivalent white LED bias light and a low-power 532 nm laser chopped at 110 Hz. A 715 nm long-pass filter prevented the excitation laser light from reaching the photodetector. The excitation photon current was calibrated using a Spectralon reflectance standard of known reflectance (2%) without the long-pass filter. A SR830 lock-in amplifier from Stanford Research System extracted the chopped PL signal from the background noise. Detailed descriptions and diagrams of this method are presented in [31,32].

3.2.5. Time of Flight (TOF) secondary ion mass spectrometry

TOF-SIMS data was collected using an IonToF TOF.SIMS 5 instrument operated in Spectroscopy mode at Colorado School of Mines. A $150\text{ }\mu\text{m} \times 150\text{ }\mu\text{m}$ area of the film was rastered using a 30 keV Bi^+ Primary Beam. The sputter source was a 1 keV thermal ionization Cs^+ source. Samples measured at EAG Laboratories were prepared and measured using proprietary methods. To study the arsenic concentration near the front interface, and minimize the effects of differing sputter rates and film roughness, the films sent to EAG were peeled from the substrate and analyzed from the peeled surface which corresponds to the MgZnO/CdSeTe interface.

3.2.6. Scanning electron microscopy and energy dispersive X-ray spectroscopy

SEM and EDS analyses were performed at University of Illinois Chicago. Electron microscopy images were taken using a JEOL JSM IT500HR field-emission SEM equipped with a high-brightness electron gun system delivering high-resolution field-emission performance. EDS data were gathered using an Oxford XMax60 EDS detector.

4. Results and discussion

4.1. Non-diffused method

To quantify arsenic incorporation, SIMS measurements were performed on films in the “non-diffused” configuration, shown in Fig. 1a. During film deposition, the cadmium co-sublimation source provided an additional cadmium vapor flux impinging on the growing film, with the purpose of achieving a cadmium overpressure to encourage the formation of tellurium vacancies (V_{Te}). Arsenic atoms may then react with the resulting V_{Te} , leading to the formation of As_{Te} sites which act as p-type dopants. This strategy has been successfully used in CdTe films grown by molecular beam epitaxy (MBE) to increase and control arsenic incorporation [21]. In our case, we hypothesized that arsenic incorporation would increase with the temperature of the cadmium source. After film deposition, the samples received the standard 600 s $CdCl_2$ treatment described in the experimental methods section followed by the 1200 s anneal at 400 °C without breaking vacuum. Fig. 2a shows the SIMS arsenic profiles of CdTe:As test structures deposited identically, with the exception of the cadmium source temperature and consequently, the cadmium overpressure during sublimation—which was varied. Unexpectedly, over the temperature range tested, the amount of cadmium overpressure provided by the co-sublimation source did not have a significant effect on arsenic incorporation. When compared against a CdTe:As standard of known arsenic concentration produced at NREL, these signals correspond to an arsenic concentration of 10^{18} cm^{-3} , indicating approximately a 1% incorporation rate from the source charge (with an arsenic concentration of 10^{20} cm^{-3}). The difference in sputtering times between the samples deposited with and without cadmium overpressure is due to a difference in sample thickness rather than a difference in the sputter rate.

Given the demonstrated connection between the concentration of tellurium vacancies and the activation of arsenic in CdTe [20], we further hypothesized that an optimized cadmium overpressure could promote high concentrations of activated arsenic acceptors (As_{Te}) without pushing the cadmium overpressure so high that interstitial cadmium (Cd_i)—which is a deep donor defect—becomes prevalent [13]. However, despite the high arsenic concentration achieved in these films, the finished devices exhibited low hole densities, typically 10^{14} cm^{-3} as

measured by CV. This is comparable to the carrier concentration found in films without intentional doping. Fig. 2b shows the CV curve for a typical CdTe:As device fabricated using the “non-diffused” methodology. Although only a single CV curve is presented here, all samples exhibited similar carrier concentrations, regardless of cadmium overpressure.

To understand these low carrier concentration, samples of the source material were prepared for scanning electron microscopy (SEM) and energy dispersive spectroscopy (EDS) analysis. The EDS maps in Fig. 3 for CdSeTe:As source material show that arsenic was not uniformly dissolved as monoatomic arsenic into the source material but rather had a tendency to cluster into areas of high arsenic concentrations consisting primarily of CdAs. CdTe:As source material was similarly studied.

The clustering of arsenic in the source material provides a possible explanation for the low carrier concentrations observed. If the arsenic is present in monoatomic form in the source material, it is expected that it will sublimate and react at the film surface as monoatomic arsenic and, thus, result in the activated dopant As_{Te} . If, however, the source material predominately contains CdAs, it will sublimate and impinge onto the growing film as As_4 , leading to the formation of defects instead of acceptors. These findings are similar to those of Burton et al., who similarly found arsenic clusters of As_2 and As_4 in MBE-deposited films [33]. In several other MBE-based studies, arsenic crackers were utilized to dissociate As_4 and As_2 and improve dopant activation [21,34].

4.2. Diffused method

Based on these findings, it appears unlikely that high arsenic activation can be obtained from direct sublimation of CdSeTe:As and CdTe:As, and further steps are required to obtain activated As. Therefore, a new structure was devised, which was designed to only allow monoatomic arsenic species into a portion of the absorber. This design, referred to as the “diffused” structure, and shown in Fig. 1b, was inspired by the density functional theory (DFT) modelling results from Krasikov and Sankin [35]. They showed that interstitial arsenic (As_i) experiences a significantly smaller diffusion barrier compared to the other As species, complexes, and AX centers—a self-compensating defect that can form when substitutional acceptors become deep donors due to lattice relaxation near certain impurities [36]. This suggests that As_i may be the only arsenic species capable of diffusing a significant distance during fabrication. Thus, the “diffused” structure is composed of a 2.5 μm -thick front layer of initially undoped CdSeTe followed by a 1 μm layer of either CdSeTe:As or CdTe:As. We hypothesize that during the aggressive $CdCl_2$ treatment, interstitial arsenic will diffuse from this back “reservoir” of arsenic into the front layer, resulting in two distinct arsenic-containing layers within the film: a front “diffused” layer where only monoatomic arsenic is present; and the back “reservoir” layer

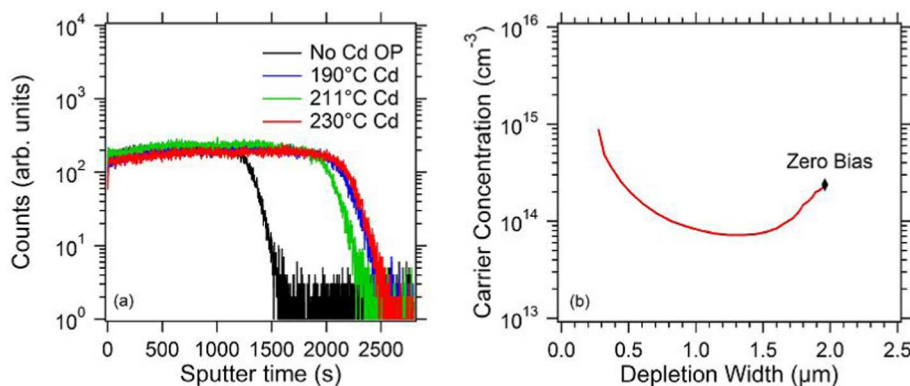


Fig. 2. (a) SIMS profile showing arsenic incorporation vs sputter time for CdTe:As films with various Cd overpressures. Reference to a known standard indicates approximately 10^{18} cm^{-3} arsenic atoms in all films. Differences in the SIMS profiles result from different film thicknesses rather than different sputter rates or arsenic profiles. (b) CV plot showing low carrier concentration in a non-diffused CdTe:As sample, despite high arsenic concentration into the film.

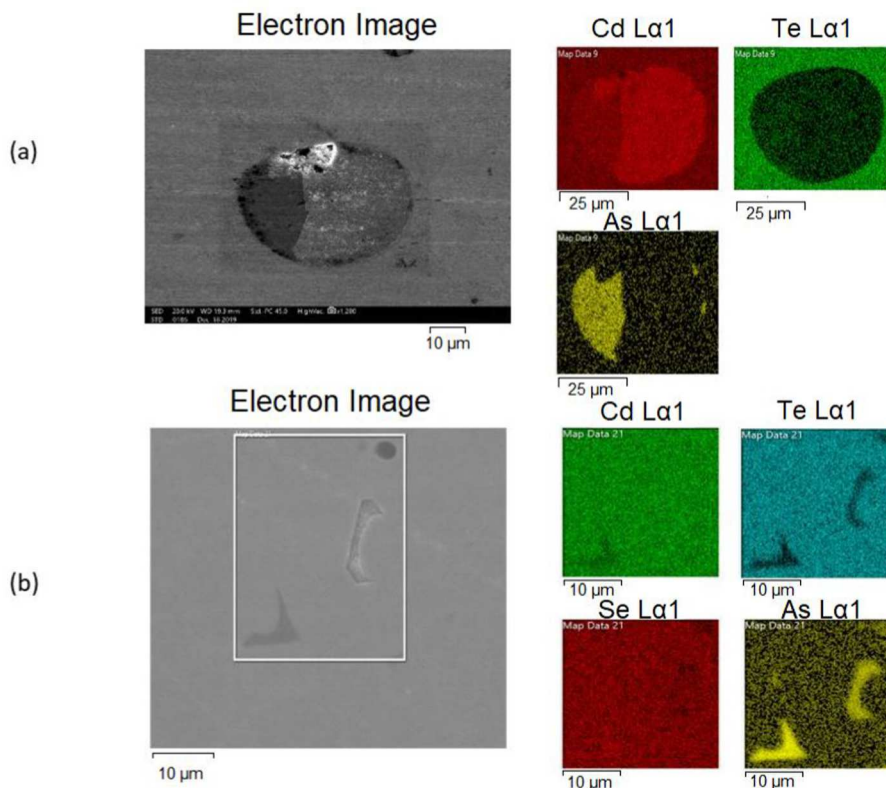


Fig. 3. Scanning electron microscopy image (left), showing a low magnification view of the source material surface and EDS map (right) showing non-uniform arsenic concentration in CdSeTe:As.

where the less mobile complexes and AX centers are retained.

To verify our hypothesis of higher arsenic incorporation and activation when using this “diffused” method, SIMS measurements were conducted on “diffused” CdSeTe/CdSeTe:As films by EAG Laboratories and the results are shown in Fig. 4a. To gain insight into the As diffusion profile without complications from surface roughness, the entire film was peeled from the substrate and measured from the front interface using a proprietary method. This profile shows arsenic concentration as high as 10^{19} cm^{-3} at the back of the film—in the “reservoir” region doped *in-situ*—when using a source material with an arsenic concentration of 10^{20} cm^{-3} . Interestingly, the arsenic concentration in the “non-diffused” CdTe:As shown in Fig. 2a only reached 10^{18} cm^{-3} , although it was deposited from a source material with the same arsenic concentration. This may indicate that arsenic more readily incorporates into CdSeTe. The arsenic signal decreases towards the front interface until it reaches the SIMS detection limit for arsenic at $5 \times 10^{15} \text{ cm}^{-3}$. The rise in the arsenic signal right at the MgZnO/CdSeTe interface is

believed to be primarily due to a known signal interference between arsenic and MgOCl, however arsenic accumulation at the front interface is also possible. The arsenic profile seen in Fig. 4a results from the combination of arsenic species present in the sample. This likely includes substantial amounts of immobile arsenic complexes retained in the “reservoir” at 2.5–4 μm from the front interface, and monoatomic As_i that diffuses rapidly towards the front interface and ultimately reacts to form more stable but less mobile As_{Te} [35].

4.2.1. Dopant activation

The location “A” in Fig. 4a and b is a point of interest, corresponding to the depth within the film where the zero bias point occurs in the CV profile. This allows us to compare the carrier concentration and the total arsenic concentration and, thus, to calculate the dopant activation. Fig. 4b shows a hole concentration of $1.3 \times 10^{15} \text{ holes/cm}^3$ at a depth of 0.7 μm from the front interface was measured at the zero-bias point. At the corresponding point in the SIMS data (Fig. 4a), the most

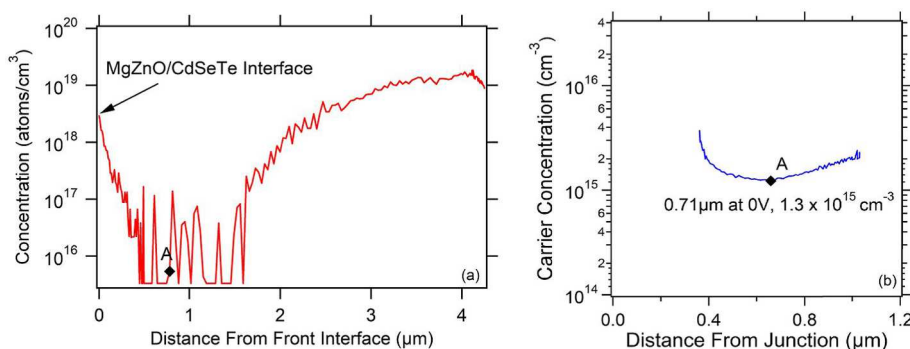


Fig. 4. (a) SIMS profile showing the arsenic concentration in a “diffused” CdSeTe/CdSeTe:As sample. SIMS was performed at EAG Laboratories. Point “A” corresponds to the same point on the CV plot for dopant activation comparison. (b) CV profile from the same device indicating a carrier concentration of 10^{15} cm^{-3} .

conservative estimate of $5 \times 10^{15} \text{ cm}^{-3}$ total arsenic concentration was taken given the SIMS detection limit. As such, an activation ratio of at least 26% is obtained. If the total arsenic concentration is some value lower than the SIMS detection limit, the activation ratio will be correspondingly higher.

4.2.2. Acceptor concentration improvement

Due to the initial success of the “diffused” method to produce films with an improved density of activated acceptors, several follow-on experiments were conducted to optimize the process and further increase the acceptor concentration. Fig. 5 shows the CV plots that resulted from these experiments, demonstrating that several different device structures utilizing the “diffused” methodology have produced hole concentrations in excess of 10^{15} cm^{-3} . The blue plot is a repeat, for reference, of that shown in Fig. 4b, which had received the aggressive 900 s CdCl₂ treatment. The black plot was obtained when the front layer of undoped CdSeTe was thickened from 2.5 μm to 4 μm , and it received the same 900 s CdCl₂ treatment. The interaction between the as-deposited CdSeTe grain structure and the CdCl₂ treatment may account for the further increase in measured carrier concentration when the front CdSeTe layer thickness was increased. The green plot, showing a carrier concentration of roughly $7 \times 10^{16} \text{ holes/cm}^3$ was achieved with a 2.5 μm layer of undoped CdSeTe, but two CdCl₂ treatments were performed. The first CdCl₂ treatment was for 600s and was performed after deposition of the front CdSeTe layer. After the first CdCl₂ treatment, the sample was removed from vacuum and the excess CdCl₂ was rinsed before deposition of the CdSeTe:As layer. The second treatment—which was the 900s treatment used for the previous two samples — was performed after all absorber layers were deposited. We hypothesize that the first CdCl₂ treatment caused recrystallization and grain growth in the front CdSeTe layer, which potentially increased the rate of arsenic diffusion during the second CdCl₂ treatment. The aggressive CdCl₂ treatment may also play a role in the arsenic-activation process. All three “diffused” arsenic-doped curves can be compared to the orange curve — which is the “non-

diffused” arsenic sample shown in Fig. 2b—and the red curve—which is the CV profile of a copper-doped device with a carrier concentration in the low- 10^{14} cm^{-3} range typical of copper-doped CdSeTe/CdTe devices [37]. In these discussions, all reported doping levels are taken as the carrier concentration at zero bias, indicated by a diamond on the plots in Fig. 5.

4.2.3. Carrier lifetime

Fig. 6 shows the TRPL decay curves for copper-doped and arsenic-doped devices. While more complex simulations are needed to precisely determine excess-carrier lifetime, a common proxy is the decay constant from a fit of the slower decay [38]. The fit-determined lifetimes are 30 ns and 1.4 μs for the copper-doped and arsenic-doped samples, respectively. Both samples had similar structures, with a 100-nm thick MgZnO electron contact at the front and a 40 nm-thick tellurium hole contact layer followed by a carbon and nickel painted electrode at the back. The extreme difference in excess-carrier lifetimes make it difficult to visualize both decay curves on the same time scale, so, for the sake of clarity, the TRPL decay curve for the copper-doped sample has been inset in Fig. 6 on a different time scale. The lifetime measured on the arsenic-doped device—orders of magnitude longer than that of the copper-doped device—is comparable to the lifetimes achieved with CdSeTe double heterostructures sandwiched between aluminum oxide passivating layers [39,40]. This represents the longest excess-carrier lifetime reported thus far for any arsenic-doped sample. We attribute this result to the passivating effects of selenium at grain boundaries and interfaces as well as the potential field effect passivation due to the graded doping profile described earlier. This graded doping profile bends the valence and conduction bands upward towards the rear of the device, reducing the electron concentration at the back surface—which is known to be highly defective and, hence, prone to recombination [41–43].

4.2.4. External radiative efficiency

External radiative efficiency (ERE) measurements are a relatively recent development within the CdTe community to evaluate the potential of device structures to deliver voltage gains [32,44]. In a photovoltaic sample under illumination, the ERE is the ratio (between 0 and 1) of the number of photons reemitted through the illuminated surface to the number of incident photons. Thus, it is a measure of the number of recombination events that are radiative and non-radiative. Because non-radiative recombination events reduce the quasi-Fermi

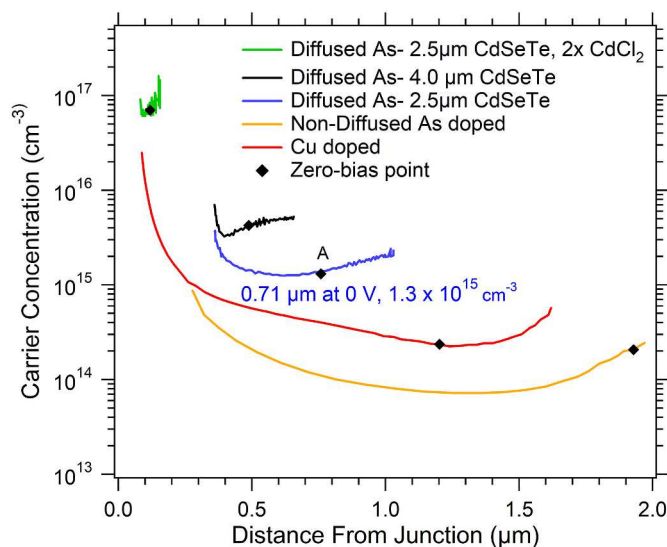


Fig. 5. CV profiles showing improved carrier concentration using arsenic doping through the “diffused” method. Three curves show the CV profiles for “diffused” structures, including a repeat of the curve shown in Fig. 4b with 2.5 μm of undoped CdSeTe at the front (blue), a structure where the undoped CdSeTe layer was increased to 4 μm (black), and a structure which received two CdCl₂ treatments (green). The CV profiles for a typical copper-doped CdSeTe/CdTe device (red) and the non-diffused arsenic doped sample (orange) from Fig. 2b are included for comparison. The diamond markers indicate the zero-bias point at which the carrier concentration was reported. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

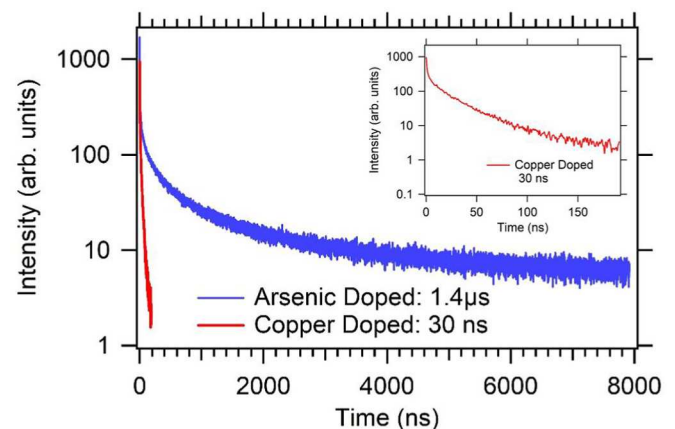


Fig. 6. Comparison of TRPL decay curves and fit excess-carrier lifetimes of copper-doped (red) and arsenic-doped (blue) devices. The copper-doped decay curve is reproduced in inset with a shorter timescale for better visualization. The copper- and arsenic-doped samples were fabricated using the structures shown in Fig. 1c and b, respectively. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

level splitting (QFLS), ERE measurements enable calculation of the maximum voltage that can be obtained from a given absorber—that is, in the presence of perfectly selective contact layers—also referred to as the implied or internal voltage iV_{OC} ($iV_{OC} = QFLS/q$, with q the elementary charge) [45]. iV_{OC} is calculated from ERE according to Equation (1) where $V_{OC,rad}$ is the radiative-recombination limited voltage, about 1150 mV in a CdSeTe absorber without sub-bandgap features [46]:

$$iV_{OC} = V_{OC,rad} - \frac{k_b T}{q} \ln(ERE) \quad (1)$$

Because the QFLS (or equivalently, the iV_{OC}) is improved by increasing the bulk minority-carrier lifetime, increasing the acceptor concentration, and decreasing grain-boundary and interface recombination, ERE measurements are a powerful tool to access these parameters and to quantify the impact that changing the fabrication process has on the potential open-circuit voltage of finished devices.

Fig. 7 shows the ERE results for cells with CdSeTe and CdSeTe/CdTe absorbers that were either undoped, arsenic-doped, or copper-doped. All cells included a front MgZnO electron contact layer and an evaporated Te back hole contact layer. The CdSeTe-only absorbers were 3–4 μm thick whereas the CdSeTe/CdTe bilayers consisted of 500 nm of CdSeTe followed by 3 μm of CdTe. The copper and arsenic-doped samples were doped as described in the methods section (post deposition CuCl treatment for copper-doping and “diffused” doping from a CdSeTe:As or CdTe:As layer for arsenic doping). The ERE data reveals several key findings. First, for all doping conditions, CdSeTe-only films exhibit significantly higher EREs than absorbers with a graded CdSeTe/CdTe bilayer. The passivating effect of selenium on CdTe grain boundaries has been described by Fiducia et al. [47], and this effect is apparent here. Second, the type of dopant directly affects the ERE. Undoped CdSeTe, in particular, exhibits remarkably high EREs, close to 1%. Arsenic doping reduces the ERE for both absorber structures, but not to the extent that copper doping does: compared with undoped samples, the addition of copper reduces the ERE by several orders of magnitude. Even though increasing the acceptor concentration is a viable method for increasing the iV_{OC} , it can be counteracted by a concurrent reduction in minority-carrier lifetime. Here, the reductions in ERE observed with doped samples suggest that the current doping methods also introduce non-negligible amounts of recombination-active defect states.

For copper-doped CdSeTe/CdTe, assuming a $V_{OC,rad}$ value of 1150 mV, the ERE reported in Fig. 7 translates into an iV_{OC} of approximately 880 mV. This means that current-generation CdSeTe/CdTe:Cu devices—with a V_{OC} of approximately 860 mV—are nearly passivation or material-quality limited, and will not produce a greater voltage unless the structure is amended to allow for higher QFLS. Alternatively, higher-ERE arsenic-doped CdSeTe samples, exhibit implied voltages of 900–950 mV. As shown in Equation (1), the exact implied voltage

depends on the $V_{OC,rad}$ term, which is affected by sub-bandgap absorption as will be discussed later. For this reason, the absorption band edge—reconstructed by either photoluminescence or external quantum efficiency—must be measured for each sample for which an iV_{OC} calculation is performed [32]. Additionally, it must be noted that even though the ERE values reported here seem small, they represent a significant improvement compared to historical values for CdTe, which have been calculated to be in the range of $10^{-4}\%$. An ERE of 0.008% has been calculated for the current record-efficiency CdTe device, and only a few photovoltaic technologies have demonstrated ERE values greater than one percent [48–50]. Our results support recent studies showing that, with proper processing and the addition of passivating layers, CdSeTe can exhibit ERE values approaching or even exceeding 1%, resulting in iV_{OC} close to 1 V [32]. These results contribute to the growing body of evidence that CdTe-based absorbers are now capable of supporting internal voltages significantly greater than the open-circuit voltages produced today. There should therefore be a renewed effort to develop passivated, carrier-selective contacts to allow for the extraction of the full voltage.

The incorporation of arsenic shows great potential to eliminate many of the most adverse effects of copper doping. As demonstrated above, arsenic-doped films simultaneously exhibit greater acceptor concentrations, vastly improved carrier lifetimes, and higher EREs compared to their copper-doped counterparts. However, obstacles remain to be overcome to maximize the iV_{OC} of arsenic-doped devices. Photoluminescence (PL) and external quantum efficiency (EQE) measurements, routinely reveal the presence of sub-bandgap features in arsenic-doped samples [51,52]. These features indicate that sub-bandgap absorption occurs, likely due to defect states or bandgap fluctuations. Such sub-bandgap absorption lowers the effective bandgap of the sample and, thus its $V_{OC,rad}$, ultimately limiting the iV_{OC} possible for any given value of ERE. Because the blackbody radiation at 300 K increases quasi-exponentially in the near infrared, $V_{OC,rad}$ is highly sensitive to sub-bandgap absorptance [53–55].

One such example of sub-bandgap features can be seen in the PL emission spectra given in Fig. 8a, between 900 and 1000 nm. Both samples were fabricated using the structure shown in Fig. 1c. The arsenic-doped sample did not receive a CuCl treatment and the CdSeTe layer was replaced with CdSeTe:As. In order to determine $V_{OC,rad}$ for these devices, absorptance was extracted as detailed by Onno et al. [32], by fitting the PL spectra at shorter wavelengths using Wurfel’s generalized Planck law [53]. The resulting absorption spectra are shown in Fig. 8b. For these samples, sub-bandgap features lead to an estimated 25 mV reduction in $V_{OC,rad}$ for the arsenic-doped sample compared to the copper-doped sample. Similar features were reported by Moseley et al. for VTD-grown CdSeTe:As samples [52]. Further investigation is needed to understand the cause of and full extent of these sub-bandgap features, as well as how different device structures or processing steps might mitigate them. Identifying, understanding and ultimately eliminating sub-bandgap absorption/emission will be an important step towards optimizing arsenic-doped structures.

5. Conclusion

In this work, we present an approach to achieve arsenic doping in CSS-deposited CdSeTe and CdSeTe/CdTe films, by diffusion of arsenic from an arsenic-containing “reservoir” layer at the back of the device to the bulk of the absorber, which is initially not intentionally doped. We provide evidence for the effectiveness of this technique, demonstrating acceptor concentrations greater than have been reported in copper-doped devices. Furthermore, we show that our arsenic-doped films exhibit minority-carrier lifetimes and radiative efficiencies at least an order of magnitude greater than can be achieved with copper doping. Microsecond lifetimes and ERE values near 1% enable implied voltages approaching 1 V, significantly higher than the current record V_{OC} . Achieving large implied voltages is foundational to improving the

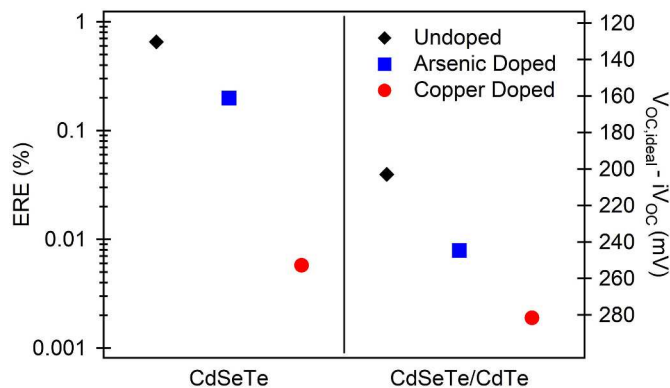


Fig. 7. ERE measurements for undoped, arsenic-doped and copper-doped CdSeTe only (left) and CdSeTe/CdTe bilayer (right) absorbers.

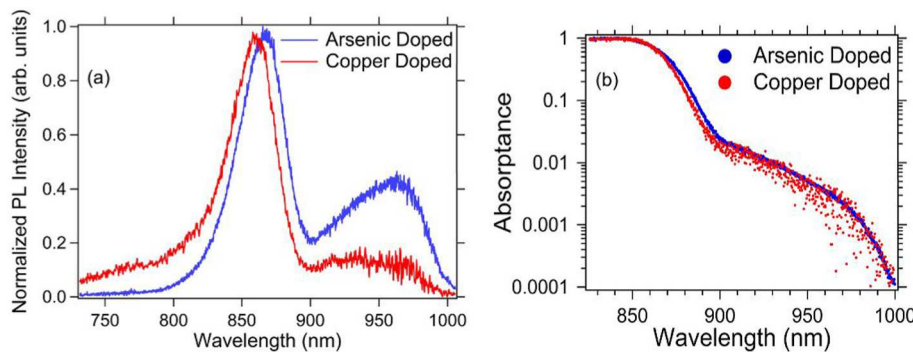


Fig. 8. (a) Photoluminescence emission spectra comparing sub bandgap features in copper (red) and arsenic (blue) doped samples. Both samples were fabricated using the structure shown in Fig. 1c. The arsenic-doped sample did not receive a CuCl treatment and the CdSeTe layer was replaced with CdSeTe:As. (b) Absorbances extracted by fitting the measured PL spectra shown in Fig. 8a. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

voltage of Cd(Se)Te solar cells. Therefore, structures such as the diffused-arsenic-doped samples presented here make excellent candidates for further study, in particular the development of carrier-selective contacts able to extract their full implied voltage, paving the way for improved external voltages.

CRediT authorship contribution statement

Adam Danielson: Writing – review & editing, Writing – original draft, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Carey Reich:** Writing – review & editing, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Ramesh Pandey:** Investigation. **Amit Munshi:** Resources, Investigation. **Arthur Onno:** Writing – review & editing, Visualization, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Will Weigand:** Investigation, Data curation. **Darius Kuciauskas:** Writing – review & editing, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Siming Li:** Investigation, Data curation. **Alexandra Bothwell:** Writing – review & editing, Visualization, Investigation, Data curation. **Jinglong Guo:** Visualization, Investigation. **Magesh Murugeson:** Resources. **John S. McCloy:** Writing – review & editing, Resources. **Robert Klie:** Visualization, Project administration, Funding acquisition, Data curation, Conceptualization. **Zachary C. Holman:** Supervision, Project administration, Methodology, Funding acquisition, Conceptualization. **Walajabad Sampath:** Writing – review & editing, Supervision, Resources, Project administration, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Adam Danielson reports equipment, drugs, or supplies was provided by 5NPlus. Adam Danielson reports equipment, drugs, or supplies was provided by Washington State University.

Data availability

Data will be made available on request.

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