A Review of Hybrid Supply Modulators in CMOS Technologies for Envelope Tracking PAs

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***Abstract*—This article reviews trends, architectures, and recent developments in CMOS-based supply modulators (SM) used for envelope-tracking power amplifiers (ET-PAs). This review details the most commonly used hybrid supply modulator (HSM) architecture in CMOS and discusses its performance requirements and design challenges. The importance of efficiency, speed, linearity, and output power in HSM design is delineated and different methods that focus on maximizing these performance parameters are presented. Finally, the design challenges of envelope tracking systems are discussed, and an overview of device technologies for implementing SM and ET-PAs is given.**

***Index Terms*—CMOS, envelope tracking (ET), long-term evolution, power amplifier (PA), radio frequency (RF), supply modulator (SM), wireless communication.**

I. Introduction

RECENT advancements in wireless communications have led to the use of spectrally efficient complex modulation schemes, such as quadrature amplitude modulation (QAM) and orthogonal frequency division multiplexing (OFDM), to achieve higher data rates within a limited spectrum. Channel bandwidths have also increased with each generation of wireless technology to support faster communication, as illustrated in Fig. 1. Unfortunately, wide channel bandwidths create signals with high peak to average power ratio (PAPR), as demonstrated in Fig. 2, for cellular handset communications [1]. The radio frequency (RF) transmitter's power amplifier (PA) is the most power-hungry block in the transceiver, as it can consume more than 60% of the total power in the entire transmitter chain [2], [3]. Therefore, to amplify signals with high PAPR levels, the PA needs to demonstrate high efficiency not only at peak power but also at power back-off levels (PBO). Standalone PAs are not highly efficient at PBO [4], thus motivating the need for advanced architectures and techniques to boost PBO efficiency [5], [6], [7], [8], [9], [10], [11].

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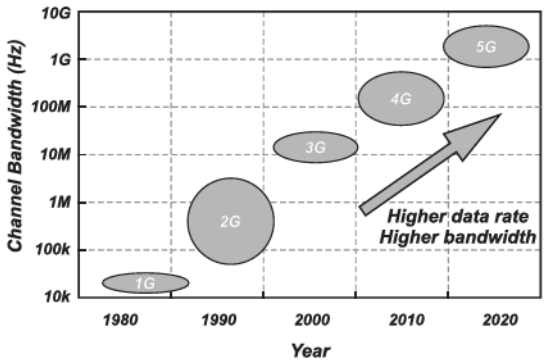

Fig. 1. Trend in channel bandwidth with evolving communications' standards.

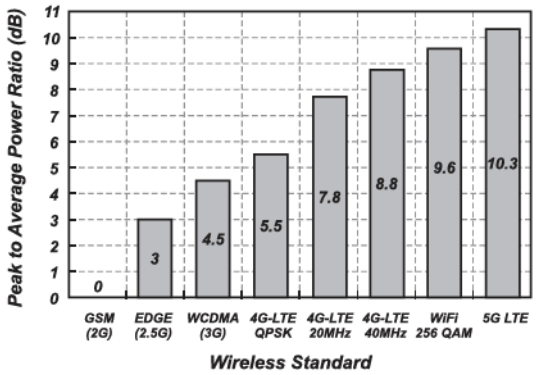

Fig. 2. PAPR trend in cellular handset communications.

Envelope tracking (ET) is a popular technique to improve the efficiency of a RF PA at PBO levels. In this technique, the PAs drain bias is modulated as a function of the RF input signal's time-varying envelope to minimize the dc power dissipation within the PA. This forces the PA to always operate near its compression point, where it usually demonstrates highest efficiency. Fig. 3(a) and (b) shows a PA using a conventional fixed supply and a modulated supply, respectively. The reduction in PA energy dissipation is conceptualized in Fig. 3(c) and (d) by illustrating that the modulated supply reduces the overhead dc power consumption. The ET technique leads to efficiency enhancement at PBO levels, as the supply modulates with power level (envelope) and, therefore, shifts the PAs efficiency curve with PA output power, as illustrated in Fig. 4.

ET systems have high integration capability within cellular handset devices, and therefore, the demand for ET integrated

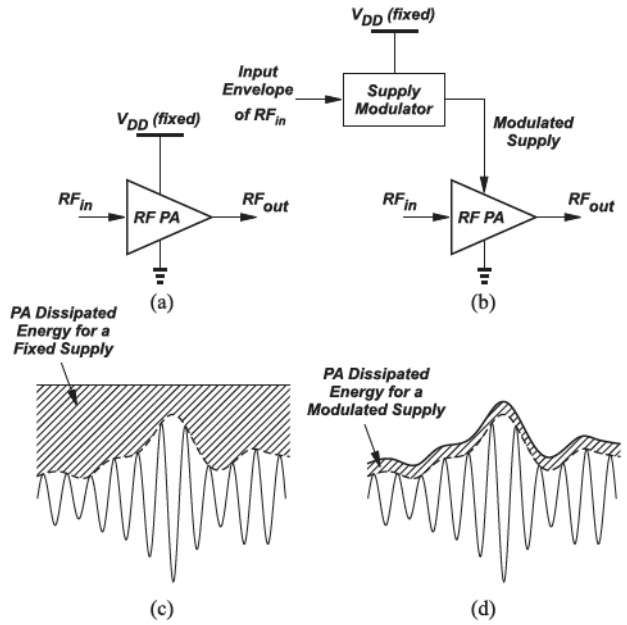

Fig. 3. Conventional RF PA (a) with fixed and (b) with modulated supply, and PA energy dissipation (c) with fixed supply and (d) with modulated supply.

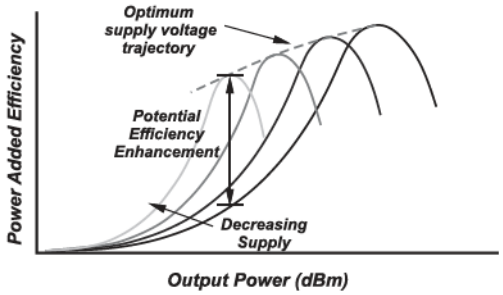

Fig. 4. PA power added efficiency versus output power showing efficiency enhancement at PBO levels with a modulated supply in an ET-PA system.

circuits (ICs) to support the smartphone market continues to rapidly grow (see Fig. 5) [12]. Fig. 5 demonstrates that the importance of ET has increased over the years and continues to do so as the wireless communication market moves closer to the fifth-generation (5G) era. ET can also be used in conjunction with other efficiency enhancement structures, such as Doherty or load modulation techniques [13], [14], switched mode [15], and outphasing [16], to further improve ET-PA performance.

In an ET system, the supply modulator (SM) acts as the power management unit for the PA. Therefore, in order to successfully realize an ET-PA, the SM must satisfy the continuously increasing performance demands of evolving wireless transmit hardware. Over the years, considerable development and research efforts in industry and academia have been spent on maximizing SM performance, and a majority of the most recently developed modulators use a hybrid SM (HSM) topology implemented in various CMOS technologies and mainly targeted for handset applications.

In light of the recent technology trends in ET-PAs and the importance of SM performance on the overall ET-PA system

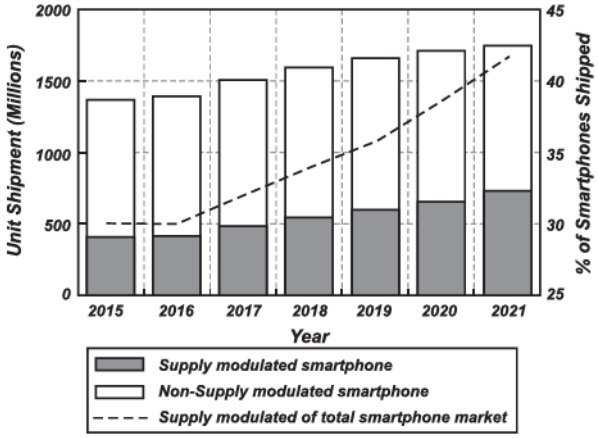

Fig. 5. Number of ET-ICs deployed over the years (and projections) [12].

performance, this article gives a comprehensive review that also categorizes and explains the various HSM developments implemented in CMOS to-date. The rest of this article is organized as follows. It begins with a discussion of the performance requirements on SM design and covers the various SM topologies in Section II. Section III explains the operation of the most widely adopted HSM topology and summarizes its performance parameters. Various proposed techniques/architectures to optimize the performance of HSMs are delineated in Sections IV–VII. Section VIII summarizes the available device technologies for HSM and PA implementations and discusses challenges of an ET-PA system. Finally, Section IX concludes this article.

II. SM for ET

SMs for ET-PA systems have three main performance requirements: efficiency, speed, and linearity (ripple). To adequately achieve these performance requirements for continuously evolving wireless standards, various SM topologies have been proposed and are discussed in the following sections.

A. SM Design Requirements

First, an SM needs to demonstrate high efficiency in order to maximize the overall efficiency of an ET-PA system ($\eta_{\text{ET-PA}}$), which can be expressed as follows:

$$\eta_{\text{ET-PA}} = \eta_{\text{SM}} \times \eta_{\text{PA}} \tag{1}$$

where η_{SM} and η_{PA} represent the individual efficiencies of the SM and PA, respectively. As can be seen from (1), the overall ET-PA system efficiency is limited by the SM efficiency, thus motivating the need for high-efficiency SMs.

Second, an SM needs to demonstrate high speed in order to track fast input envelopes. The term speed for an SM is expressed in terms of both bandwidth and slew rate (SR) (covered in Section V). It should be noted that the envelope of a modulated RF signal has a much higher bandwidth than the bandwidth of the actual RF signal itself. As explained in [17], the envelope signal's power is distributed from dc to the envelope signal's higher order harmonics. In order to process most of the envelope signals and

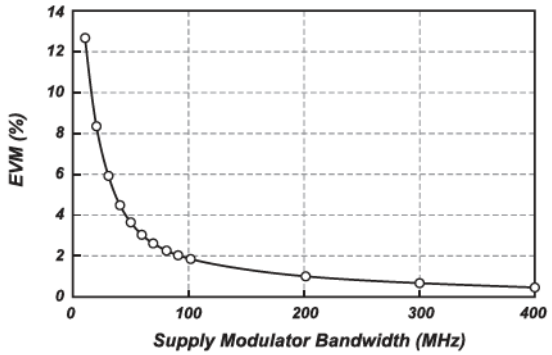

Fig. 6. Simulated EVM versus SM bandwidth for a WLAN IEEE 802.11g OFDM signal [17].

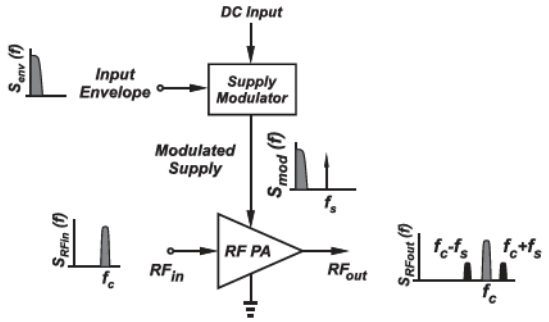

Fig. 7. Frequency spectrum at different locations in an ET-PA system.

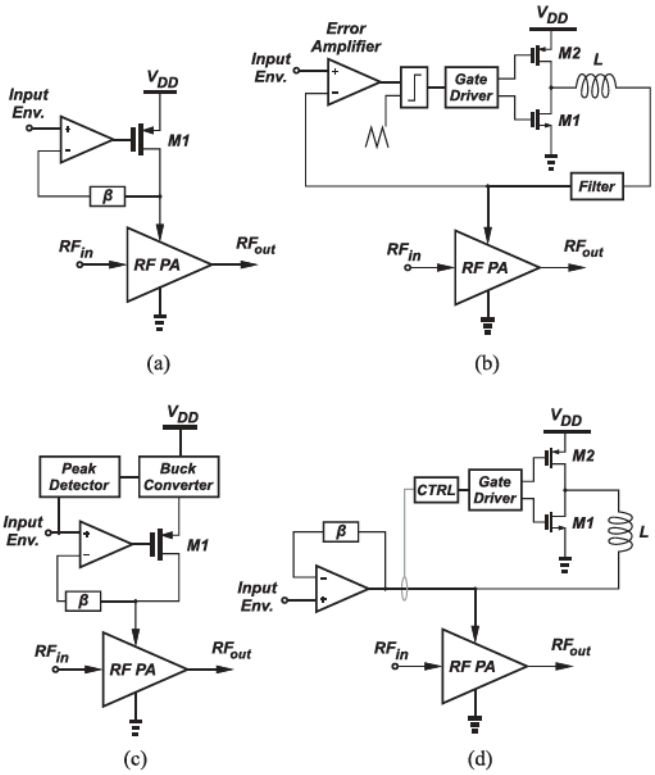

Fig. 8. Different SM topologies. (a) Linear. (b) Switching. (c) Series. (d) Hybrid [20].

avoid significant distortion at the output, the SM is required to have much higher bandwidth (usually around 4–5 times) than the RF input signal's bandwidth. To demonstrate the importance of SM bandwidth on RF signal quality, Fig. 6 shows the effect of SM bandwidth on the RF signal's error vector magnitude (EVM) when tracking a WLAN envelope signal of 20 MHz bandwidth.

Finally, an SM needs to demonstrate low ripple at the output in order to achieve high linearity. At the SMs output, the processed input envelope signal is replicated along with an additional ripple that can be represented by a frequency f_s. As shown in Fig. 7, there is a mixing effect [18] that upconverters have the ripple around the fundamental carrier frequency (f_c) at the sidebands $f_c \pm f_s$, with a separation entirely dependent on the ripple frequency. Although the linearity of an ET-PA system is mainly dictated by the PA, the effect of ripple on the SM output can be observed in the PAs output spectrum [19]. If the input RF signal is $S_{\text{in}} = v_{\text{in}}\cos(2\pi f_c t)$ and the ripple from the SM is $S_{\text{ripple}} = v_s\cos(2\pi f_s t)$, then the amplitude ($v_{\text{out}}$) of the supply ripple at the sidebands is given by the following:

$$v_{\text{out}}(v_{\text{in}}, v_{\text{ripple}}) = \sum_{i,j=0}^{\infty} a_{i,j} v_{\text{in}}^{i} v_{\text{ripple}}^{j} \tag{2}$$

where $a_{i,j}$ are the gain terms as a function of the ith order of the input voltage and the jth order of the voltage ripple. The first-order ripple induced sidebands (at $f_c \pm f_s$) around the RF carrier (at f_c), which is

$$v_{\text{out}}(f_c \pm f_s) = \frac{1}{2} a_{11} v_{\text{in}} v_{\text{ripple}} \tag{3}$$

where v_{in} and v_{ripple} are the amplitude of the signals at f_c and f_s, respectively, and a_{11} represents the first-order intermodulation product between the RF signal and SM ripple. From (3), the PAs output linearity is directly affected by the SMs output ripple (v_{ripple}).

B. SM Topologies

There are four main SM topologies [20], namely linear, switching, series, and hybrid, as illustrated in Fig. 8. All topologies are optimized for the main specifications of efficiency, speed, and linearity (ripple). Most recent advancements in SM are direct implementations, variations, or extensions of these four basic topologies.

In the first topology of Fig. 8(a), the SM is implemented with a linear regulator. A linear topology can achieve high bandwidth and high linearity, but a main drawback is poor efficiency at low power levels. The efficiency of a linear regulator is directly proportional to its output voltage [21], so the efficiency drops rapidly as the output voltage level decreases. Since existing (and future) communication standards depict high PAPR levels, this linear topology is not effective because the PA operates mostly in the PBO region.

The second SM topology of Fig. 8(b) uses a switching regulator. This topology provides higher efficiency than the linear

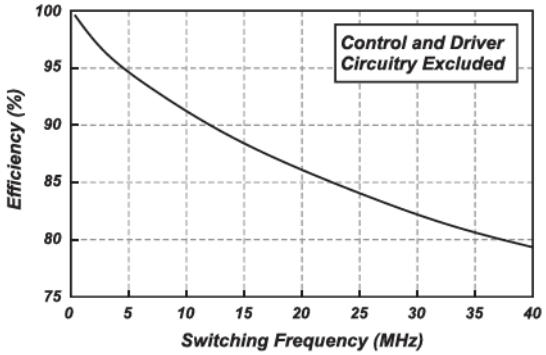

Fig. 9. Case study illustrating idealized switching regulator efficiency versus switching frequency.

regulator for a wider range of voltage levels, as this efficiency can reach above 90% depending upon frequency and load current [22]. But the disadvantage is that the switching function produces high ripple content at the output, which degrades the SM linearity. Filtering this ripple through the use of a high-order filter is one option, but filtering reduces the maximum achievable bandwidth and would not be suitable for wideband applications. Another option is to increase the regulator's switching speed, but the switching losses increase with the frequency [23] and efficiency degrades. In order to demonstrate the increase in switching loss with switching frequency, a mostly ideal switching regulator (with control/driver circuitry excluded) was designed in a TSMC 65 nm CMOS process. This case study uses the TSMC device [field-effect transistor (FET)] models, but all drivers and output passive circuitry are ideal. Although the exact value of switching loss depends upon the sizing of transistors and quality factor of passives, the general behavior of efficiency with respect to switching frequency is demonstrated in Fig. 9 and shows efficiency decay with increasing frequency.

The third SM topology of Fig. 8(c) uses a series connection of linear and switching regulators [24]. This is mainly used to enhance the efficiency of the linear regulator and maintain good SM linearity, as the linear regulator exhibits low output ripple and provides power supply rejection that attenuates the ripple from the switching regulator. While this topology has higher efficiency than the standalone linear regulator of Fig. 8(a), the main drawbacks of this topology are high switching losses for wideband applications, conduction loss due to the presence of a pass device in the load current path, degradation of the linear regulator's power supply rejection, and, most importantly, the required additional overhead to operate the series switching regulator. The added overhead makes this architecture difficult to realize in most CMOS process technologies.

The fourth SM topology of Fig. 8(d) uses a parallel combination of linear amplifier (LA) and switching amplifier (SA). This topology is popularly known as an HSM, and it is currently the most prevalent and widely used SM topology. The LA is responsible for wide bandwidth operation and high linearity due to ripple compensation, while the SA provides high efficiency current to the load. This topology is discussed in detail in Section III.

TABLE I
PERFORMANCE COMPARISON OF SM TOPOLOGIES

SM topology	Efficiency	Speed (Bandwidth)	Linearity
Linear	Low	High	High
Switching	High	Low	Low
Series	Moderate	Low	Moderate
Hybrid	High	Moderate	High

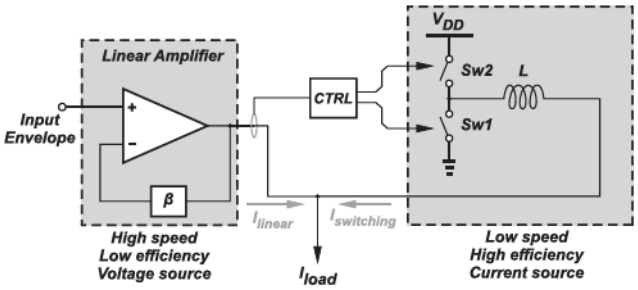

Fig. 10. HSM architecture.

Table I provides a qualitative performance comparison amongst the four different SM topologies.

III. HYBRID SM

The HSM architecture [17], [25], [26], [27], [28], [29] emerges as a promising solution to the efficiency, speed, and linearity tradeoffs observed in different SM topologies. The working principle of the HSM and different loop control methods involved in HSM design are explained in detail in the following sections.

A. Description of HSM Operation

A typical HSM design consists of two amplifiers working simultaneously, as shown in Fig. 10. The left side of Fig. 10 is a voltage-control/LA, which is responsible for regulating the output voltage to the input envelope voltage via feedback. The right side of the HSM in Fig. 10 is a current-control/SA, which is responsible for providing high-efficiency inductor current to the load. The majority of the low-frequency load current is provided by the SA, while the wideband LA supplies the remainder of the higher frequency current. The ripple on the switching current is compensated by the LA to provide a highly linear power supply to the load (i.e., PA).

Depending upon the input signal's envelope bandwidth, the transition frequency (F_{tr}) of an HSM [31], defined as the frequency where the current provided by the SA and LA is equally split, is chosen based on an efficiency and linearity tradeoff. Fig. 11(a) and (b) illustrates the frequency response of SA and LA currents for low and high values of F_{tr} with a fixed input envelope power spectral density (PSD). If F_{tr} is chosen too small, the low-efficiency LA supplies the majority of the current to the load, which degrades the efficiency of the HSM. If F_{tr} is chosen too large, the SA must switch at higher speed with higher switching loss and generates more current ripple that can result in linearity degradation.

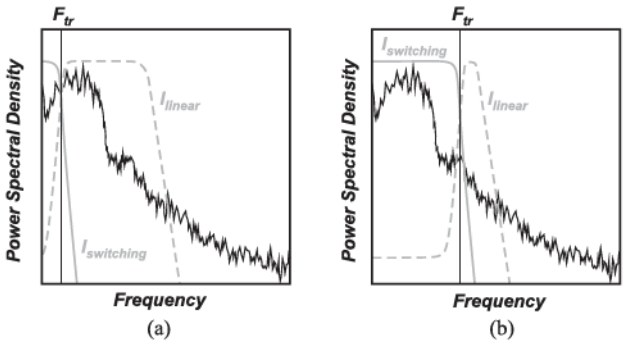

Fig. 11. HSM with (a) low and (b) high transition frequency (F_{tr}) [31].

The basic operation of an HSM is demonstrated through the example plots of Fig. 12, which are generated via simulation of an HSM using verilog-A models of the LA and SA. In this example, the LA is modeled with a dc gain of 60 dB and 3 dB bandwidth of 50 kHz and the SA has an output inductor of 1 μH. The HSMs load is modeled as 5 Ω || 10 pF to emulate a PAs drain impedance. For this case study, an input sinusoidal signal is provided to the circuit to generate 200 mA of dc current with 100 mA of ac swing. The frequency of the input signal is varied, and the current waveforms I_{linear}, $I_{\text{switching}}$, and I_{load} are observed in Fig. 12.

When the input signal is a dc input, as shown in Fig. 12(a), the SA provides the average current to the load with switching ripple caused by the SAs switching operation. The ripple is compensated by the LA to generate a constant load current. For a low-frequency 100 kHz input signal, as shown in Fig. 12(b), the SA current moves with the input signal because the SA generates the average current and the ripple cancelation is provided by the LA. As the signal frequency is increased to 1 MHz in Fig. 12(c), the SA begins to slew due to its limited bandwidth. The load current still follows the input signal, but the magnitude of the LA current increases where the SA cannot provide current during the fast signal transitions (high frequency). Finally, at a high input signal frequency of 10 MHz in Fig. 12(d), the SA ramps up slowly and cannot adequately follow the input signal. The low-efficiency LA provides a significant amount of the load current, thus degrading HSM efficiency.

B. Loop Control Methods

There are two main methods to generate the SAs control signal (CTRL shown in Fig. 10) and regulate the switching loop. The first method is known as pulsewidth modulation (PWM) control and is illustrated in Fig. 13(a) [25], [26], [27]. In this method, the LA current (I_{linear}) is converted to a voltage, using an I-to-V converter, that drives the compensator $A(s)$. The output of the compensator is compared with a synchronization waveform, which can be a ramp or a triangular signal, to modulate the duty cycle of the switching loop to adjust the SA current ($I_{\text{switching}}$). In PWM control, the switching loop bandwidth is limited to a fraction of its switching frequency, thus leading to a slower loop response.

The second method, as shown in Fig. 13(b), is known as hysteretic control [17], [28], [29]. In a hysteretic controller, a fraction of I_{linear} current is first converted to a voltage (V_{sense}) typically by using a sense resistor (R_{sense}). The value of V_{sense} is then compared with two threshold voltage values set by the designer using a hysteretic comparator, and the output of this comparison controls the switching loop to adjust the SA current ($I_{\text{switching}}$). Since hysteretic control uses a window comparator instead of a clocked comparator as in PWM control, the loop response of the hysteretic control is faster, which means wider SA bandwidth. A hysteresis loop is also inherently stable across a wide load range and does not require compensation circuitry, which leads to simpler loop design compared with PWM control.

In PWM control, the switching frequency is independent of the input signal and remains constant. But in the case of hysteretic control, the switching frequency varies with the magnitude of the input signal [30]. The expression for its average switching frequency (f_{sw}) is given by

$$f_{\text{sw}} = \frac{R_{\text{sense}} V_{\text{out}} (V_{DD} - V_{\text{out}})}{2 V_{DD} N L V_{\text{hys}}} \tag{4}$$

where V_{DD}, V_{out}, V_{hys}, R_{sense}, N, and L are the supply voltage, the output voltage, the hysteresis window of the comparator, the sense resistor, the current sensing ratio, and the inductor value, respectively. The highest switching frequency ($f_{\text{sw\_max}}$) is reached when the output voltage equals $V_{DD}/2$ and this maximum frequency can be expressed as follows:

$$f_{\text{sw\_max}} = \frac{R_{\text{sense}} V_{DD}}{8 N L V_{\text{hys}}}. \tag{5}$$

It can be seen from (4) and (5) that the f_{sw} depends on two important factors, the hysteresis window and the output inductor value. Therefore, the value of V_{hys} and L should be optimized for highest achievable HSM efficiency, speed, and linearity. Furthermore, the hysteresis can be implemented in both voltage and current mode, which is generally not the case in PWM control. Since hysteretic control provides several advantages compared with PWM control as outlined above, hysteretic controllers are used in the majority of present-day HSMs.

HSMs must be continuously advanced to follow the continuously more demanding requirements of wireless communication standards. HSMs must track wideband/fast-changing signals in present and future communications. Obtaining adequate output power from an HSM has also become a significant challenge in recent years due to battery voltage variation over time and aggressive scaling in CMOS process technologies. Various techniques and architectures have been proposed to optimize the performance of HSMs in terms of efficiency, speed, linearity, and output power. For the purposes of this review, and in order to organize the various architectures and differentiate them from one another, these techniques have been categorized in the diagram of Fig. 14. Various methods and architectures are organized into these categories based on their primary performance parameters for improvement, but it is important to note that most of these works improve multiple performance parameters, such as both output power and efficiency. Sections IV–VII provide more details on these different techniques.

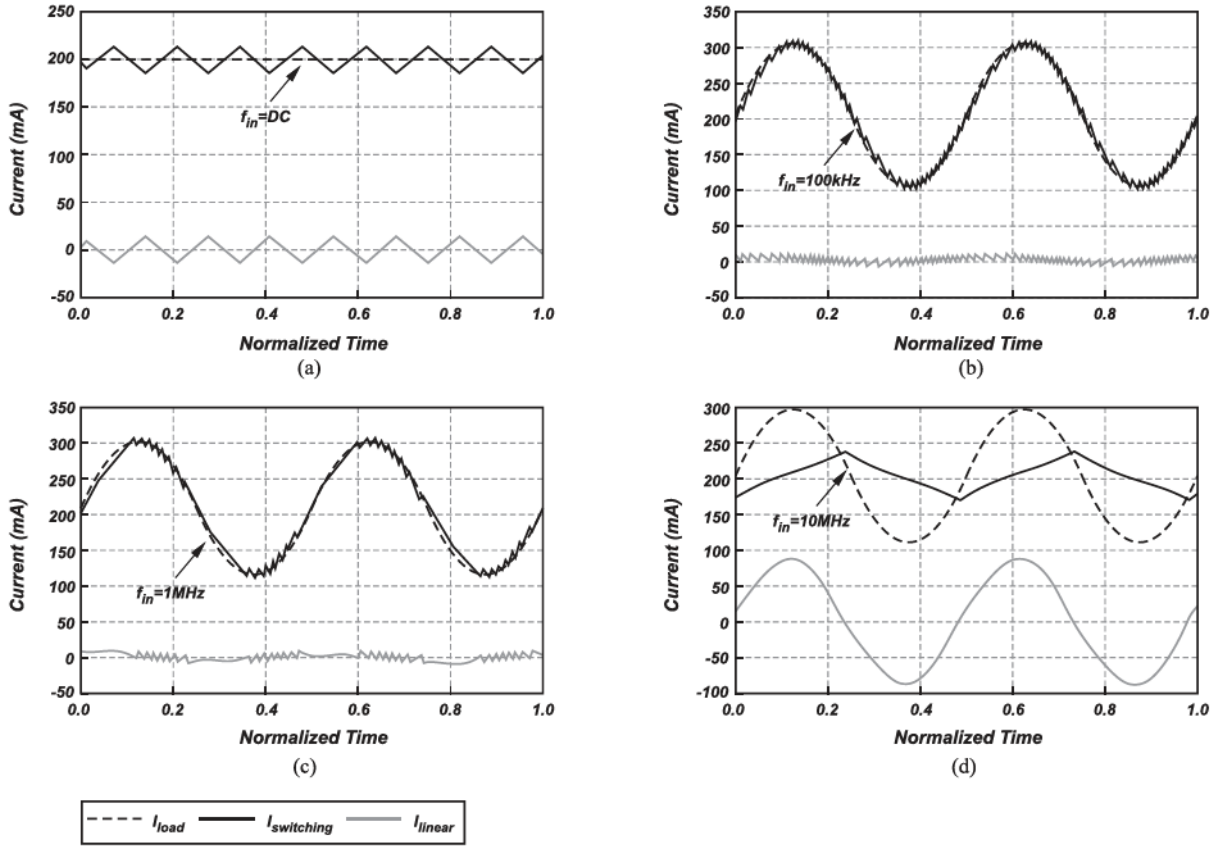

Fig. 12. Linear (I_{linear}), switching ($I_{\text{switching}}$), and load (I_{load}) current waveforms for (a) DC, (b) 100 kHz, (c) 1 MHz, and (d) 10 MHz input signals.

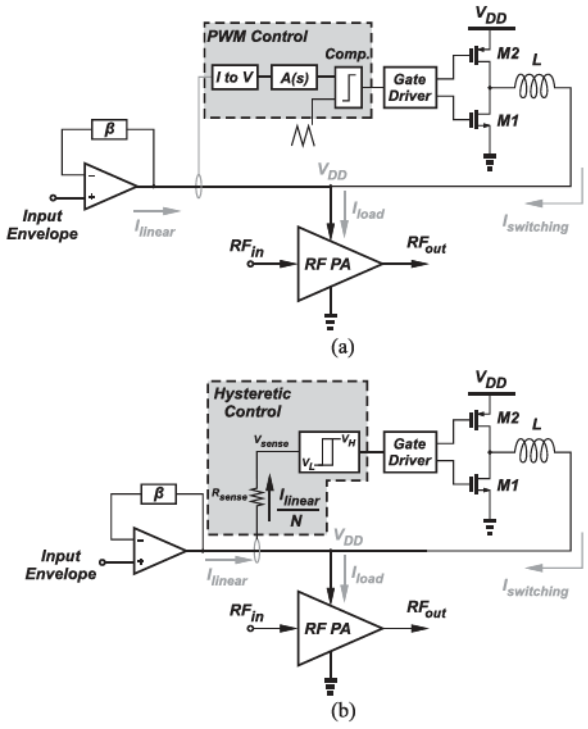

Fig. 13. Loop control methods in an HSM design. (a) PWM mode. (b) Hysteretic mode.

IV. Efficiency Improvements in HSM

An HSM needs to demonstrate high efficiency to maximize the overall ET-PA system efficiency [from (1)]. Since the PA operates mostly in its PBO region, it is desirable for the HSM to maintain high efficiency at both peak and back-off power levels. In the following sections, this work presents a brief analysis of the loss mechanisms contributed by different components in an HSM and reviews the proposed efficiency enhancement techniques.

A. HSM Peak Efficiency Improvement

In order to maximize peak efficiency of an HSM, it is important to acknowledge the HSMs different sources of loss and minimize them using improved design techniques.

1) Analysis of Loss: Many different sources, such as the linear and SAs, controller block, off-chip inductor, and board parasitics, contribute to the overall static and dynamic losses in an HSM. A simplified model of the HSM for loss analysis is shown in Fig. 15. The majority of the losses in an HSM are contributed by the LA and the SA [32]. Therefore, most optimization efforts focus on minimizing the losses in these circuit blocks.

The LA loss is mainly dominated by the voltage drop of the class-AB output stage ($V_{\text{drop}} \times I_{\text{linear}}$), where the voltage drop V_{drop} depends upon the output voltage [32], [33]. Apart from this,

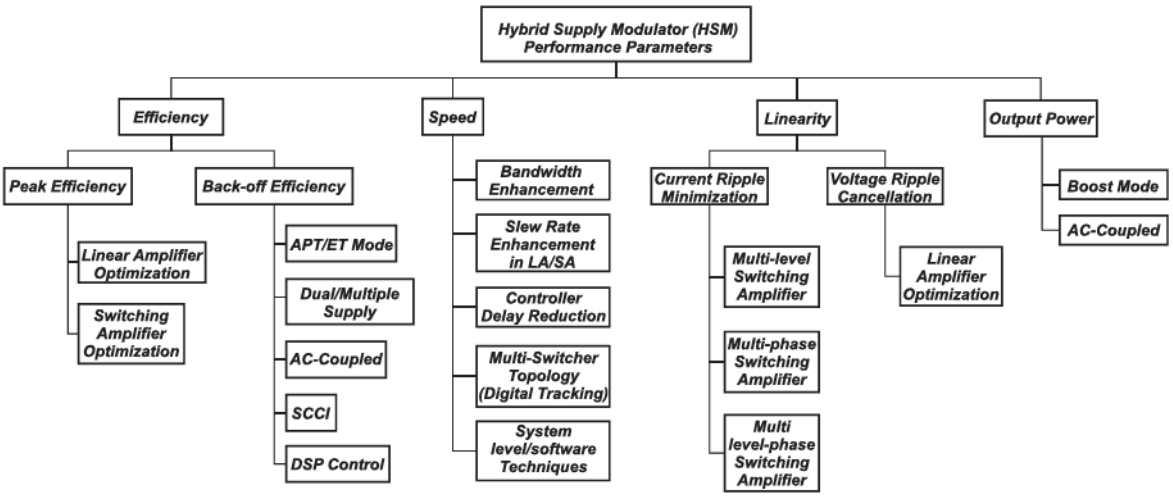

Fig. 14. Various methods for optimizing HSM performance.

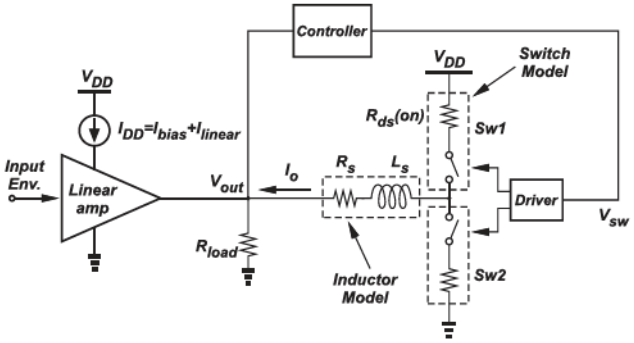

Fig. 15. Simplified model of the HSM for loss analysis.

the biasing circuitry of the amplifier and the quiescent current in the LA output stage (e.g. class-AB stage) contribute to the static dc loss ($P_{\text{LA\_bias}}$). Hence, the total loss in the LA (P_{LA}) can be expressed as the sum of $P_{\text{LA\_classAB}}$ and $P_{\text{LA\_bias}}$.

The loss mechanisms in an SA (P_{SA}) include, but are not limited to switching losses (gate drive loss, diode-recovery loss, etc.), conduction losses due to the ON-resistance of the switches and dc resistance of the inductor and capacitor losses due to finite equivalent series resistance. The SA losses are dependent upon several design parameters, such as switching frequency, load current, and duty cycle, and a detailed breakdown of the different losses with their expressions can be found in [34].

The loss mechanism in the HSMs controller block is static dc power dissipation and can be expressed as P_{Ctrl}, whose magnitude depends upon the type of control used (hysteretic or PWM control). The HSMs extra sources of loss (P_{ext}) consists of nonideal effects caused due to packaging, board routing, board parasitics, etc. It should be noted that the losses described so far are broadly analyzed in the existing works, such as the article presented in [35], and are highly dependent upon implementation and system specifications.

If V_{out} is the output voltage across a load resistor R_{load}, then the power obtained at the output of an HSM is P_{out} and the expression for its efficiency (η_{HSM}) is given by

$$P_{\text{out}} = \frac{V_{\text{out}}^2}{R_{\text{load}}} \tag{6}$$

$$\eta_{\text{HSM}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{LA}} + P_{\text{SA}} + P_{\text{Ctrl}} + P_{\text{ext}}} \times 100. \tag{7}$$

Different circuit techniques and methods to reduce the HSM loss (dominated by LA and SA) are discussed in the following sections.

2) Reducing LA Loss: The LAs output devices are generally of large size to drive a large amount of transient current I_{linear} to compensate for the switching ripple. Hence, there is a need for design techniques that reduce the amount of I_{linear} to reduce $P_{\text{LA\_classAB}}$ and also static dc loss, $P_{\text{LA\_bias}}$, in the LA.

In order to reduce LA static power dissipation $P_{\text{LA\_bias}}$, class-AB devices can be biased more toward a class-B configuration. But a class-B output stage generates more crossover distortion and reduces the current providing capability of the LA. Therefore, adaptive biasing for the class-AB devices can be employed to save dc power in which the bias is shifted between class-AB and class-B depending upon the output current requirements [36]. Additionally, LA designs are sensitive to process, voltage, and temperature variations that can change the class-AB quiescent current significantly (by more than 300%). Therefore, circuit-level techniques, such as accurate current quiescent control and supply voltage and temperature insensitive quiescent current control, can be used to control the variation of class-AB current and avoid wasting $P_{\text{LA\_bias}}$ [37], [38].

In order to reduce conduction loss $P_{\text{LA\_classAB}}$, the LAs output current I_{linear} needs to be reduced. For low-frequency operation, I_{linear} equals the ripple current from the SA [from Fig. 12(b)]. So, the value of I_{linear} can be reduced by adopting improved SA designs, such as multilevel or multiphase [39] architectures, that generate lower switching current ripple. These architectures are detailed in Section VI. For high-frequency input signals, I_{linear} increases because the SA cannot provide the entire load current

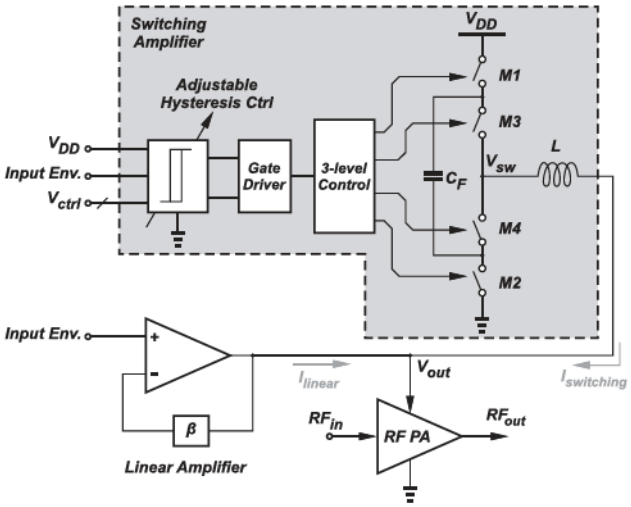

Fig. 16. HSM design with a three-level SA implementation [41].

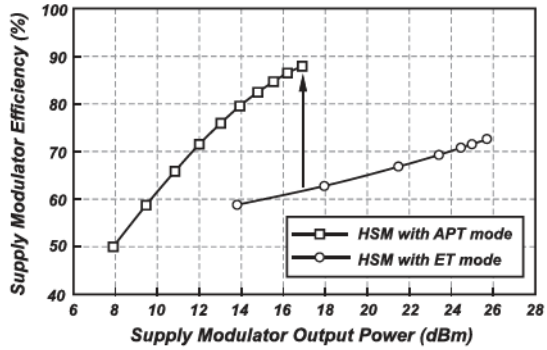

Fig. 17. Efficiency of the dual-mode HSM (with APT and ET modes) for a 16-QAM LTE input signal [45].

[from Fig. 12(d)]. The SAs switching frequency can be increased to reduce I_{linear}, but the tradeoff is increased to reduce SA loss, as discussed in Section IV-A3.

3) Reducing SA Loss: In an SA design, the magnitude of the SAs average output current (I_o) is determined by the PAs load requirement, which, in turn, determines the SA device size and, therefore, conduction losses. The SAs driver and power stage devices are typically sized at the optimum crossover point between conduction loss and switching loss. The SA power loss can be decreased by two methods. In the first method, the switching frequency f_{sw} of an HSM can be lowered, but this leads to a slower response from the SA and is not effective for tracking wideband signals, as was previously illustrated in Fig. 12(c). In the second method, advanced topologies for the SA are implemented to reduce various losses, which can improve the HSM efficiency.

Abdulslam et al. [40] show that the conduction loss due to the inductor peak-to-peak current ripple is proportional to the voltage swing at the switching node. For an input voltage of V_{DD}, the voltage swing at the switching node is V_{DD} (for two-level SA), $V_{DD}/2$ (for three-level SA), $V_{DD}/4$ (for five-level SA), and so on. So, in the case where conduction losses are dominant over other SA losses, moving to a multilevel SA topology can lead to the reduction of conduction losses and boosting of efficiency. Another work in [41] explains that the multilevel SA topology allows stacking of multiple shorter channel length devices, as shown in Fig. 16. Hence, due to reduced parasitics, the switching losses in high-frequency SAs can be reduced [42], and better efficiency can be achieved while tracking wide bandwidth signals. Furthermore, Parisi [43] shows that if the load current requirements are high (in the case of a high-power PA), then the SA may benefit from a multiphase topology because the conduction losses become a significant factor for high load current. In cases, where load current changes significantly, digital controllers can be further employed to improve efficiency by adaptively changing the number of phases based on the magnitude of the load current [44].

In addition to peak HSM efficiency, the HSMs efficiency at back-off power levels is also important because the ET-PA and, hence, HSM operate at back-off power during the majority of the transmit time to process high PAPR signals.

B. HSM Back-Off Efficiency Improvement

At backed-off input signal levels, the HSMs required load current is low and the static power dissipation $P_{\text{LA\_bias}}$ in the LA becomes a dominant factor of loss. Due to this, the HSM demonstrates poor efficiency in the PBO region. There are various architectures proposed in the literature to improve the back-off efficiency of an HSM by eliminating or reducing $P_{\text{LA\_bias}}$ at PBO. The efficacy of each architecture is explained in the following sections.

1) Dual-Mode [Average Power Tracking (APT)/ET] HSM: A dual-mode architecture improves the PBO efficiency of an HSM by avoiding the use of an LA in the back-off region when the RF PAs input power is also low. For peak average output power, the HSM operates using both the LA and SA. But for output power levels lower than some threshold that is set based on the system design requirements, the HSM is reconfigured to work as a standalone SA using an additional lower bandwidth SA. This SA demonstrates significantly higher efficiency than the combination of both LA and SA because the high biasing current of the LA is eliminated and the standalone SA is optimized for lower power levels. The standalone SA must have a lower output filter bandwidth (i.e., higher inductor value) than the SA+LA combination to attenuate switching ripple that is normally canceled by the LA. Therefore, the standalone SA cannot track as wide of an input signal bandwidth as the combined SA+LA HSM. This dual-mode modulator, therefore, supports ET in high-power mode and APT of PAs at PBO.

Ham et al. [45] adopt a dual-mode HSM architecture and the measured results are shown in Fig. 17. The results demonstrate that the efficiency of the HSM at 9 dB PBO was boosted up from 60% in ET mode (using the HSM with combined SA+LA) to approximately 87% in APT mode using the standalone SA. However, the tradeoff of this architecture is that it requires an additional standalone SA with additional circuit-level components, such as a comparator, switching driver, power devices,

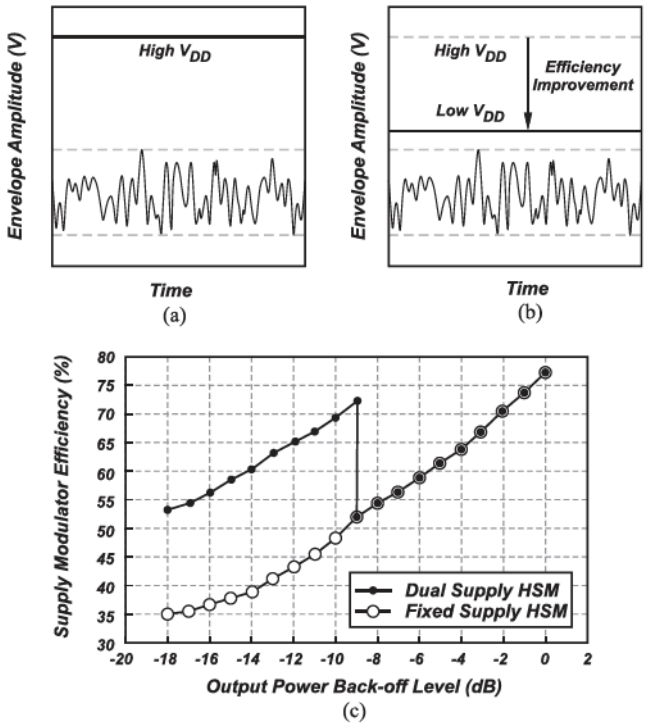

Fig. 18. (a) Fixed-supply and (b) dual-supply voltage at the lower power levels. (c) Efficiency of conventional (fixed-supply) and dual-supply HSM [46].

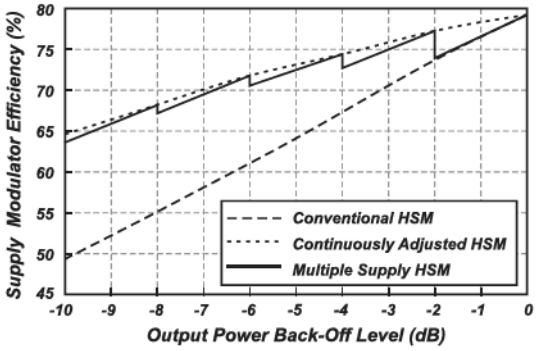

Fig. 19. Efficiency of the conventional and multiple-supply HSM [47].

control switches, and off-chip inductor, which leads to extra die-area/board space.

2) Dual/Multiple-Supply HSM: The static power loss in the LA remains constant irrespective of the input envelope power level for a fixed LA supply voltage. It can be seen from Fig. 18(a) that in the PBO region when the envelope power level is low and V_{DD} is high, there is a wastage of dc power. But when the V_{DD} is reduced for lower power signals, dc power can be saved and efficiency is enhanced, as illustrated in Fig. 18(b). Therefore, the LAs supply voltage can be varied with the HSMs input signal level to reduce LA static losses, $P_{\text{LA\_bias}}$. Kim et al. [46] propose a dual-supply HSM architecture in which the V_{DD} of the LA is set to 5 V in high-power mode and reduced to 2.5 V in low-power mode (or back-off). The measured results of the dual-supply HSM are recaptured in Fig. 18(c) and demonstrate about 20% improvement in efficiency at 9 dB PBO when compared with an HSM using a single fixed-supply LA. The disadvantage of this architecture is that it requires two LAs working individually for low- and high-power modes, with extra control switches that add die/board area and circuitry.

The dual-supply architecture provides only two supply voltage levels. But, this structure can be further expanded to change the LAs supply voltage to multiple levels based on the tracking of the HSMs input envelope. Adding more levels increases the complexity of design and there is a minimum supply voltage required to provide sufficient headroom for proper operation of the LAs transistors. Ham et al. [47] propose a multiple-supply HSM architecture that adjusts the dc supply of the LA adaptively with the average power of the envelope signal. As the bias state of the class-AB output stage determines the distortion in the LA, the class-AB is tied to a separate supply. As shown in Fig. 19, the efficiency of the multiple-supply HSM is improved from 49.5% to 63.6% at 10 dB PBO. However, this architecture requires additional components, such as a low-pass filter, for the envelope detection and a voltage–current converter. Moreover, the LAs adaptive supply needs to be realized using finite bandwidth SMs (e.g., an HSM), which was not implemented in work [47].

3) AC-Coupled HSM: An alternative method that enables a reduced LA supply voltage is an ac-coupled architecture. Most of the conventional HSM architectures are dc coupled, i.e., the LA and the SA are directly connected to the HSM output (or PA load). But in ac-coupled designs, the output of the LA is isolated from the HSM output using an ac-coupling capacitor, as shown in Fig. 41, and the supply voltage of the LA does not need to be as high as the peak envelope voltage [48]. Instead, the supply voltage just needs to provide the ac signal swing plus the LAs device headroom. By using a smaller V_{DD} for the LA, the value of $P_{\text{LA\_bias}}$ is reduced and the PBO efficiency is improved. The detailed operation of the ac-coupled architecture is covered in Section VII.

4) Single-Capacitor Current-Integration (SCCI) HSM: In an HSM design, the LA is designed to provide only the compensating ripple created by the SA, ideally making its average current zero (excluding $P_{\text{LA\_bias}}$). Typically, an SA can be more than 90% efficient [22] and an LA is around a maximum efficiency of 50% due to its class-AB output stage biasing. Therefore, it is desirable to have most of the HSMs load current provided by the SA in order to maximize the efficiency. The LA provides ripple compensation with maximum and minimum current ripple values of I_H and I_L, as labeled in Fig. 12(a). For the realistic case when $I_L = 0$ or $I_L \neq -I_H$, the average value of current ripple is a finite value. But for the ideal case when $I_L = -I_H$, the average value of the current ripple is zero and there is no flow of LA current to the load in the steady state.

Tan and Ki [49] introduce an SCCI HSM architecture, as shown in Fig. 20. This architecture forces the average output current from the LA to be around zero, hence reducing the LAs average output current and improving HSM efficiency. In the SCCI design, a scaled version of the LA output current (I_{ab}) is used to modulate charge on the capacitor C_c to generate a control voltage V_c. This V_c is compared with a reference voltage

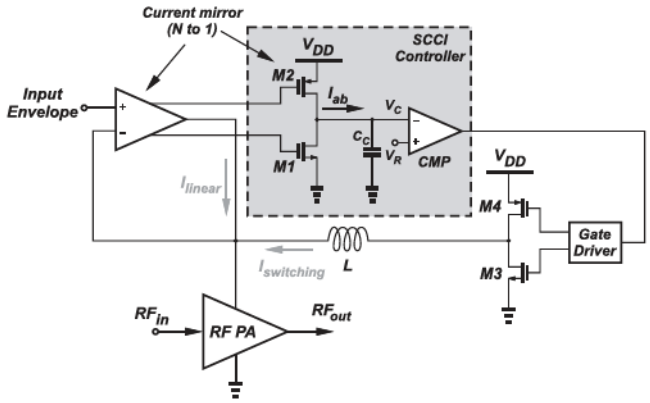

Fig. 20. SCCI HSM architecture [49].

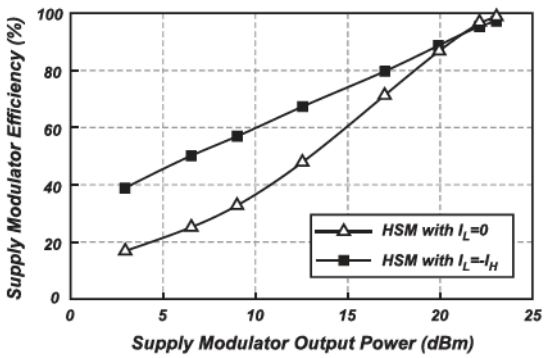

Fig. 21. HSM efficiency with $I_L = 0$ and with SCCI HSM $I_L = -I_H$ [49].

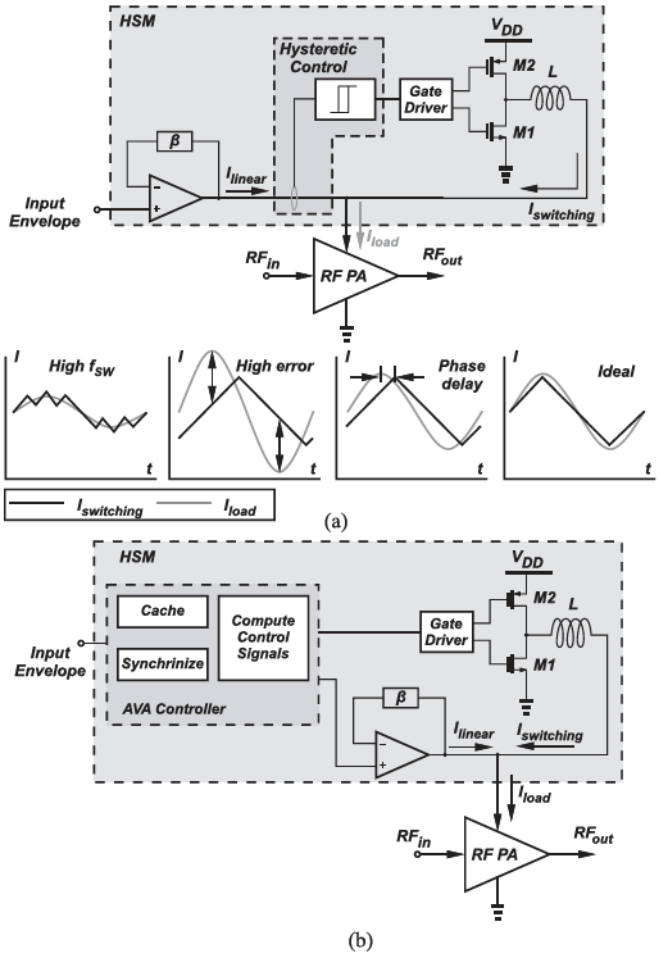

Fig. 22. (a) Conventional hysteretic control-based HSM. Current waveforms for different SA SRs are summarized into three cases (case-1 to case-3). Case-4 shows the relatively ideal condition, but it is very hard to be realized by hysteretic control strategy. (b) Proposed AVA-based HSM that aims to realize case-4 [50].

(V_R) to regulate the switching loop. After each switching cycle, the voltage level of V_c returns to the same value, which forces the net charge accumulated on C_c during each cycle to zero. As a result, the average value of I_{ab} and the average output current from the LA are also approximately zero. It can be seen from Fig. 21 that the efficiency of an HSM that uses $I_L = 0$ is improved by approximately 20% at 10 dB PBO when using an SCCI architecture with $I_L = -I_H$ instead [49].

More efficiency enhancement is observed in the PBO region, as the LAs average current (along with $P_{\text{LA\_bias}}$) becomes more dominant with the reduction of signal power. The tradeoff of this architecture is the addition of an extra capacitor (C_c) in the main switching path, which can slow down the loop response, thus reducing HSM speed, and the SCCI HSM can face stability challenges.

5) Optimizing Losses Through DSP Control: Conventionally, most of the HSM designs use analog-based hysteresis comparison for the controller block. The controller detects the direction of LA current by using a current/voltage sensing circuit. Once the LA sources or sinks large current, the controller regulates the charging state of the SA. The hysteresis controller is sensitive to the SR difference between the SA output current ($I_{\text{switching}}$) and the desired load current (I_{load}). Fig. 22(a) categorizes the current waveforms of HSM into three cases according to the current SRs of the SA (e.g., case-1, case-2, and case-3). In case-1 and case-2, the SR difference between $I_{\text{switching}}$ and I_{load} is large, which results in high switching frequency of the SA and high tracking error, respectively. Due to the high switching losses, the efficiency of the HSM decreases and due to mismatch in tracking, more I_{linear} current goes to the load, which is again detrimental to the HSM efficiency. But if the SRs of $I_{\text{switching}}$ and I_{load} are close, the SA can provide more high-efficient current without increasing switching frequency, as shown in case-3. However, case-3 is very hard to maintain due to the irregular variations of the RF envelope. Also, the loop delay of the hysteresis controller (also the SA driver stage) makes the phase of $I_{\text{switching}}$ always lag behind that of I_{load}, which prevents the HSM from reaching the relatively ideal (or desirable) state of case-4.

Chen et al. [50] propose an open-loop digitally controlled HSM as good alternative to closed-loop hysteresis-based HSM designs to improve efficiency while tracking wide bandwidth envelopes. Open-loop control does not suffer from the inherent lag of closed-loop control. Also, the digital processor can realize more flexible control methods. In the work, using the existing processors, such as field-programmable gate array or digital signal processing (DSP), an extended efficiency model is put

forward to systematically analyze the energy loss of an HSM from the aspect of current loss. The relationship between the SA output and RF signal envelope is analyzed by a short-time Fourier transform method. Thus, an average voltage alignment (AVA) algorithm is proposed to overcome the limitations of the closed-loop controller. The AVA controller caches the signals in discrete segments, which is conducive to system-level SA control. The control method reduces power loss in the HSM by ignoring the phase limitation and small waveform fluctuations. In addition, a digital low-pass filter is applied to shape the input of the AVA, which helps to control the SAs switching frequency while tracking different envelope bandwidths. The measurement results for the proposed technique show the tracking bandwidth from 10 MHz up to 200 MHz. The HSM achieves an efficiency improvement of 20% under a maximum PAPR condition of ∼9 dB with a maximum switching frequency of 10 MHz compared with the conventional hysteresis comparison controller block.

Leng et al. [51] uses a Viterbi-like Trellis search (TS) DSP algorithm to find the optimal switching sequence for the SA in the HSM, thus lowering rms error current in the LA and minimizing SA switching frequency. Using the proposed TS search for 20 MHz ET, the measurement results show that the average LA current drops by 27% and TS improves efficiency of the HSM by 3% (from 71.2% to 74.2%) at 6 dB back-off, when compared with a conventional hysteresis comparison controller block. Furthermore, Chen et al. [52] demonstrate an open-loop digitally control HSM with just an SA (without an LA). The SA controller implements envelope shaping and transient filtering processes to reduce the envelope bandwidth and corresponding SA switching frequency.

Since the controller algorithm can be implemented in a baseband modem, the proposed techniques of digitally optimizing the HSM losses show promise for tracking wideband envelopes with improved DSP and machine-learning algorithms.

V. Speed Improvements in HSM

Increasing communication data rates requires the use of wideband envelopes. Therefore, HSM designs are continuously increasing in speed to track the increasing envelope signal bandwidths. In order to track high-frequency (fast varying) envelopes, the speed of the transistors in an HSM should be maximized. As there is a trend toward the CMOS scaling, the transition frequency (f_T) of a transistor can be increased by using shorter channel length processes, but this is not always beneficial to the overall ET-PA system or within the designer's control. Therefore, this section discusses the various architectures that have been proposed to maximize HSM speed.

A. LA Bandwidth Enhancement

The term bandwidth is a small signal phenomenon (calculated around a dc operating point) and signifies how fast an amplifier can track a signal. As discussed in Section II, the input envelope consists of fundamental and multiple harmonics, which requires bandwidth of the LA (BW_{lin}) to be higher than that of the envelope (BW_{in}). In order to demonstrate the effect of LA bandwidth

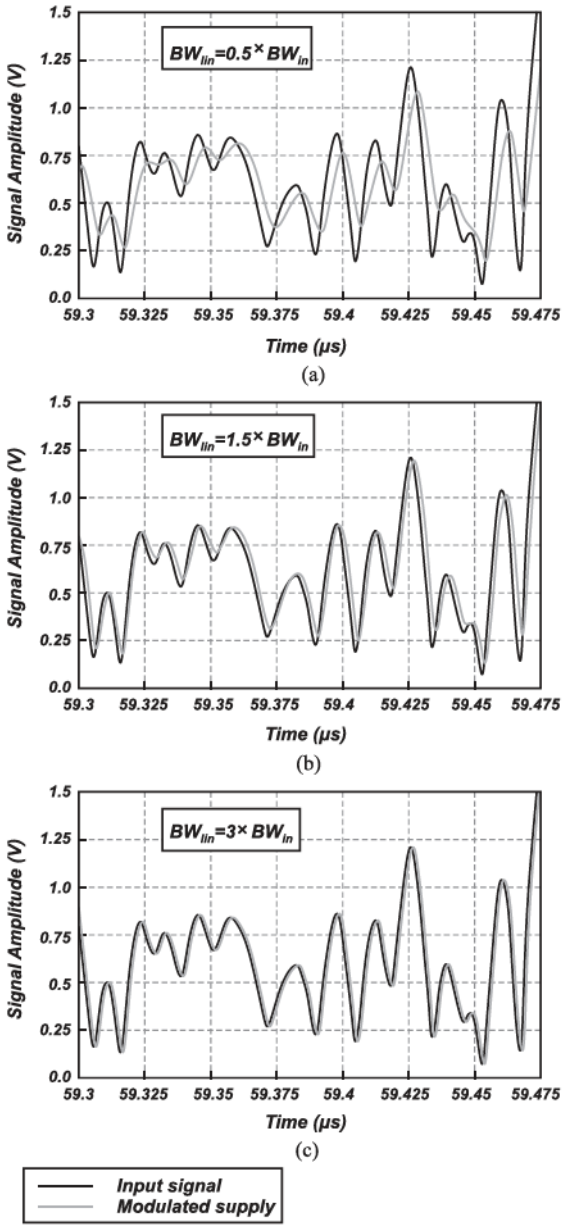

Fig. 23. Transient waveforms to show tracking of an LTE 100 MHz envelope for LA bandwidth of (a) 0.5× (b) 1.5× (c) 3× the signal bandwidth.

on tracking performance of a modulated signal, a simulation setup with a test LTE signal of 100 MHz bandwidth is chosen for a case study. The LAs tracking performance for different bandwidths is observed from Fig. 23(a)–(c). The simulation results show that the LA needs to demonstrate BW_{lin} of at least three times the BW_{in} to track an envelope signal with high accuracy. Although high accuracy or minimal tracking error is desired to maximize ET-PA efficiency, the value of BW_{lin} also depends upon the linearity requirements for the HSM.

The LA is typically used in a closed-loop configuration (in Fig. 10); therefore, research efforts have been made to improve its open-loop unity gain bandwidth (UGB). This is because the 3-dB bandwidth of the LAs closed loop is equal to the UGB of the open-loop LA (assuming a single-pole system). The UGB

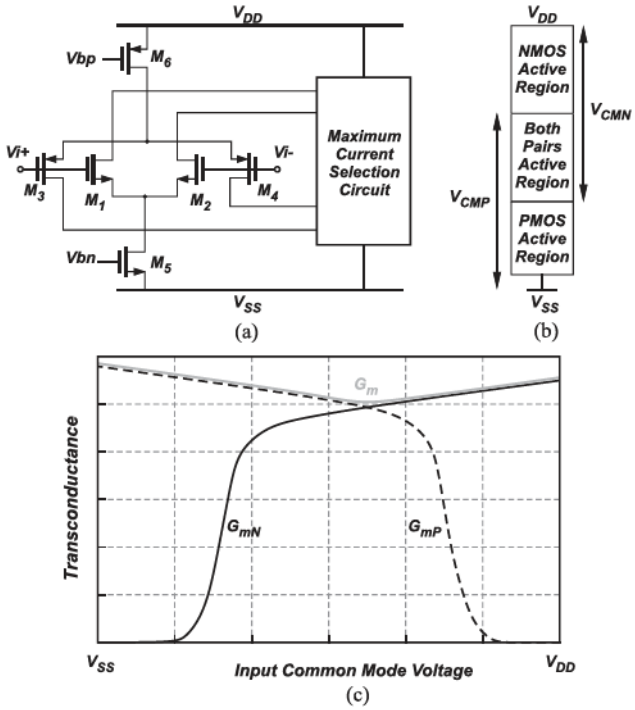

Fig. 24. (a) Maximum-current selection circuit. (b) Active region of both p-type metal-oxide-semiconductor (PMOS) and n-type metal-oxide-semiconductor (NMOS). (c) Effective G_m value (almost constant) [41].

of an LA depends upon the transconductance (G_m) of the input devices and the load capacitor (C_L), as follows:

$$\text{UGB} = \frac{G_m}{2\pi C_L}. \tag{8}$$

As the value of C_L is generally decided by the PA load, the magnitude of G_m [from (8)] should be increased in order to achieve a higher UGB. Different methods [53], [54], [55], [56] are proposed in the literature to boost the value of G_m, such as G_m boosting, cross-coupled structure employing positive feedback, current recycling structure, and dual-path crossover current-reuse mechanism. In case of a multipole system, the nondominant poles can be pushed to higher frequencies (by consuming more current) or zeroes can be inserted (pole–zero cancelation [64]) in order to increase the UGB value.

As the input signal envelope spans multiple dc operating points, it is important for the LA to maintain a high bandwidth over the entire dc operating range. Usually, an LA is designed with both PMOS and NMOS input pair in order to process the entire envelope range (from supply rail to ground). Since both PMOS and NMOS input pairs show different transconductance values depending upon the operating point, the total value of the G_m does not remain constant, and hence, the LAs UGB varies significantly [from (8)]. Therefore, there have been different techniques proposed in the literature to force the G_m of the LA to remain almost constant over signal swing [57]. Mahmoudidaryan et al. [41] adopt one of these constant G_m techniques by using a maximum-current selection circuit, as shown in Fig. 24(a). This circuit always selects the maximum of

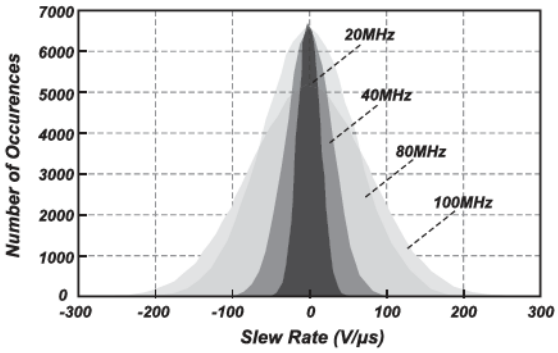

Fig. 25. SR trend for different bandwidths of an LTE signal.

the PMOS or NMOS currents at any given dc operating point. As the maximum-current value remains almost constant, this technique helps in reducing the variation in the overall G_m (dependent on current), as demonstrated in Fig. 24(b) and (c), and therefore achieves constant UGB over the entire envelope.

B. LA Slew-Rate Enhancement (SRE)

The term SR for an LA is a large signal phenomenon (covers multiple dc operating points) that signifies how fast an amplifier can track transient changes [58]. It is an important attribute of LA speed, as the envelope signal is usually a transient waveform whose value changes over time. Fig. 25 shows the trend of SR for different modulation bandwidths of an LTE signal, illustrating that the SR requirements go up with higher modulation bandwidth. In an LA, the expression for the SR is given by

$$\text{SR} = \frac{2I_{\text{Tail}}}{C_L} \tag{9}$$

where I_{Tail} is the tail current of the input stage, and C_L is the load capacitor. In order to increase the SR, the value of I_{Tail} should be increased. But it is important to note that the increase in I_{Tail} value should happen only in the case of transient change and not at dc in order to avoid an increase in $P_{\text{LA\_bias}}$ and prevent efficiency degradation.

To improve the SR in an LA, the most popular technique is addition of an auxiliary SRE circuit in parallel with the main LA. The SRE circuit consists of a large signal detector (LSD) to detect a transient change and additional mechanism to increase the value of I_{Tail}. The SRE does not affect nominal operation of the LA and does not significantly add to the $P_{\text{LA\_bias}}$. In conventional LA designs, the SRE circuit is added in parallel to the input stage to change the value of tail current, as shown in Fig. 26(a). But this requires a large amount of current (from another branch/circuit) to increase I_{Tail} and there is a delay (due to multiple stages in the LA) to see the increased current effect from input to the output.

To avoid additional circuitry for providing current (to increase I_{Tail}) and reduce input to output delay, a better alternative is to add the SRE circuit at the gate of the output class-AB stage, as shown in Fig. 26(b). The SRE circuit senses the voltage difference between the inputs during transients through the LSD and adjusts the bias of the class-AB pair adaptively. As the

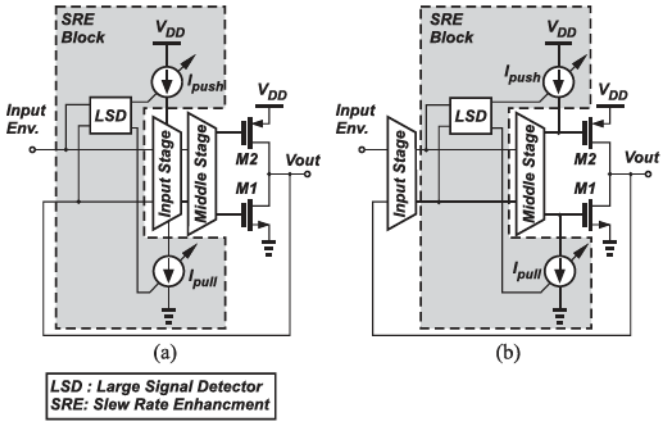

Fig. 26. SRE circuit added at (a) input stage and (b) output class-AB stage [59].

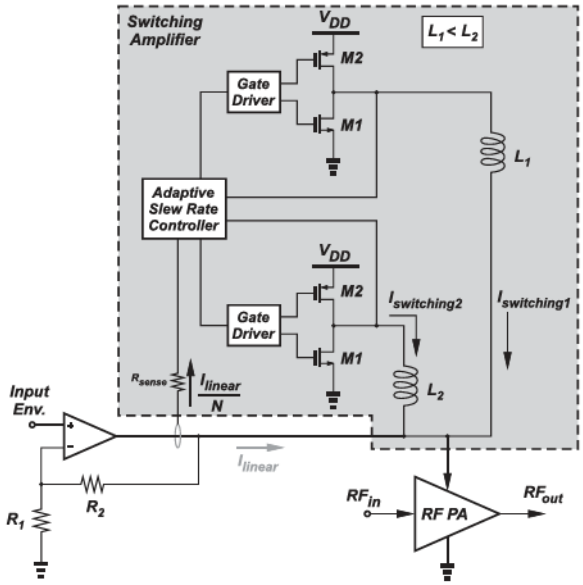

Fig. 27. SRE using dual-switch HSM architecture [61].

class-AB transistors demonstrate a high value of transconductance, they can respond to the input gate voltage change faster by sourcing/sinking the required amount of current to cancel the SAs current ripple. Mahmoudidaryan et al. [59] implement an LA with a SR that is enhanced from 178 to 325 $\mathrm{V}/\mu\mathrm{s}$ and from -169 to -307 $\mathrm{V}/\mu\mathrm{s}$ after adding the SRE circuit. Jing and Bakkaloglu [60] report the enhancement in the positive and negative SR of their designed LA by 86.8% and 75.3%, respectively.

C. SA SR Enhancement

The SR in an SA is determined by the slope of the load current, which depends on the value of the off-chip inductor. Typically, an SA uses a single inductor in an HSM, whose value is selected based on the SA design requirements for bandwidth and ripple. Therefore, the SA is SR limited and cannot provide the current instantaneously to track the fast transient changes. To overcome this challenge, multiple SAs (with different inductor values) can be used, and the SR can be varied based upon the input envelope transients using an additional control knob. Kim et al. [61] introduce a dual-switch HSM architecture, as given in Fig. 27, which uses an LA, two SAs (fast and slow) with inductors L_1, L_2, respectively, and $L_1 < L_2$, and an adaptive SR controller. The current in the LA is monitored using four different controller switch states and both SA currents ($I_{\text{switching1}}$ and $I_{\text{switching2}}$) are adaptively changed, which improves the SA SR and enables faster tracking. The dual-switch architecture can be expanded to multiswitch architectures with the tradeoff of adding multiple SAs and extra die-area/board space.

SRE using fast and slow SAs can also be implemented, as Amo et al. [62] implement a topology where the low-frequency portion of the output power is provided by a standalone slow buck–boost SA and the high-frequency portion of the output power is provided by a multilevel SA. The slow buck–boost SA uses an inductance L_{slow} of 4.7 μH and operates from 1.9 to 7 MHz (2 MHz typical), while the fast multilevel SA uses an inductance L_{fast} of 22 nH and its switching frequency can reach up to 140 MHz (80 MHz typical). Another extension of the SA SRE concept is implemented in [63], where a fast SA and a slow SA are implemented in the same design for tracking a 5G new radio (NR) envelope signal of bandwidth of 40 MHz. The slow SA is implemented using a PWM control and a larger inductor is used (as compared with the fast SA) to provide 60% of the total power to the load. The fast SA is implemented using hysteretic control and two smaller inductors are used in a multiphase configuration to provide the remaining 40% of the total power to the load. The fast SA inductors are sized to ensure that the HSM bandwidth is higher than the tracking signal's bandwidth and to provide correct phasing between the two inductor current paths.

D. Combined LA Bandwidth and SA SRE

As discussed in Section V-A and C, there are different circuit-level techniques in the literature to make speed improvements in an HSM: increase LA bandwidth and increase SA SR. In order to track high-bandwidth envelopes for sub-6 GHz 5G NR applications, a balanced combination of these two techniques is used. Paek et al. [64] propose an HSM to track 100 MHz envelope bandwidths in which a dual-supply buck and an ac amplifier operate jointly to provide the modulated supply voltage to the RF PA, as illustrated in Fig. 28. The ac amplifier supports three operating modes according to the signal bandwidth and communications standard: First, for low bandwidth, a feedforward fast-switching (FFFS) buck converter is used; second, for medium bandwidth, the FFFS buck converter assisted by an LA is used; and third, for large bandwidth, a voltage-buffer-compensated (VBC) class-AB LA is used. The technique for enhancing bandwidth using a VBC class-AB LA and enhancing SR using a fast-switching SA is explained in the work of Paek et al. [64].

A similar implementation can also be found in [65] that proposes an HSM to track 130 MHz of envelope bandwidth. In the ET operation, there are four modes according to the required bandwidth and output power: low bandwidth and low power; low bandwidth and high power; high bandwidth and low power;

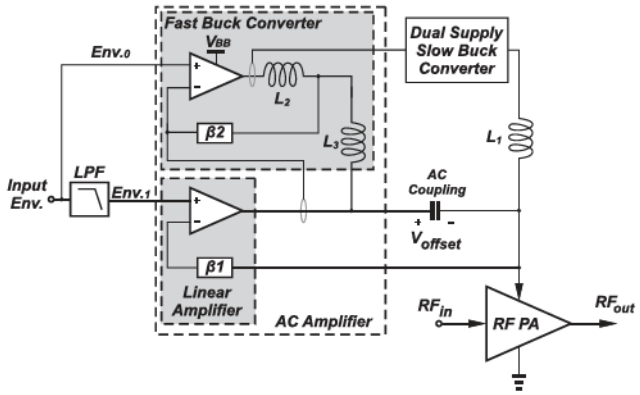

Fig. 28. Simplified version of the HSM architecture in [64] with LA bandwidth and SA SRE.

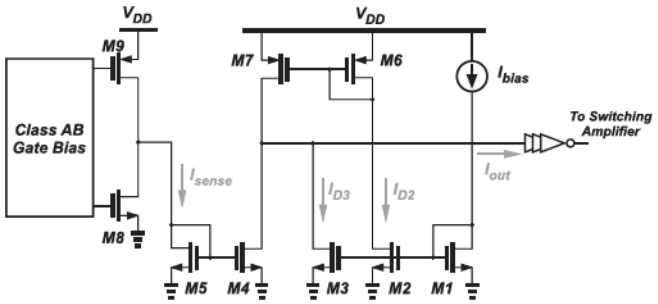

Fig. 29. Simplified version of the delay-based hysteretic controller [37].

and high bandwidth and high power. Depending upon the bandwidth, different circuitry are activated. The operational details for these modes are found in [65]. All of the above-mentioned high-speed tracking techniques come at the cost of increased design complexity and extra die-area/board space.

E. Reducing Controller Delay

Most recent works in improving HSM speed focus on improving the speed of both LA and SA. But little attention has been paid to the controller block, which contributes to a finite propagation delay. For narrowband applications (e.g., low-bandwidth signals, such as EDGE and CDMA envelopes) whose HSM switching frequency is low, the effect of controller delay can be neglected because the switching period is much longer than the delay. But for wideband applications (e.g., high-bandwidth signals, such as LTE and 5G-NR envelopes), the switching period becomes comparable with the controller delay. Due to this significant delay, the SA cannot respond quickly to fast signal transitions, which results in increased current flow from the LA (low efficiency) to the load [from Fig. 12(d)]. This leads to HSM performance degradation in terms of efficiency and output power.

As explained in Section III-B, an HSM works by either PWM or hysteretic control. In PWM control, the switching loop bandwidth is limited to a fraction of its switching frequency. But in the case of hysteretic control, the switching loop bandwidth can be as high as the switching frequency. Therefore, most of the existing HSM designs use hysteretic control to achieve faster loop response that is suitable for tracking wideband envelopes. For a hysteretic controller with upper (I_U) and lower (I_L) current limit and hysteresis threshold currents ($\pm I_T$), the more accurate controller limits, (I'_U) and (I'_L), that include the intrinsic controller delay (t_D) can be expressed as follows [37]:

$$I'_U = +I_T + \left(\frac{V_{DD} - V_{\text{out}}}{L_o}\right) \times t_D \tag{10a}$$

$$I'_L = -I_T + \left(\frac{0 - V_{\text{out}}}{L_o}\right) \times t_D \tag{10b}$$

$$I_{\text{HYS}} = I'_U - I'_L = 2I_T + \left(\frac{V_{DD}}{L_o}\right) \times t_D \tag{11}$$

where V_{out}, L_o, and I_{HYS} are the output voltage, external inductor, and hysteresis window, respectively. The comparison time in the controller, which is dictated by the value of I_{HYS}, leads to a finite delay between the LA and the SA. Therefore, various works in the literature focus on reducing the magnitude of I_{HYS}. As can be seen from (11), there are mainly two ways to reduce the delay: First, by reducing the value of intrinsic controller delay t_D or second, by reducing the value of threshold current I_T. A conventional hysteretic controller works in voltage mode that involves voltage sensing across a series resistor [66]. This increases the loop delay and output impedance of the class-AB buffer. Alternatively, a current-mode hysteretic controller can be used, which demonstrates less t_D because signal mirroring and comparison are much faster in the current domain. Chowdhury et al. [67] propose a current-mode hysteretic controller that enables the SA to source/sink current in synchronization with the fast input envelope transients of 20/40 MHz bandwidth for a 802.11n WLAN transceiver.

The second method for reducing delay focuses on reducing the value of hysteresis threshold currents ($\pm I_T$) in order to the reduce the overall magnitude of I_{HYS}. Since I_T is a design parameter that can be set through internal or external control, its value can be made smaller at the cost of high switching frequency. He et al. [37] propose the hysteretic controller, as shown in Fig. 29, for tracking LTE signals up to 40 MHz bandwidth. With this structure, there is no requirement of generating the hysteresis reference currents, thus making $I_T \approx 0$, and hence reducing the value of I_{HYS}. There is a just one reference signal (I_{bias}) in the design along with an input signal (I_{sense}), which is a fraction of the output current from the LAs class-AB stage. Instead of comparing I_{sense} within a hysteresis window of $\pm I_T$ as typically done in the conventional controller designs [17], the proposed structure of Fig. 29 compares (I_{sense} + I_{bias}) with I_{bias} through a basic current comparison, which significantly reduces the delay. Choi et al. [68] introduce a programmable hysteretic controller that uses an external voltage to control the value of I_T, and hence I_{HYS}. The control voltage is varied to change the value of I_T depending upon the input signal's bandwidth.

F. Multiswitcher Topology (Digital Tracking)

The conventional HSM architecture operates in an analog fashion, which generally supports carrier channel bandwidths for the 5G frequency range 1 (FR1) standard up to 100 MHz [69].

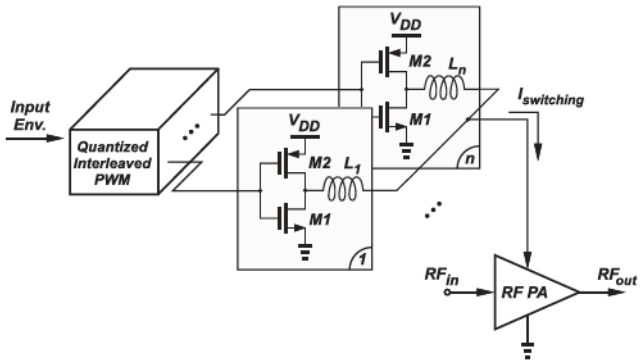

Fig. 30. Multiswitcher architecture (digital tracking) [71].

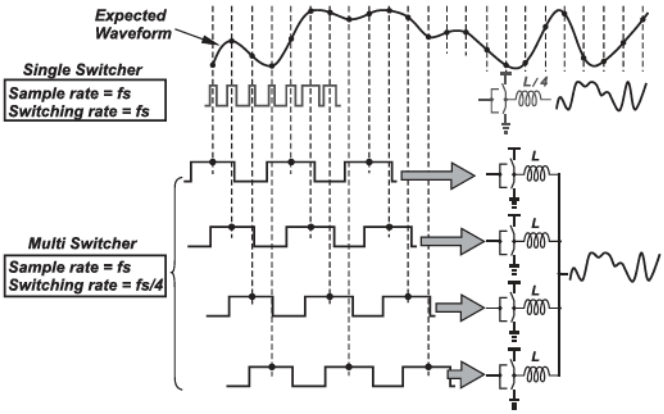

Fig. 31. Transient waveforms of single and multiswitcher topologies [72].

In order to support the 5G FR2 standard (or mmWave bands), there are two main design bottlenecks. First, it is difficult to design an LA that can support higher channel bandwidths (typically more than 100 MHz) due to stability challenges and power consumption. Second, the switching losses increase significantly in the SA due to the requirement for high switching frequency.

In order to remove the analog limitations of an HSM, the SM can potentially be operated with a multiswitcher topology in a digital manner [70]. A multiswitcher topology [71] typically uses multiple switches (or power stages) connected together in parallel, as shown in Fig. 30, and avoids the use of an LA. The switches are controlled digitally by PWM signals [72] and operate in an interleaved manner. With interleaving, the switching rate of each switcher is reduced by the number of interleaved stages, as illustrated in Fig. 31. Furthermore, the digital tracking is less sensitive to the RF-envelope path delay mismatch [73]. Hence, this topology can potentially lead to tracking of wideband envelopes. Multiple improved techniques, such as zero-voltage switching (ZVS) [74] and soft switching [75], can also be employed with the power stages to further reduce the switching losses.

To avoid the use of multiple power stages and inductors in the digital tracking topology, several improvements have been made. Bang et al. [73] proposes an SM using a multiswitcher/digital tracking topology to track 200 MHz of channel bandwidth. The proposed design employs a switched-capacitor voltage divider

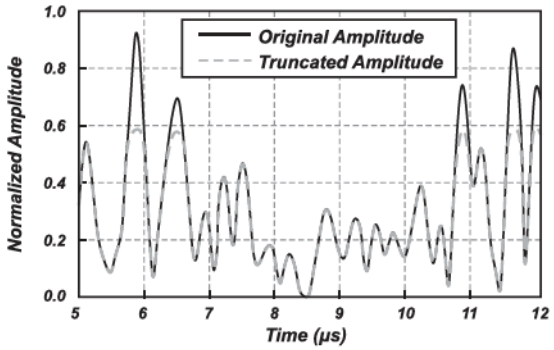

Fig. 32. Time-domain waveform of the wideband code division multiple access (WCDMA) signal and its truncated (or decrested) version [79].

with level-selection switches (which can be controlled at the system level) to generate six uniform voltage levels for the envelope supply voltage. This digital tracking supports wider bandwidth than the traditional analog HSM amplifier because it dynamically changes a supply voltage level by connecting one of the multiple voltages generated by the switched-capacitor voltage divider to the output via switches [76].

G. System-Level/Software Techniques

The above proposed methods that improve speed by enhancing bandwidth, enhancing SR, or reducing controller delay add additional challenges to the original HSM design. The improved topologies/architectures increase complexity of the circuit, introduce stability challenges [77], increase switching frequency, add to static dc power consumption, and/or increase the physical size. On the other hand, system-level/software techniques that perform DSP on the input envelope signal require minimal hardware overhead. With these proposed techniques, the bandwidth, SR, and delay requirements are significantly relaxed with some compromise on the ET performance. There are three popular input signal processing techniques, namely, PAPR reduction, bandwidth reduction, and SR reduction of the input envelope. Each of these techniques is discussed in the following text.

The first technique focuses on PAPR or crest-factor reduction of the input envelope using various algorithms [78], such as clipping and filtering, selective mapping, partial transmit sequence, linear block coding, and peak insertion. These methods generate a decrested version of the input envelope signal, which essentially reduces the peak of the input envelope above a certain voltage level (decided by design requirements). Notably, Jeong et al. [79] introduce an algorithm that generates a decresting function for the RF input signal to reduce the PAPR of an input WCDMA envelope from 7.6 to 5.2 dB with minimal impact on its linearity and efficiency performance. Fig. 32 shows the time-domain waveform of a WCDMA signal before and after this PAPR reduction.

The second technique primarily focuses on reducing the bandwidth of the input envelope using different algorithms, such as low-pass finite impulse response filtering, power ET [80], and elimination of drastically changing peaks [81]. These methods

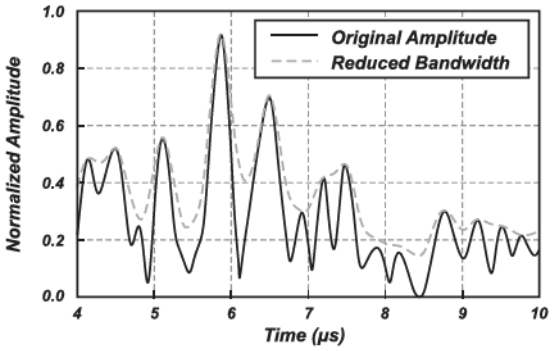

Fig. 33. Time-domain waveform of the WCDMA signal before and after bandwidth reduction [82].

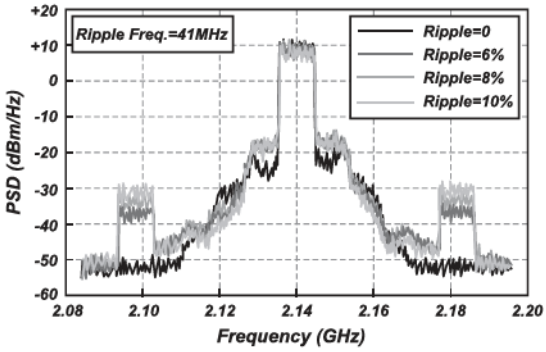

Fig. 35. Effect of supply ripple (HSM output) on the PAs PSD [19].

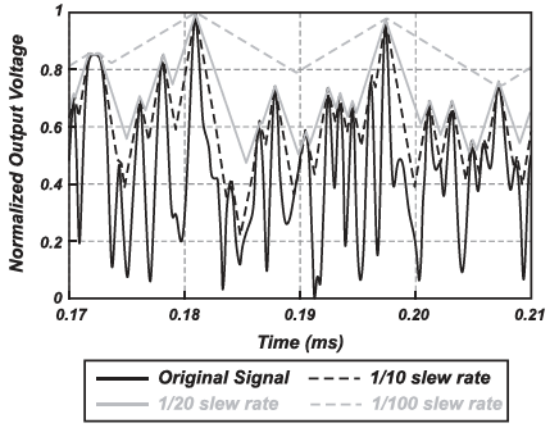

Fig. 34. Envelope signal with different SRs [85].

essentially generate a slow varying version of the actual envelope and feed it to the PA supply. With a slower varying supply signal, the PAs efficiency is affected, but the design constraints on the HSM are more relaxed. Jeong et al. [82] introduce a filtering technique where the envelope signal is low-pass filtered and subtracted from itself to derive a difference signal, which is then rectified. The rectified residue signal is filtered and then added back to the filtered envelope signal. This technique reduces bandwidth of the original envelope signal from 20 to 5 MHz. Fig. 33 shows the time-domain waveform of this WCDMA signal before and after bandwidth reduction.

The third technique focuses on generating an SR limited version of the original envelope to control the PA's dynamic supply. Multiple algorithms [83], [84], [85] have been proposed to reduce the input envelope's SR. Gilabert et al. [86] generate several envelopes with reduced SR (1/10, 1/20, and 1/100 of the original signal), as shown in Fig. 34, using an algorithm that resamples the original envelope $E(n)$ at a lower rate of F_S defined by the designer. The SR limited instantaneous envelope $SL\_E(n)$ can be defined as follows:

$$SL\_E(n) = \left|\frac{E(n) - E(n-1)}{T_S}\right| . V_{\text{MAX}} \tag{12a}$$

$$= |\Delta E(n)| . F_S . V_{\text{MAX}} \tag{12b}$$

where $E(n)$ is the input envelope, V_{MAX} is the maximum voltage value at the HSM output that corresponds to the maximum desired transistor drain bias, and T_S and F_S are the sampling time and sampling frequency, respectively. From (12a) and (12b), the resulting SR $SL\_E(n)$ is reduced from the original envelope signal's SR and dependent upon the sampling frequency F_S (which can be set externally).

VI. Linearity Improvement in HSM

An HSM needs to demonstrate high linearity at its output, as any ripple component injected to the PA from the power supply mixes with the RF carrier and is upconverted to the PAs output signal sideband frequencies (as illustrated in Fig. 7). The magnitude of the sidebands due to PA supply ripple can be calculated from (3). Alsahali et al. [19] demonstrated through measurements that the supply ripple component present at a frequency of 41 MHz was upconverted to the PAs output signal sidebands around the RF carrier frequency of 2.14 GHz, as shown in the PAs output signal PSD plot of Fig. 35. Fig. 35 also demonstrates that increasing the PAs supply ripple magnitude increases the magnitude of the sidebands in the PSD. If the PA demonstrates insufficient power supply rejection, the ripple from the HSM is likely to cause violations of the transmit spectral mask [87].

The ripple content at the output of an HSM can be reduced by using a higher order output LC filter. But the use of such filters limits the maximum HSM bandwidth of operation and is not suitable for wideband applications. The ripple voltage at the output node (V_{out}) of the HSM can be expressed as follows:

$$V_{\text{out\_ripple}}(s) = I_{\text{ripple}}(s) \times (Z_{\text{out}}(s) \parallel R_{\text{PA}}) \tag{13}$$

where $V_{\text{out\_ripple}}$, I_{ripple}, Z_{out}, and R_{PA} represent the output ripple voltage, switching ripple current, closed-loop output impedance of the LA, and PA load resistance, respectively. As seen from (13), the value of $V_{\text{out\_ripple}}$ can be reduced by two methods. First, the magnitude of I_{ripple} can be minimized by reducing the amount of generated ripple content. Second, the magnitude of the parallel combination of $Z_{\text{out}}(s)$ and R_{PA} can be decreased by providing ripple cancelation from the LA. Different methods for reducing the HSM output voltage ripple are explained in the following sections.

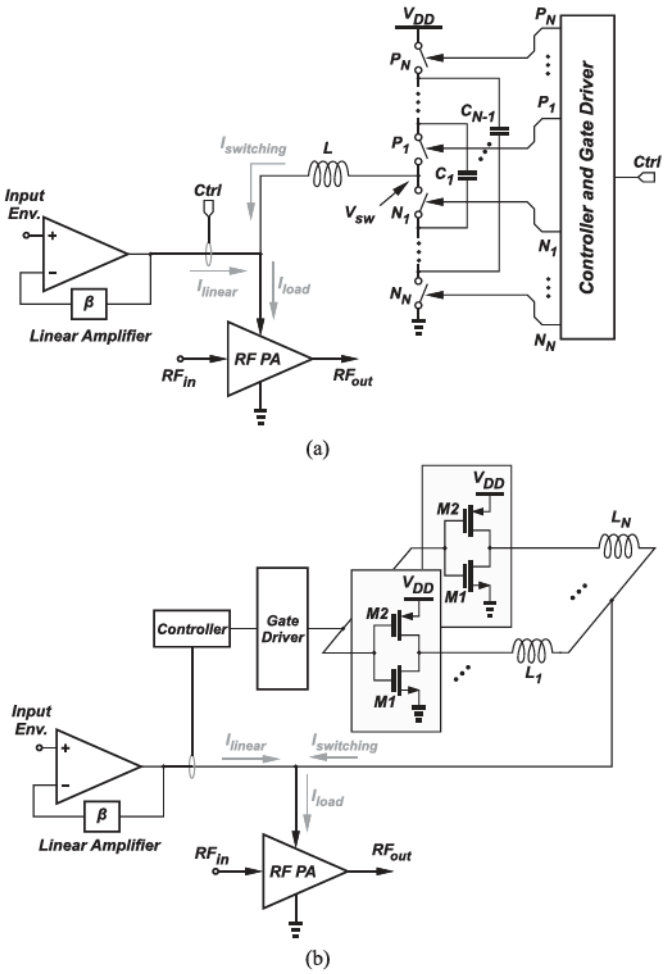

Fig. 36. HSM with (a) multilevel and (b) multiphase SA topologies.

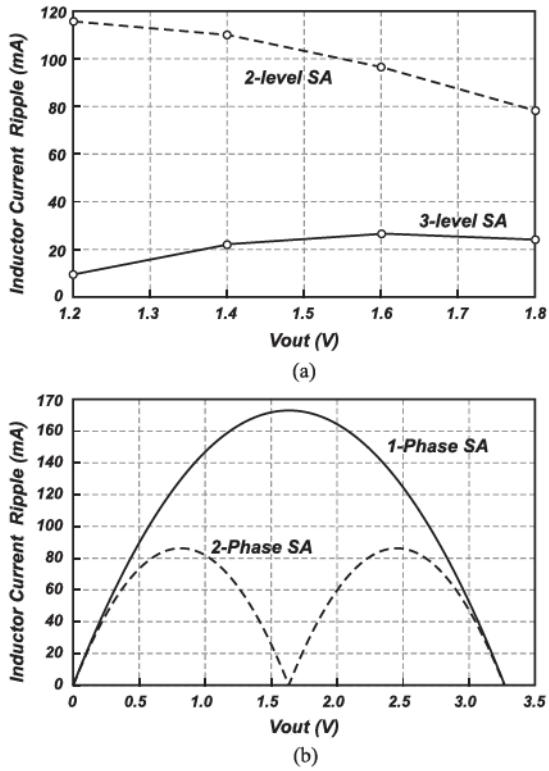

Fig. 37. Current ripple reduction with (a) three-level [92] and (b) two-phase [27] SA topologies.

A. Minimizing Current Ripple (I_{ripple})

The SA is responsible for providing the average supply current to the load. This current also includes switching ripple. The linearity of an HSM can be improved if the inductor's ripple current I_{ripple} from the SA is reduced. This can be achieved by adopting one of the advanced SA topologies discussed in the following text.

1) Multilevel SA: In the first topology, a multilevel converter design is used for the SA, as shown in Fig. 36(a). The basic idea behind the multilevel converter is to reduce the inductor current ripple by reducing the voltage swing across the inductor (or at the switching node V_{sw}). The magnitude of the maximum-current ripple for a multilevel converter ($I_{\text{max\_ripple}-n}$) compared with the maximum-current ripple ($I_{\text{max\_ripple}-2}$) for a basic two-level converter is described by the following relationship:

$$I_{\text{max\_ripple}-n} = \frac{1}{(n-1)^2} I_{\text{max\_ripple}-2} \tag{14}$$

where n represents the number of switching levels. Due to its low output ripple (or noise), a multilevel SA topology is used for improving linearity in ET-PA systems [62], [88], [89].

The most commonly used multilevel SA topology is a three-level converter, as previously shown in Fig. 16. A complementary signal drives the outer devices, $M1$ and $M2$, with duty cycle $D = V_{\text{OUT}}/V_{DD}$, similar to the two-level converter. A second complementary signal of equal duty cycle drives the inner devices, $M3$ and $M4$, but is 180° out-of-phase from the outer device's signal. By keeping the flying capacitor C_F balanced at $V_{DD}/2$, the V_{sw} switch node alternates among V_{DD}, $V_{DD}/2$, and ground; hence, the term "three-level." In three-level operation, when V_{out} is smaller than $V_{DD}/2$, the V_{sw} node switches between either ground and $V_{DD}/2$, and when V_{out} is larger than $V_{DD}/2$, the V_{sw} node switches between $V_{DD}/2$ and V_{DD}. The smaller step of V_{sw} voltage reduces the slope of the inductor current ripple. Moreover, the frequency of the inductor current is twice of the switching frequency. As a result, the inductor current ripple of the three-level topology is smaller than one-fourth of the standard two-level topology with the same LC value [42]. A detailed description of the charging/discharging for different duty cycle ratios and control logic to always regulate $V_{DD}/2$ across the flying capacitor is given in [90] and [91]. Liu et al. [92] adopt a three-level SA converter topology and demonstrates a reduction of more than 65% in I_{ripple} (as compared with a two-level SA) over the HSM output voltage range, as shown in the measured I_{ripple} results in Fig. 37(a).

2) Multiphase SA: In the second topology, a multiphase converter design is used to implement the SA, as described by the diagram in Fig. 36(b). In a conventional single-phase SA converter, all the load currents (along with I_{ripple}) are provided

through a single inductor. However, in the case of a multiphase SA converter, the total load current is split between multiple inductors. Based on the alignment between the multiple phases, ripple cancelation can be achieved [43] to minimize the effective magnitude of I_{ripple}. To achieve this operation, a current-sharing control circuit is needed to balance the phase currents in the multiple inductor paths. The most commonly used multiphase topology is a two-phase SA converter. Wu and Mok [27] adopt a two-phase SA converter topology and demonstrates a reduction of more than 50% in I_{ripple} (as compared with single-phase SA) over the HSM output voltage range, as shown in the measured I_{ripple} results in Fig. 37(b).

3) Combined Multilevel and Multiphase SA: As discussed in the previous sections, there have been works that implement advanced SA topologies, such as multilevel and multiphase. But to the best of the authors knowledge, works that implement both multilevel and multiphase together have not been well explored for CMOS HSMs. Although this article focuses on HSM implementations in CMOS technology, there are notable works that use discrete/off-the-shelf components and employ both multilevel and multiphase in the same design as well as some current ripple reduction techniques in the SA [93], [94], [95], [96]. However, it is important to note that these works implement the SM as an SA (not within an HSM architecture) and focus on improving multiple performance parameters, such as efficiency, speed, and linearity [97]. The devices are driven by PWM signals, but due to high switching ripple at the output (because there is no ripple cancelation from the LA), the system linearity can be jeopardized. Lazarevic et al. [98], [99] explain the choice of output filter passive components based on the cutoff frequency. The sources of nonlinearity in linear and switched-assisted SMs are also explained and the optimum values of bandwidth, feedback ratio, switching frequency, and digital control hardware clock frequency can be identified to achieve the desired ET-PA system linearity. The multilevel and multiphase architectures offer advantages for performance enhancement and may be explored for realizing the SA within future CMOS-based HSMs.

Yerra and Krishnamoorthy [93] propose a two-phase three-level SM to track a 20 MHz 4G LTE envelope signal, as shown in Fig. 38. The design uses Gallium Nitride FETs for the power devices and a discrete gate driver with adjustable deadtime and switching frequency to drive the power stage. The SM uses a ZVS technique for better efficiency and a fourth-order ZVS low-pass filter to track large bandwidth envelope signals and to maintain current self-balancing in the multiphase converter system. Yerra et al. [94] extend the work in [93] to propose a cascaded switching capacitor-based four-phase three-level SM and the experimental results are provided to validate the proposed concept.

Roberts et al. [95] introduce a novel single-flying capacitor multiphase converter with negatively coupled output inductors as an attractive alternative to multiphase solutions based on the conventional two-level SA topologies that are almost exclusively used in industry. With the combination of relatively low switch-node voltages and the output inductors being negatively coupled together, each phase's current ripple is significantly less than a

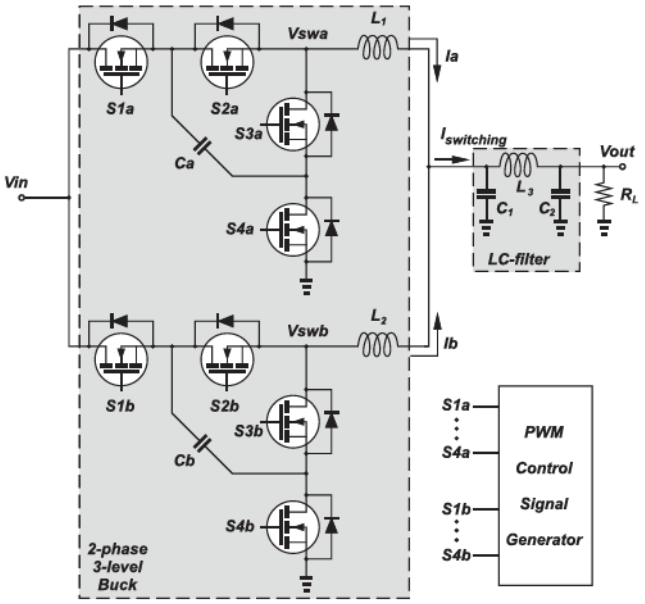

Fig. 38. SA with two-phase and three–level converter topology [93].

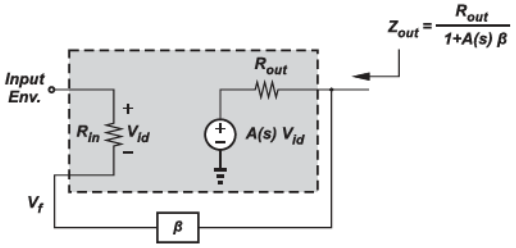

Fig. 39. Simplified model of the LA for calculating output impedance.

multiphase with the conventional two-level SA and magnetically isolated inductors. The architecture of the article presented in [96] explores a multiphase flying capacitor multilevel SA with coupled inductors for ripple reduction and intrinsic flying capacitor voltage balancing.

Depending upon the HSMs linearity requirements, the numbers of levels or phases are selected in multilevel and multiphase topologies of the SA. But both of these SA current ripple reduction topologies suffer from some inherent tradeoffs. The multilevel SA converter design requires the use of flying capacitors for its operation. The value of each capacitor is generally large ($\approx$ nF to μF range) and difficult to integrate on-chip. The multiphase SA converter design requires the use of more than one off-chip inductor for its operation, which also consumes extra area on the board and increases complexity for assembly. Furthermore, both SA converter topologies require additional control circuitry for their operation, which ultimately increases the complexity of the HSM design.

B. Voltage Ripple Cancelation

Another way of reducing ripple is to optimize the LAs gain and bandwidth. Since the PA load R_{PA} is generally fixed and set by the PAs design requirements, ripple reduction efforts

focus on reducing the magnitude of the LAs closed-loop output impedance $Z_{\text{out}}(s)$ in (13). As depicted in Fig. 39, The value of $Z_{\text{out}}(s)$ depends on the output impedance R_{out} of the class-AB stage, the gain of the LA ($A(s)$), and the feedback factor (β), as follows:

$$Z_{\text{out}}(s) = \frac{R_{\text{out}}}{1 + A(s)\beta}. \tag{15}$$

Therefore, a low value of $Z_{\text{out}}(s)$ can be accomplished by designing a high-gain amplifier with a proper feedback network. Since R_{out} and β are nearly constants (based on the design), $Z_{\text{out}}(s)$ shows a reverse frequency response to $A(s)$ from (15), and its value gets higher as the frequency increases. Therefore, it is important for the LA to maintain a high value of $A(s)$ to keep the value of $Z_{\text{out}}(s)$ low. When doing this, the magnitude of output voltage ripple $V_{\text{out\_ripple}}$ approaches zero, which means that the LA absorbs all the ripples from the SA and, therefore, provides voltage ripple cancelation. But with aggressive channel length scaling in CMOS technologies, it is increasingly more difficult to achieve high LA gain because the intrinsic low-frequency gain of a transistor drops, as described by the following equation:

$$\text{Intrinsic gain} \propto \frac{L}{V_{ov}}. \tag{16}$$

With smaller channel lengths, the transistor's intrinsic gain becomes so low (on order of 10s V/V) [100] that a single-stage LA does not provide sufficient gain. Also, the supply voltage level decreases with advancing CMOS generations, which reduces the device headroom in an LA and makes it difficult to cascode transistors. Therefore, horizontal cascading of multiple stages is performed to maximize the overall LA gain, $A(s)$. Cascading of multiple stages can provide higher gain, but LA stability must be ensured at all operating points of the input signal envelope. Tan and Ki [49] and Kim et al. [55] adopt a three-stage cascaded LA architecture to achieve a high value of $A(s)$. Due to this high gain, Kim et al. [55] demonstrate a low ripple voltage ($\approx 3-8$ mV) at the HSMs output with attenuation for the second harmonic remaining below -40 dBc.

VII. Output Power Improvement in HSM

In an ET-PA system, the HSM acts as a power source that modulates the PAs supply power with respect to input envelope. The HSMs output power depends upon the maximum supply voltage that the LA can support (via feedback) and load resistor [from (6)]. When the battery voltage level supplying the LA remains constant, delivering output power to the load is not difficult. But due to voltage variation in the battery over time, the supply level of the LA decreases, thus reducing the LAs output power. Moreover, the maximum supply voltage level decreases with advancements in CMOS technologies, which limits the LAs supply voltage and, hence, HSM output power. Various architectures to prevent LA supply voltage degradation and improve HSM output power are discussed in the following sections.

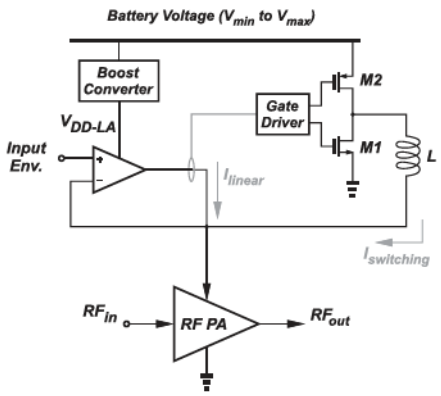

Fig. 40. Boost-mode HSM architecture [102].

A. Boost-Mode HSM

A wireless handset device is generally powered by a Li-ion battery whose voltage degrades with time and discharge. For instance, when the battery is fully charged, its voltage is nearly 4.2 V, but as it is discharged, the voltage level reduces to 3.5 V and drops quickly thereafter [101]. Since the output voltage of the LA depends upon the battery voltage, the HSM output power degrades as the battery drains. Therefore, a boost converter can be added between the LAs supply and the battery to maintain a constant voltage supply for the LA, irrespective of battery voltage variations, as illustrated by the diagram in Fig. 40. With this architecture, the LA can process envelope levels up to the constant boosted supply voltage ($V_{DD-\text{LA}}$), while the battery voltage varies from V_{max} to V_{min}. Choi et al. [102] adopt a boost-mode HSM architecture that maintains a constant 5 V supply for the LA and provides constant HSM output power with battery voltage variation from 4.2 to 2.8 V.

The major disadvantage of a boost-mode HSM architecture is that the efficiency of the additional boost converter limits the maximum HSM efficiency. Also, due to the presence of a switched-mode boost converter, the LA receives additional ripple at its supply node, which can propagate through the HSM and degrade the ET-PA system linearity.

B. AC-Coupled HSM

A boost-mode HSM architecture prevents the degradation of output power but does not improve HSM output power beyond its nominal value. Furthermore, the boost-mode HSM does not provide a solution for achieving higher output powers (large envelope voltage) with decreasing supply levels. An ac-coupled HSM architecture can be used to overcome these challenges.

Most of the conventional HSM designs are dc coupled, where the LA and SA are directly connected to the output. But in the ac-coupled HSM of Fig. 41, the output of the LA is isolated from the HSMs output via a large ac-coupling capacitor. This capacitor maintains a constant offset voltage (V_{offset}) across it, which makes the sum of the LA supply (neglecting device headroom) and V_{offset} equal to the input envelope voltage value. With this architecture, the LAs supply voltage can be lowered (V_{DD_L}), and an HSM can be implemented in smaller CMOS

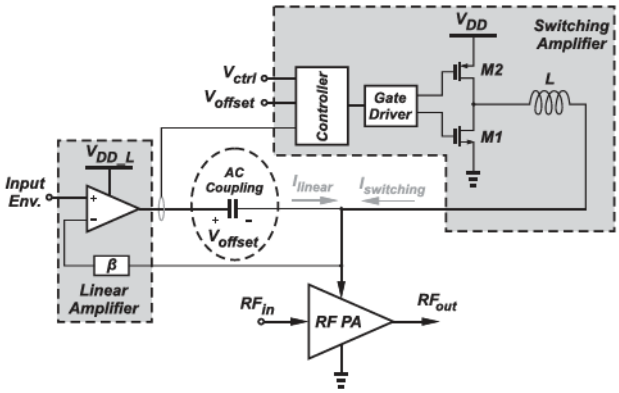

Fig. 41. AC-coupled HSM architecture.

TABLE II
PERFORMANCE COMPARISON OF AC-COUPLED HSM

Ref	CMOS Tech.	Modulation	V_{DD} (V)	Max eff (%)	Max pout (W)
[64]	90 nm	LTE 6RB	5.0	88.0	3.2*
[64]	90 nm	LTE 10M	5.0	83.0	3.2*
[104]	0.153 μm	LTE 20M	3.8	87.1	3.5
[105]	0.13 μm	LTE 40M	4.0	83.0	0.92*
[104]	0.153 μm	LTE 40M	3.8	85.5	3.5
[106]	90 nm	LTE 40M	4.0	83.0	1.8
[104]	0.153 μm	LTE 60M	3.8	82.3	3.5
[104]	0.153 μm	LTE 80M	3.8	81.2	3.5
[64]	90 nm	5G NR 100M	5.0	77.0	3.2*

* Extracted from graph.

technology nodes to support faster tracking of input envelopes (as discussed in Section V). Furthermore, depending upon the value of V_{offset}, the envelope signal's voltage magnitude can be increased to increase the HSMs output power. To-date, the ac-coupled HSM architectures have achieved highest reported output powers in CMOS.

A disadvantage of the ac-coupled architecture is that it requires an extra ac-coupling capacitor that has large value ($\approx$ nF to µF range) and is, therefore, difficult to integrate on-chip. The value of V_{offset} also needs to be carefully controlled to attain the proper envelope signal at the HSM output. Additionally, an extra control loop is required [103] to maintain V_{offset}, which leads to increased HSM design complexity. Table II summarizes the state-of-the-art works using the ac-coupling technique. The majority of the most recent works in HSM design focus on ac-coupled architectures and demonstrate highest reported ET bandwidths.

VIII. DEVICE TECHNOLOGIES AND ET-PA SYSTEM CHALLENGES

An SM alleviates the PAs impact on transmitter power consumption, which leads to considerable power savings, extended battery lifetime, smaller heat-sink designs (for base-station applications), and potentially higher reliability. But this improvement in efficiency comes at the cost of extra die area and an increased bill-of-materials. As multiple SM and PA device technologies are industrially available, selecting the most suitable technologies for hardware realization is a key decision to achieving optimum performance for an ET-PA system.

TABLE III
COMPARISON OF DIFFERENT PA DEVICE TECHNOLOGIES

Parameters	Device technology			
	CMOS	GaAs	SiGe	LDMOS
Passives quality	Low	High	Low	Low
Transition freq.	Moderate	High	High	Low
Breakdown voltage	Low	High	Moderate	High
Cost	Low	High	High	Moderate
Integration	High	Low	Moderate	Moderate
Availability	High	Moderate	Moderate	Low

A. SM Device Technologies

Most of the developments in HSM target cellular handset applications in sub-6 GHz bands. CMOS and SiGe-BiCMOS are the two main device technologies typically chosen for HSM implementation. Due to their lower cost, low power consumption, and high integration capability with the baseband processor and RF frontend, CMOS processes are the favored choice. Furthermore, CMOS allows integration of on-chip calibration and self-test circuitry [107]. Table IV summarizes performance of the state-of-the-art CMOS HSMs. It can be observed from Table IV that lower CMOS nodes are preferred for tracking higher modulation bandwidths, but they also lead to lower output power (due to lowered supply). Therefore, the ac-coupled architectures for HSM are gaining traction (in both academia and industry), as they provide the ability to track high bandwidths using more advanced CMOS process nodes without compromising on power. This is demonstrated in Table IV, where the articles presented in [64], [149], [150], and [51] are the ac-coupled architectures that also achieve highest bandwidths of 100 MHz and above.

B. PA Device Technologies

There are multiple technologies for PA implementation, most popularly CMOS, gallium arsenide (GaAs), silicon germanium (SiGe), and laterally-diffused metal-oxide semiconductors (LDMOS), which are industrially available for cellular mobile applications. GaN has yet to be adopted for commercial handsets due to its higher cost, knee voltage, and typically lower yields. The PA technology is typically chosen based on the PAs RF performance specifications and integration requirements. A qualitative performance comparison of different PA device technologies is given in Table III.

It is important to note that, while CMOS is usually preferred for HSM realization, GaAs is mainly chosen for implementing PAs because of its superior ability to support high-frequency and high-power applications with good efficiency and reliability. Therefore, GaAs processes dominate the existing PA market [108].

TABLE IV
PERFORMANCE COMPARISON OF STATE-OF-THE-ART CMOS HSM SOLUTIONS (SORTED BASED ON MODULATION BANDWIDTH)

Ref.	CMOS tech.	BW (Hz)	V_{DD} (V)	Load (Ω)	Max pout (W)	Max eff (%)	Die (or Chip) area (mm^2)	Off-chip ind	AC-Cap
[20]	0.15 μm	10M	4.5	8.0	0.93	82.0	1.60	1 μH	NA
[64]	90 nm	10M	5.0	3.2	3.2*	83.0	5.14	3 ind	1 cap
[60]	0.18 μm	10M	3.6	6.0	1.02*	83.0	1.10	10 μH	NA
[139]	0.13 μm	10M	4.0	8.0	0.8	80.0	5.00	1 ind	1 cap
[140]	0.18 μm	10M	3.4	7.5	–	80.4	1.82	1 ind	NA
[141]	0.18 μm	10M	5.0	6.5	0.56*	75.3	1.82	1 ind	NA
[142]	0.18 μm	10M	3.3	6.2	1.05	86.5	3.84	4.7 μH + 51 nH	NA
[143]	0.18 μm	10M	3.3	–	1.5	85.8	7.44	78 nH (×2)	NA
[62]	0.13 μm	10M	3.8	4.7	–	86.2	6.35	4.7 μH + 22 nH	0.47 μF#
[144]	0.18 μm	10M	4.7	7.8	–	81.5	0.60	1 ind	NA
[145]	0.18 μm	10M	3.3	6.0	0.85	75.2	1.55	1 ind	NA
[146]	0.18 μm	10M	3.3	–	1.0	83.6	1.50	1 ind	NA
[47]	0.18 μm	20M	3.45 - 5.0	6.5	–	75.9	1.40	1 ind	NA
[56]	0.18 μm	20M	3.5	4.6	1.1	79.6	1.15	1 ind	NA
[92]	65 nm	20M	2.4	3.9	0.8	88.7	3.42	206 nH	1 μF + 7 nF#
[104]	0.153 μm	20M	3.8	4.0	3.5	87.1	5.13	1 μH + 0.68 μH	4.7 μF
[147]	0.18 μm	20M	5.5	5.2	0.89	83.0	1.47	1 μH + 0.3 μH	NA
[149]	90 nm	20M	–	–	0.25	88.4	4.1	3 ind	1 cap
[56]	0.18 μm	40M	3.5	4.6	1.1	76.4	1.15	1 ind	NA
[59]	65 nm	40M	2.4	4.7	1.0*	93.0	2.72	538 nH	12 nF#
[104]	0.153 μm	40M	3.8	4.0	3.5	85.5	5.13	1 μH + 0.68 μH	4.7 μF
[105]	0.13 μm	40M	4.0	5.0	0.92*	83.0	4.00	2 ind	1 cap
[106]	90 nm	40M	4.0	4.7	1.8	83.0	3.00	3 ind	1 cap
[122]	0.18 μm	40M	3.6	6.7	1.2	85.0	2.25	1 μH	NA
[148]	0.18 μm	40M	3.6	4.0	1.8	85.0	2.25	4.7 μH	NA
[63]	0.25 μm	40M	5.0	–	1.5	79.1	2.89	2 ind	NA
[56]	0.18 μm	60M	3.5	4.6	1.1	74.0	1.15	1 ind	NA
[104]	0.153 μm	60M	3.8	4.0	3.5	82.3	5.13	1 μH + 0.68 μH	4.7 μF
[56]	0.18 μm	80M	3.5	4.6	1.1	72.8	1.15	1 ind	NA
[59]	65 nm	80M	2.4	4.7	1.0	91.0	2.72	538 nH	12 nF#
[104]	0.153 μm	80M	3.8	4.0	3.5	81.2	5.13	1 μH + 0.68 μH	4.7 μF
[52]	0.18 μm	100M	5.0	5.0	5.0	88.0	–	2.2 μH	NA
[64]	90 nm	100M	5.0	3.2	3.2*	77.0	5.145	3 ind	1 cap
[149]	90 nm	100M	–	–	0.55	84.0	6.9	4 ind	1 cap
[150]	90 nm	100M	5.0	–	3.5	84.0	–	2 ind	1 cap
[65]	90 nm	130M	5.8	–	3.53	84.1	6.9	2 ind	4.7 μF
[51]	40 nm	160M	3.6	5.0	1.9	88.0	2.24	1 μH	1 μF
[50]	0.18 μm	200M	5.0	5.0	4.0	88.0	–	2.2 μH	NA
[73]	90 nm	200M	–	–	4.5	93.6	13.6	4 ind	NA

* Extracted from graph.
# flying capacitor value.

C. PA Integration

The commercial wireless handset market demands high levels of sophistication [109] with low component cost and power. Modern solutions require multistandard and multiband functionality, along with a platform to support wireless connectivity features, such as GPS, Bluetooth, and WLAN.

Due to significant channel length scaling, the transition frequency of transistors in CMOS technology has reached well beyond 100 GHz, which makes CMOS popular for RF applications. [110]. Therefore, to achieve complete integration of baseband functionality and the radio chain, it is desirable to also integrate the PA in CMOS [111], [112], [113], [114], [115], [116], [117]. CMOS technology has already proliferated hardware for Bluetooth and ZigBee applications that include integrated PAs. However, these PAs typically operate at lower power levels and demand lower bandwidths, therefore having more relaxed performance requirements compared with cellular communications hardware.

Unfortunately, PA implementation in CMOS processes faces some technical hurdles. Low breakdown voltage levels, lower device gain, linearity issues due to high-compression characteristics, lack of through-wafer ground-vias, high substrate loss, poor thermal dissipation, and lack of high-voltage capacitors are among the technical challenges. The cost of research and development for deep submicron CMOS IC design has also increased dramatically due to the high cost of photomasks [118].

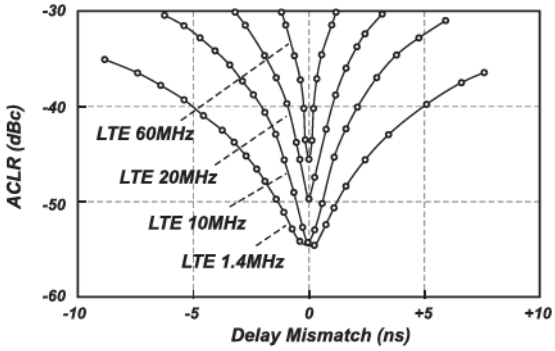

Fig. 42. ACLR versus delay mismatch for various LTE envelope signal bandwidths [124].

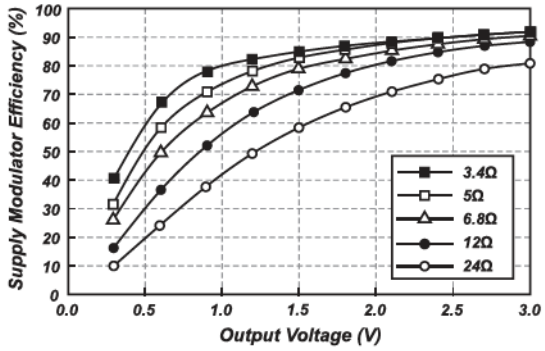

Fig. 43. Measured HSM efficiency for various load resistances [14].

The ability to overcome these challenges will largely determine if and when production PAs can be integrated in CMOS (with the HSM). There is a recent trend toward implementing PAs in Silicon-on-Insulator (SOI) processes, as SOI processes provide higher speed, low power, higher intrinsic gain, much less substrate loss/coupling, no source-body and drain-body diodes (in fully depleted version of SOI), separate back-gate terminal for reducing leakage current, and higher device density compared with most bulk CMOS processes [119], [120], [121].

D. ET-PA System Challenges

An ET-PA system consists of the SM, the PA, and extra control circuitry. Typically, the SM and PA are designed separately, and the connection between the separate blocks can become a bottleneck in ET-PA system performance. There are multiple challenges in interfacing the SM with PA, which are briefly analyzed in the following sections.

1) Delay Mismatch: In an ET-PA system, the baseband input envelope signal and the RF signal are provided separately to the SM and the PA, respectively. The delay in the RF path is usually substantially shorter than that of the envelope (SM) path. Therefore, the delay mismatch [122] between these two paths is a source of distortion. As explained in [123], the intermodulation distortion (IMD) introduced by this delay mismatch can be described as follows:

$$\text{IMD} = 2\pi B_{\text{RF}}^2 \Delta_\tau \tag{17}$$

where B_{RF} is the modulation bandwidth of the RF signal, and Δ_τ is the magnitude of delay mismatch. The minimum lower and upper band intermodulation distortion ($\text{IMD}_{l,u}$) determines the PA output signal's ACLR value as follows:

$$\text{ACLR} = \min(\text{IMD}_{l,u}) + k \tag{18}$$

where k is a correction factor determined by the PAPR level and the PA's compression point [124]. An example of the effect of delay mismatch on ACLR can be observed in Fig. 42 for various bandwidth LTE signals. As the LTE envelope signal's bandwidth increases, the delay mismatch between the RF and the envelope path must decrease to satisfy the required output signal quality (EVM). The delay mismatch can be fixed through calibration techniques with fine delay tuning capability.

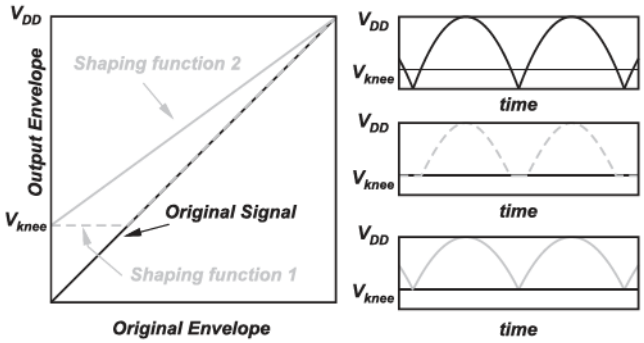

Fig. 44. (left) Envelope shaping using different functions and (right) their respective time-domain waveforms [68].

2) SM Load Variation: Historically, an SM is designed and optimized for a fixed value of PA load (drain impedance) [49], [55]. But, this fixed resistive model for the PA does not hold true in practical ET operation. Collins et al. [125] and Bhardwaj et al. [126] have demonstrated that the PAs drain impedance varies with the V_{DD} supply. As the SM efficiency is dependent on the PAs drain impedance [from (6)], this variation leads to a change in SM efficiency. Choi et al. [14] measure HSM efficiency under different resistive loads (see Fig. 43) and shows that SM efficiency can change significantly under different loading conditions. Therefore, the variation in PA drain impedance should be accounted for when optimizing any HSM design in order to minimize efficiency degradation.

3) Envelope Shaping: Most SMs are designed to process the entire input envelope's voltage swing, and this swing appears at the drain of the PA as its supply voltage. If the PAs supply voltage becomes lower than the PA device's knee voltage (V_{knee}), the nonlinear output capacitance in the PA device would suddenly increase [131] and the PA would demonstrate a highly nonlinear behavior with high amplitude-to-amplitude modulation (AM–AM) and amplitude-to-phase modulation (AM–PM) distortion at the output. To avoid this problem, the input envelope is shaped to avoid lower power levels below the V_{knee} region. As demonstrated in Fig. 44, different functions can be used to shape the original envelope. Notably, Zhu et al. [132] introduce a shaping function for the entire envelope voltage range to achieve

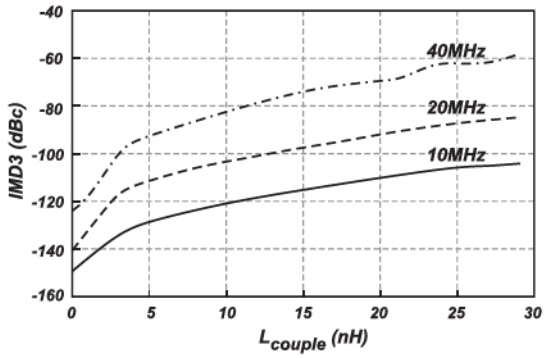

Fig. 45. IMD3 response versus coupling inductor (L_{couple}) [134].

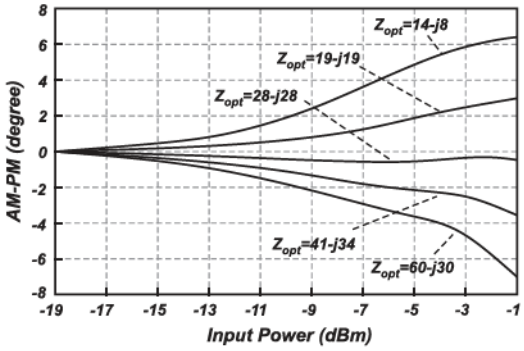

Fig. 46. PAs AM–PM response for various Z_{opt} values [128].

improved PA linearity through third-order intermodulation distortion (IMD3) cancelation.

4) SM-PA Physical Interface: Usually, a coupling inductor (L_{couple}) is used to connect the SMs output to the PAs drain node since these are typically implemented on separate die. The L_{couple} can be a bondwire or can be used as a choke for the PA, but the presence of L_{couple} degrades the PAs linearity because it increases the PAs memory effects and adds to the output noise [133]. Balteanu et al. [134] implement an ET-PA system in which the SM is implemented in a 0.18 μm process and connected to a heterojunction bipolar transistor class-E PA via L_{couple}. The ET-PA system is excited with different LTE signals of varying bandwidths (10, 20, and 40 MHz). The value of L_{couple} is varied and the IMD3 response at the output of the PA is measured, as shown in Fig. 45. It can be observed that PA linearity degrades severely with higher envelope bandwidths and for increased values of L_{couple}. In addition to the coupling inductor, the nonideal effects of wirebonds, pad capacitances, and printed circuit board (PCB) routings have a detrimental impact on the ET-PA system performance. For wideband applications, these parasitics become the bottleneck for operating bandwidth. These effects can be minimized by implementing a fully integrated single-chip ET-PA system or integrating the SM and PA on a multichip module package with advanced packaging techniques [135], [136], at the expense of higher cost and potentially lower assembly yield.

5) Variation in PAs Optimum Load Impedance: A linear PA is designed for an optimum load impedance (Z_{opt}) that is typically found through load-pull simulations/measurements. et al. [127] prove that the value of Z_{opt} does not remain constant and changes with the PAs V_{DD} supply in an ET operation. This effect is more pronounced for wideband systems, where the value of Z_{opt} can vary significantly over the range of instantaneous operating frequencies, thus complicating the design of the PAs output matching network. Incorrect matching degrades the PA efficiency and limits the maximum power that can be delivered to the load. Furthermore, variation in the Z_{opt} value leads to nonlinearity in the ET-PA system. Xia et al. [128] conclude that when different Z_{opt} values are presented to a PA, the PA exhibits varying AM–PM response. This variation was measured in [128] using a NMOS-input common-source differential PA architecture implemented in GlobalFoundries 45 nm SOI CMOS process, and the results are shown in Fig. 46. The need for dynamically variable matching networks has driven developments in tunable on-chip matching techniques and passive structures [129], [130].

6) Heat Management: The management of heat is a another major challenge for the ET-PA system. Since the PA dissipates significant power, the unused energy in the form of heat can lead to impaired linearity, reduced effective power density, and the heat affects the SM performance [137]. In integrated ET-PA systems, catastrophic failure may occur due to self-heating, especially under m ismatch conditions typically occurring in the mobile user equipment environment [138]. Therefore, significant design consideration must be given to power density, thermal dissipation techniques through the substrate, assembly materials for die attach and bonding to the substrate, and grounding techniques, as heat sinks are not available in mobile handsets due to limited area (unlike base stations).

Many of the discussed ET-PA interface problems can be eliminated by implementing a fully integrated single-chip ET-PA system, but single-chip implementations face another set of challenges, including noise coupling, large die areas, thermal dissipation, monolithic integration of the passive devices, and nonoptimal choice of process technology for either the SM or PA that leads to reduced RF performance. To-date, single-chip implementations have generally not achieved the efficiency and output power performance of multichip module implementations.

IX. Conclusion

ET techniques provide a solution for improving the efficiency of a PA system under power back-off conditions. One of the major benefits of ET is its compatibility with handset applications, which makes it amongst the most popular efficiency enhancement techniques and the most widely implemented enhancement technique to-date.

This work reviews the HSM, which is the most popular SM architecture for implementation of ET-PA systems. This article summarizes the HSMs theory of operation, categorizes the various HSM architectures, and details the advancements in HSM topologies for maximizing HSM performance. The state-of-the-art HSM implementations are thoroughly compared

in Table IV with respect to the achieved performance. Finally, the challenges for ET-PA system implementation and integration of the SM with PA are highlighted in Section VIII.

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Dr. Kitchen was a recipient of a DARPA Young Faculty award in research advancements on digital transmitters, and her work in power converters and amplifiers has been recently recognized through an NSF CAREER award.