Low Phase Noise Oscillator Design Using Degenerate Band Edge Ladder Architectures

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***Abstract*—A new approach based on a strong degeneracy state to design oscillators that exhibit low phase noise and low power consumption is presented. A 100-MHz oscillator is designed using a periodic structure based on a degenerate band edge that is augmented with an NMOS cross-coupled pair. The analysis and simulation results show 16 dB phase noise improvement compared to oscillators based on a conventional single-ladder periodic structure. It is also shown that this oscillator dissipates less power than a conventional LC oscillator that requires a buffer to drive a 50Ω load.**

***Index Terms*—Oscillator, phase noise, periodic structures, energy efficiency, distributed amplifiers.**

I. Introduction

OSCILLATORS are essential blocks used in a variety of mixed-mode or RF systems. These oscillators are typically implemented using an LC tank with positive feedback [1]–[2] or through a ring architecture [3]–[4]. In kHz and MHz frequency ranges, oscillators are normally implemented using a resonant crystal or an RC relaxation circuit [5]–[6]. Designing oscillators with low phase noise is always a main concern in mixed-mode and RF circuits. Periodic structures known to exhibit low phase noise include distributed oscillators [7], substrate integrated waveguides (SIW), and microwave structures [8]–[12]. These structures are usually modeled using a standard LC ladder topology.

The concept of a degenerate band edge (DBE), which is a strong degenerate state realized by a special type of double-ladder periodic structure [13]–[15], has been shown to have the potential to achieve a higher Q-factor, which in turn results in lower phase noise as compared to oscillators realized by a more conventional periodic structure. In this brief, a DBE circuit topology is presented in Section II. Then, the frequency-domain admittance of such a periodic structure is studied to identify the criteria for oscillation in Section III. Following the mathematical concepts developed in [16], the oscillator is implemented using the DBE structure and a cross-coupled pair that realizes a negative conductance implementation as described in Section IV. Simulation results showing phase noise and power consumption are also presented in this section to show the advantages of employing the DBE architecture in an oscillator design.

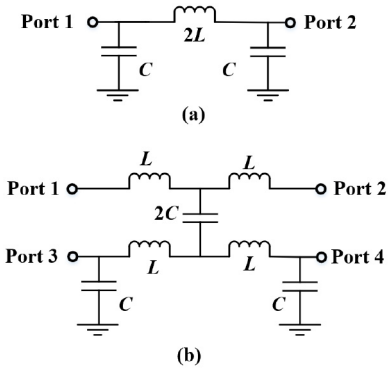

Fig. 1. Ladder periodic circuits. (a) Symmetrical single-ladder unit cell. (b) Symmetrical double-ladder unit cell exhibiting a DBE. These two infinitely long ladders have the band edge at the same frequency $f_d = 1/(2\pi\sqrt{LC})$, but the double ladder exhibits a degenerate band edge [15].

II. Degenerate Band Edge Structures

As described in the previous section, single-ladder periodic structures have been demonstrated to realize oscillator architectures that achieve higher Q factors than conventional LC or ring oscillators. The unit cell of such a structure is shown in Fig. 1(a). These structures, which are normally implemented using either waveguides or lumped elements, consist of a number of such unit cells connected in tandem. In contrast with normal single-ladder periodic structures, double-ladder periodic structures exhibit a DBE and can realize an even higher Q factor. Following [15], a symmetrical DBE unit cell is shown in Fig. 1(b) with the same L and C values as in the Fig. 1(a) circuit. Fig. 2(a) shows a number of DBE unit cells connected in tandem, where series inductors and parallel capacitors have been combined. In order to realize an oscillator based on this passive structure, an active circuit should be added, which is described in the next section.

III. DBE Oscillator Implementation

A. Driving Admittance in DBE Double Ladder Architecture

Due to the loss in the components that make up the DBE double-ladder structure, an active circuit is required to create

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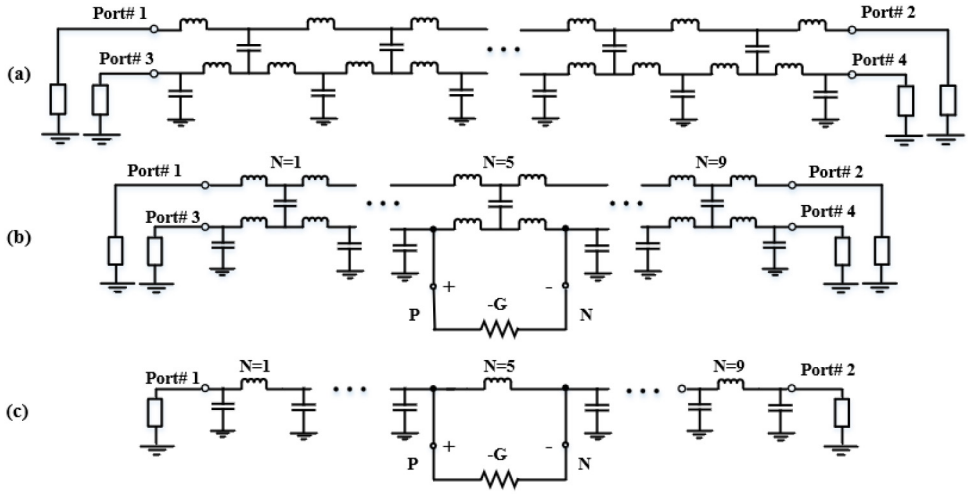

Fig. 2. (a) DBE periodic structure model (series inductors and parallel capacitors have been combined). (b) DBE double ladder oscillator architecture. (c) Single ladder oscillator.

a net negative conductance that can overcome the total loss. Such loss at the resonant frequency can be determined by observing the real part of the driving admittance between the two nodes at which the negative conductance will be connected, at the frequency where the imaginary part crosses zero.

The DBE structure has unit cell parameters of $L = 45$ nH and $C = 56$ pF, with equivalent series resistances of $R_L = 180$ mΩ and $R_C = 60$ mΩ, corresponding to $Q_L = 150$ and $Q_C = 470$, respectively, at the resonant frequency of 100 MHz. These components are selected from available off-chip lumped elements [18], [19]. The double ladder consists of nine unit cells with Ports 1 and 2 terminated with 50 Ω and Ports 3 and 4 open-circuited. For the case where the negative conductance is connected across the middle cell, as shown in Fig. 2(b), a sweep of the driving-point admittance over frequency is shown in Fig. 3(a). The real part of the driving admittance around 100 MHz (corresponding to the circuit's resonant frequency, where the imaginary part vanishes) indicates that the minimum negative conductance of 660μS will be required to meet the oscillation criteria. This is less than half of what would be required for the single-ladder oscillator Fig. 2(c), using the same unit cell parameters, as indicated in Fig. 3(b), which exhibits a resonant frequency similar to that of the Fig. 2(b) circuit.

A set of similar frequency-domain simulations were performed with the negative conductance connected across each unit cell in Fig. 2(b). Fig. 4 shows the driving-point admittance at the resonant frequency corresponding to each of those simulations. It is observed that the minimum amount of negative conductance needed for oscillation occurs when the negative conductance is connected to the middle of the structure.

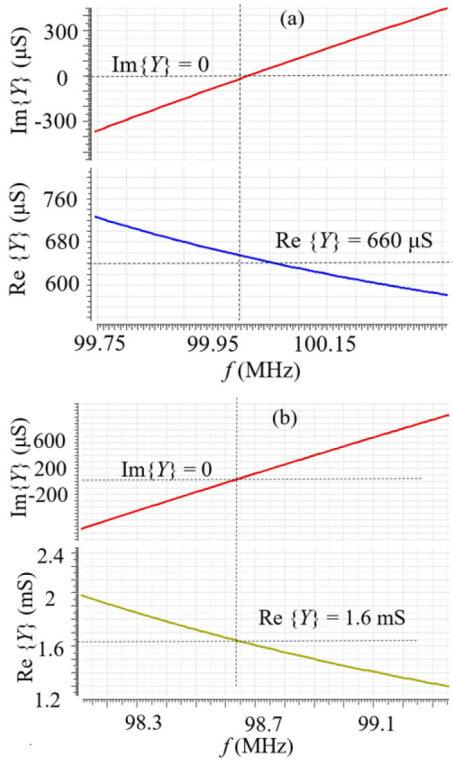

Fig. 3. Real and imaginary parts of driving admittance, to determine the required negative conductance between points P and N in Fig. 2, for the (a) DBE double-ladder architecture and (b) equivalent single ladder.

B. Nonlinear Negative Conductance

Negative conductance architectures are normally implemented using positive feedback realized by active devices. Among different architectures, a conventional NMOS cross-coupled pair shown in Fig. 5(a) is a straightforward approach. The tail current source provides the biasing for the cross-coupled pair, which determines the small-signal negative conductance. In large-signal operation, the negative conductance starts to degrade as one of the transistors moves into the triode region. Finally, when the differential signal is sufficiently large, one of the devices turns off. In this region, the cross-coupled pair behaves like a current source. This behavior is illustrated by the dc sweep simulation shown in Fig. 6 where the active circuit is implemented using TowerJazz

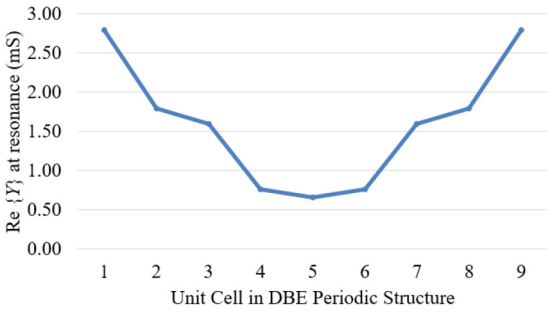

Fig. 4. Real part of the admittance at resonance evaluated corresponding to each unit cell of the bottom ladder Fig. 2(b). The central unit cell, i.e., between points P and N, exhibits the minimum conductance.

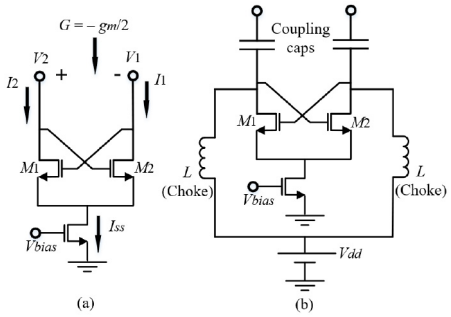

Fig. 5. (a) Nonlinear negative conductance implementation using cross-coupled pair. (b) Proposed biasing scheme for the negative conductance circuit connecting to DBE structure.

sbc18h BiCMOS N-channel devices with 1.8 V and 700 μA supply voltage and bias current, respectively.

IV. Degenerate Band Edge Oscillator Architecture

A. Circuit Implementation

As discussed in the previous section, connection of the negative conductance, implemented using the circuit in Fig. 5(b), to the middle DBE unit cell [Fig. 2(b)] will allow for the smallest value of negative conductance in order for oscillation to occur. The off-chip chokes are employed to DC bias the cross-coupled pair. In addition, a pair of off-chip coupling capacitors are used to decouple the DC biasing from the periodic structure. Their values are chosen to be 100 nF so that they behave almost as short circuits at the oscillation frequency. The oscillation transient waveforms for three different pairs of termination loads on Ports 1 and 2 – open circuit, 50Ω, and 25Ω – are shown in Figs. 7(a) and (b). It is observed that the oscillation amplitude is only weakly dependent on the termination resistance connected at Ports 1 and 2, while in the single-ladder oscillator case the oscillation amplitude decreases significantly as the termination resistance is decreased, as shown in Fig. 8.

The optimum number of unit cells in the circuit is determined by two factors: Minimizing the amount of negative conductance required for oscillation, and minimizing the sensitivity of the output amplitude to the termination resistance. For lossless inductors and capacitors, a higher number of cells will exhibit behavior closer to the ideal DBE theory. On the other hand, when losses in the inductors and capacitors are present, having too many unit cells will increase the total loss to the point where the oscillation amplitude at the loads begins to decrease; moreover, in this case there will also be more sensitivity in the oscillation amplitude to the termination resistance. These trade-offs are illustrated in two ways: Fig. 9(a) shows the minimum negative conductance required

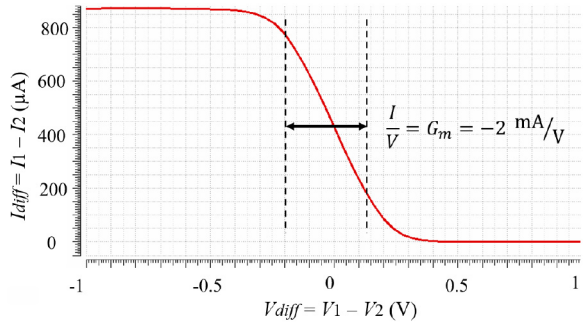

Fig. 6. Nonlinear negative conductance from cross-coupled pair differential I-V Curve.

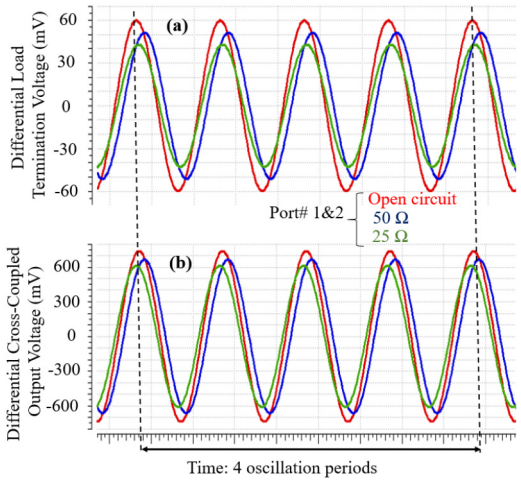

Fig. 7. DBE oscillator's terminal transient signal for different load impedance values. This result shows how stable is the output amplitude to large load variations.

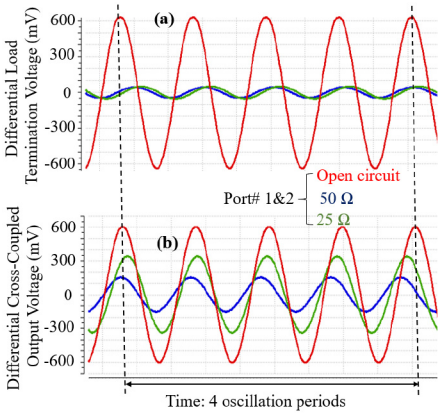

Fig. 8. Single-Ladder oscillator's terminal transient signal for different load impedance values. In contrast to the DBE double-ladder architecture, this result shows how unstable is the voltage output to large load variations.

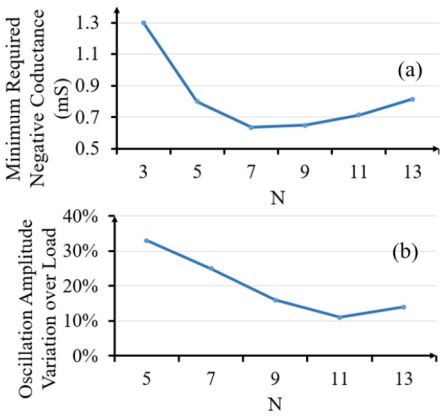

Fig. 9. (a) Real part of the admittance at resonance seen at the central unit cell evaluated for different unit cell numbers. (b) Oscillation amplitude variation in % from 50 Ω to 25 Ω at termination load normalized to 50 Ω load oscillation amplitude.

for oscillation versus number of cells. Fig. 9(b) shows the relative amplitude sensitivity to the load resistance, defined as the percentage change in amplitude that occurs when the load resistance is decreased from nominal 50Ω to 25Ω, versus the number of cells. An odd number of unit cells was used in all cases in order to provide symmetry in the circuit. From the graphs in Fig. 9 it can be observed that seven cells were optimum with respect to the minimum required negative conductance, while eleven cells were optimum with respect to load sensitivity. Thus nine unit cells were used in the final design to provide a balance between the two constraints.

B. Advantages of DBE Oscillators

In addition to the lower sensitivity to load variation, the advantages of using the proposed DBE architecture to realize an oscillator include lower phase noise and lower power dissipation. Because a DBE double-ladder structure in general exhibits a higher Q-factor compared to a single-ladder structure with the same unit cell parameters and load terminations, the DBE-based oscillator exhibits improved phase noise. However, the high Q-factor is probably not the only reason since as shown in analogous optics studies in [17], a DBE cavity exhibits a lower lasing threshold than other types of cavities that have a similar Q factor. The results of a phase noise simulation, under the condition that ports 1 and 2 are both terminated with 50 Ω, for both the DBE double-ladder oscillator (with ports 3 and 4 open) and the single-ladder oscillator, are shown in Fig. 10. A nearly 16 dB phase noise improvement is observed at offset frequencies below 100 kHz.

To study how variations in the values of the resonator elements affect the oscillation frequency and phase noise of the proposed architecture, Monte Carlo simulations were run on the circuit where the inductor and capacitor values were randomly perturbed. These perturbations had a Gaussian distribution with standard deviation (σ) of 1%. The histogram plots of oscillation frequency and phase noise variations over 500 random samples are shown in Figs. 11(a) and (b), respectively. A symmetrical Gaussian distribution with standard deviation of 0.27% can be observed for the oscillation frequency, indicating reduced sensitivity to the resonator random variation

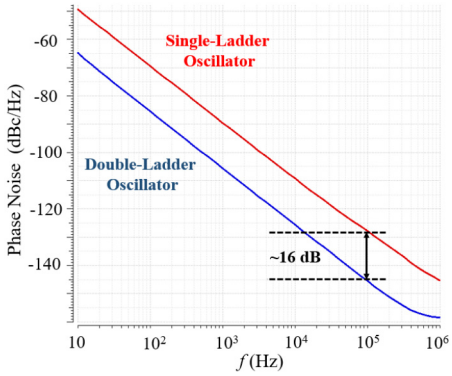

Fig. 10. Phase noise comparison. The DBE double-ladder oscillator leads to lower phase noise than the single-ladder oscillator.

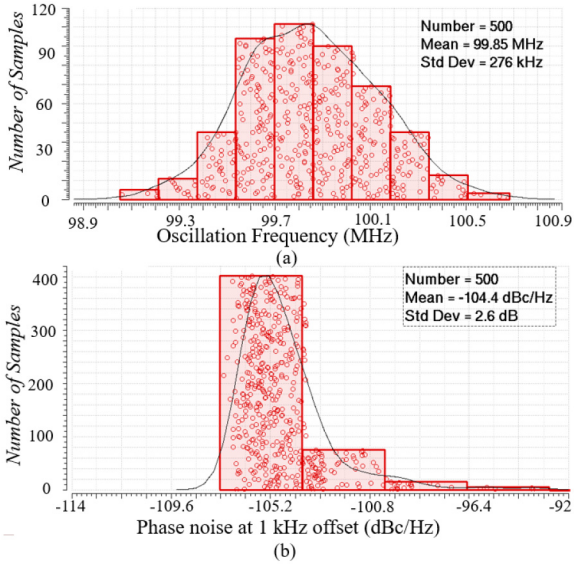

Fig. 11. Histogram plots showing the effect of resonator elements variation (σ = 1%) on DBE oscillator parameters: (a) oscillation frequency (σ = 0.27%), (b) phase noise at 1 kHz offset (σ = 2.6 dB).

due to the large number of resonator elements. Simulations also show that most perturbations in the inductor and capacitor values increase the phase noise, which results in a nearly one-sided Gaussian distribution with standard deviation of 2.6 dB around the nominal value. It was also found from simulations (not shown here) that a $+/-10\%$ mismatch between the cross-coupled transistors results in no more than $+/-5$ ppm change in the oscillation frequency and less than 0.05 dB change in the phase noise.

Another significant advantage of using the DBE structure is that the oscillation signal can be delivered directly to the load termination without the need for a buffer, thereby reducing the power dissipation. In a conventional LC oscillator implementation, it is not possible to connect the termination resistances directly to the outputs without dissipating excessive power; hence one or more buffer stages are required to drive the 50 Ω termination. To achieve a 100 mV peak-to-peak oscillation amplitude at the load, a typical current-mode logic (CML) buffer with a 50 Ω termination resistance requires a tail current of at least 1 mA in the last stage in order to drive a 50 Ω output

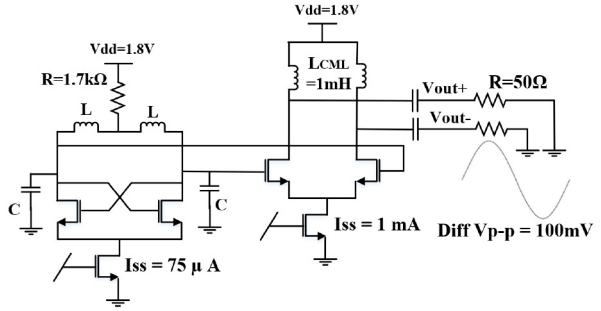

Fig. 12. Current-mode logic (CML) buffer used for load termination of conventional LC oscillator architecture.

TABLE I
COMPARISON OF CURRENT CONDUCTED FOR THREE DIFFERENT OSCILLATOR CONFIGURATIONS. ALL CONFIGURATIONS OPERATE FROM A SINGLE SUPPLY $V_{DD} = 1.8$V

Oscillator	Negative Gm Current	Buffer Current	Total Current	No. of resonator elements
Double-ladder	0.7 mA	-	0.7 mA	47
Single-Ladder	0.74 mA	-	0.74 mA	19
Conven. LC	0.075 mA	1 mA	1.075 mA	6

termination resistance as shown in Fig. 12. On the other hand, the DBE-based oscillator achieves the same amplitude without buffering and thus the only current conducted from V_{DD} is the 700 μA bias current in the negative conductance circuit shown in Fig. 5(b). The details of this comparison are presented in Table I. The resonator parameters are the same in all comparison cases: $L = 45$ nH and $C = 56$ pF, which include equivalent series resistance of $R_L = 180$ mΩ and $R_C = 30$ mΩ corresponding to $Q_L = 150$ and $Q_C = 500$, respectively, at the 100 MHz resonant frequency.

V. CONCLUSION

A new architecture has been introduced to design oscillators with low phase noise that do not require buffers for driving an external load. The method is based on using double-ladder periodic structures with a degenerate band edge (DBE). The resonator is modeled by lumped element parameters to introduce the theoretical concept and show the possible advantages. The oscillation criteria show smaller required negative conductance as well as approximately 16 dB phase noise improvement compared to a single-ladder oscillator, and 4 times reduced sensitivity of oscillation frequency to the resonator elements random variation. The DBE oscillator has an output amplitude that exhibits small dependence on the termination load, and consumes less current compared to a conventional LC oscillator with a 50 Ω load CML buffer.

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