

Compact atto-joule-per-bit bus-coupled photonic crystal nanobeam switches

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ABSTRACT

The benefits of photonics over electronics in the application of optical transceivers and both classical and quantum computing have been demonstrated over the past decades, especially in the ability to achieve high bandwidth, high interconnectivity, and low latency. Due to the high maturity of silicon photonics foundries, research on photonics devices such as silicon micro ring resonators (MRRs), Mach-Zehnder modulators (MZM), and photonic crystal (PC) resonators has attracted plenty of attention. Among these photonic devices, silicon MRRs using carrier depletion effects in p-n junctions represent optical switches manufacturable in the most compact magnitude at high volume with demonstrated switching energies ~ 5.2 fJ/bit. In matrix multiplication demonstrated with integrated photonics, one approach is to couple one bus straight waveguide to several MRRs with different resonant wavelengths to transport signals in different channels, corresponding to a matrix row or column. However, such architectures are potentially limited to ~ 30 MRRs in series, by the limited free-spectral range (FSR) of an individual MRR. We show that PC switches with sub-micron optical mode confinements can have a FSR > 300 nm, which can potentially enable energy efficient computing with larger matrices of ~ 200 resonators by multiplexing. In this paper, we present designs for an oxide-clad bus-coupled PC switch with 1 dB insertion loss, 5 dB extinction, and ~ 260 aJ/bit switching energy by careful control of the cavity geometry as well as p-n junction doping. We also demonstrate that air-clad bus-coupled PC switches can operate with 1 dB insertion loss, 3 dB extinction, and ~ 80 aJ/bit switching energy.

Keywords: Photonic crystal, nanocavity, quality factor, energy consumption, doping concentration

1. INTRODUCTION

With the growing global application of semiconductor chips, the demand for performing computations and data processing on compact and energy-efficient form factors is increasing exponentially. Optical computing is enabled by electro-optic (EO), thermo-optic (TO) and acousto-optic (AO) modulations which make it possible to transport data at the speed of light. [1-4] In contrast to electrons propagating down a copper wire on an electronic chip, optical waveguides can guide light and hence data on several orthogonal wavelengths at the same instant of time thereby greatly increasing the data bandwidth. Low energy consumption is an important requirement for practical optical interconnects. Reducing both the loss in passive components and the operating energy in active components of an optical data link are being explored in the photonics community. Traveling wave MZM provides the highest electrooptic bandwidth and great tolerance to manufacturing errors, temperature changes, and laser wavelength drifts. However, from the perspective of energy-efficiency and compact form factors, the micro ring resonator modulator is the current go-to device in the silicon photonics community. MRR switches can be exceedingly small, highly energy efficient with low loss, and can perform data modulation at high speed. [5] Photonic crystal (PC) nanocavities with sub-micron optical mode volumes however promise the potential for even denser integration and more than an order of magnitude better energy efficiency than MRR. [6-7]

PC cavities have demonstrated numerous advantages over other cavity resonator structures due to their ability to confine an optical mode in subwavelength-scale mode volumes and quality factors (Q-factors) approaching several million on a silicon chip. [6-7] Photonic devices on-chip should be compact and energy-efficient and perform a conversion from the radio-frequency (RF) signal to the optical domain, or switch light from one channel to another, with as little an energy as possible. Since the power required to switch one bit is dependent on both the optical mode volume overlapping with the dielectric in which change of refractive index occurs, and the magnitude of the refractive index change per unit transducing signal, minimizing either can reduce the energy required to switch from a high to a low, and vice-versa in any digital communication and computing circuit. A high Q-factor cavity together with a small mode volume (reaching sub-micron scales in a PC cavity) is thus extremely beneficial as it reduces the transducing energy required to cause an optical index

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change for compact, energy-efficient photonic switch applications. PC cavities with top cladding silicon dioxide or air and bottom cladding silicon dioxide are designed here to identify the optimal switch with the lowest switching energy.

2. THEORY

2.1 Bus-coupled Photonic Crystal Nanobeam Switch

Photonic crystals are periodic dielectric structures in which the periodic modulation of the refractive index gives rise to allowed and forbidden photonic energy bands. Gaps in the photonic band structure of the photonic crystal correspond to frequencies (wavelengths) at which photons are forbidden to propagate in certain directions. The introduction of a defect in the perfect periodic lattice gives rise to in-gap defect states where light is trapped (in the case of a photonic crystal microcavity (PCM)) or propagates via Bloch confinement (in the case of a photonic crystal waveguide (PCW)). The present research demonstrates 1D PCMs where light is confined by a 1D periodic array of holes etched in silicon along the linear axis of the cavity and by total internal reflection (TIR) in the other two orthogonal directions.

Introduction of a defect in the perfect lattice of a PC gives rise to defect states in the photonic band gap in which light is confined to sub-micron mode volumes. Our nanocavity design comprises a row of elliptical air holes etched in a single mode silicon waveguide whose major radii are quadratically decreased from a large radius at the center to smaller radius at the two sides symmetrically. The inline nanobeam cavity is shown in Figure 1(a) and is contrasted with the bus-coupled photonic crystal nanobeam structure (Figure 1(b)) used in this paper. In the inline configuration, the resonator resonance is transmitted through the PC cavity while other wavelengths are reflected. [6-7] In the bus-coupled-cavity nanobeam configuration, the resonance wavelength of the coupled cavity is dropped from the wavelengths transmitted in the bus leading to a dip in the transmission spectrum. [10-11]

The Q-factor demonstrates the ability of the cavity to confine and store light. A higher Q-factor means a better confinement of the resonant light and more energy stored in the cavity with less loss. There is a trade-off between the resonance linewidth and the cavity lifetime. If the Q-factor is too high, the photon storage time in the PC cavity is increased, which compromises the modulation speed of the device. If the Q-factor is too low, larger shifts of the resonance wavelength are required to allow measurable change from a transduction event. In an inline PC nanobeam cavity as shown in Figure 1(a), the Q-factor is a result of the intrinsic Q-factor from the radiative loss into free space, effects of scattering loss at material and physical boundaries and bulk material absorption loss. For a bus-coupled PC nanobeam structure as shown in Figure 1(b), an extra component to the effective Q-factor is the bus waveguide-cavity coupling related Q-factor which is dependent on the dimensions of the bus, the gap between the bus waveguide and the cavity, as also on the refractive index of the material filling the gap.

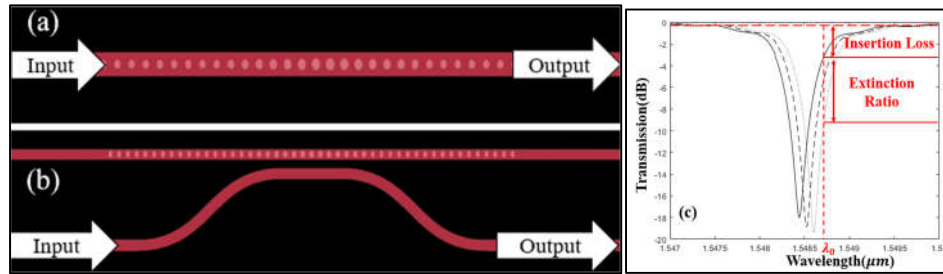


Figure 1. (a) Inline etched and (b) Bus-coupled photonic crystal structure; (c) The definition of insertion loss and extinction ratio

The extinction ratio (ER) and insertion loss (IL) are two additional parameters to optimize as defined in Figure 1(c). In this paper, our designs try to achieve an optimized design with a target value IL ~1dB and ER ~5dB. The Q-factor and extinction of the resonance is optimized by changing the lattice constant and the hole radii and the number of mirror hole periods, as also the gap between the bus and the PC microcavity. Elliptical air holes are etched in silicon (that is, holes with different major and minor radii) to improve the resonance Q factor and extinction.

2.2 Doping distribution

In P-N junction doped E-O modulators, the EO modulation is based on the carrier plasma dispersion effect. The carriers are either injected into the active area (carrier injection approach) or removed from the active area (carrier depletion

approach). Each approach has its own advantages and drawbacks. The carrier injection approach enables lower switching voltage since the switching operation is dependent on the minority carrier injection and removal process which makes it more efficient to change the refractive index of the active area, compared with the carrier depletion approach. In contrast, the carrier depletion approach is a majority carrier limited process and thus devices utilizing carrier depletion can perform at faster speeds (~ 50 Gbps) [12] than the carrier injection approach (< 5 Gbps) [13] due to the smaller majority carrier lifetimes (picoseconds) than minority carriers (nanoseconds). The carrier depletion approach is adapted in this design to reach a higher switching speed. Carrier depletion resonator modulators and switches also have larger Q-factors (due to reduced free carrier absorption losses) and have smaller switching energies (due to reduced capacitance) than the carrier injection type devices.

For the PN junction with N_D denoting N-type doping concentration and N_A denoting P-type doping concentration, the built-in voltage is $V_{bi} = V_t \ln \left(\frac{N_D N_A}{n_i^2} \right)$ where n_i is the intrinsic concentration of silicon. In forward bias, the depletion region is narrowed with increasing bias. In contrast, reverse bias increases the built-in potential barrier and widens the depletion region. The total width of depletion region is given by $W = \sqrt{\frac{2\epsilon_0\epsilon_r}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_{bi} - V_a)}$ where ϵ_0 is the permittivity of free space, ϵ_r is the dielectric constant of silicon, V_a is the applied bias voltage. The depletion region width in the P-type region X_p and in the N-type region X_N are determined by $X_p = W \left(\frac{N_D}{N_A + N_D} \right)$ and $X_N = W \left(\frac{N_A}{N_A + N_D} \right)$ respectively. As the applied bias changes, the width of the depletion region changes and thereby changes the concentration of free electrons (ΔN_D) and holes (ΔN_A). From the seminal paper by Soref et al. [14], the index change caused by free holes is up to 3.3 times of the index change by free electrons at the concentration $\sim 10^{17} \text{cm}^{-3}$. Carrier concentrations at least in $10^{17} \sim 10^{18} \text{cm}^{-3}$ magnitude range is desired to obtain a substantial refractive index change. The change in refractive index versus free carrier concentration is given by

$$\Delta n = -8.5 \times 10^{-22} (\Delta N_A)^{0.8} - 8.8 \times 10^{-22} (\Delta N_D)^{1.05}$$

Higher doping concentrations lead to higher change of refractive index but also increase loss due to free carrier absorption. A high change in the refractive index leads to larger resonance wavelength change while an increase in free carrier absorption loss leads to lower resonance Q-factors. Hence choosing an appropriate doping profile and concentration requires a balanced performance between resonator Q, extinction, and index change.

3. DESIGN

Nanocavity Design

The cavity is made by etching a periodic array of holes in a silicon waveguide with width 438nm and height 220nm. The period (a) or lattice constant of the array is set as $a=365\text{nm}$ to achieve device operation in the telecom-friendly $\lambda \sim 1550\text{nm}$ wavelength range. As shown in Figure 2, there are two groups of etched holes. The center group defines the resonant cavity where the hole radii gradually taper down from the center of the cavity ($r = 0.3a$) to ($r = 0.22a$) symmetrically over 8 periods to the two ends. On each end of the taper region, the cavity mirror is formed by an array of holes with the same radii. The mirror holes are kept as $r = 0.22a$. The taper region and mirror regions together form the nanocavity with resonant optical modes confined in the center. The resonance Q-factor increases with the number of mirror holes on each side of the nanocavity till about 15 mirror holes beyond which the effect is not significant.

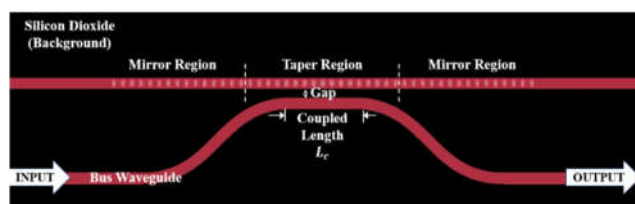


Figure 2. Schematic design of bus-coupled waveguide PC cavity

Figure 3(a) shows the defect cavity mode of the oxide-clad PC cavity geometry where the mode antinodes are preferentially located in the high index silicon regions. The corresponding spectrum with the resonant wavelength is shown in Figure

3(b). The transmission spectra are simulated by the three-dimensional (3D) finite-difference-time-domain (FDTD) simulations in Ansys/Lumerical FDTD.

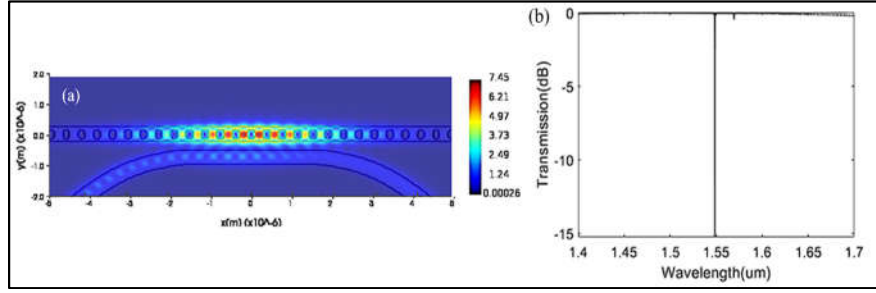


Figure 3. Simulated results for oxide-clad PC cavity of (a) confined mode profile in z-normal cross-section; (b) transmission spectrum with lattice constant 365nm and gap 350nm

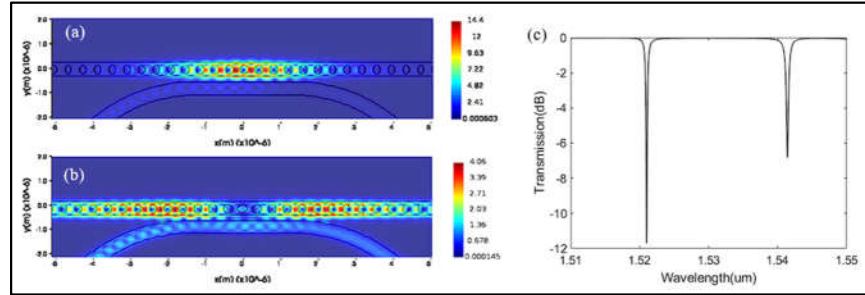


Figure 4. Simulated results for air-clad PC cavity of (a) the confined mode profile of first resonance in z-normal cross-section; (b) second resonance in z-normal cross-section; (c) transmission spectrum with lattice constant 385nm and gap 150nm

We also designed an air-clad PC cavity with a bottom oxide-cladding, as shown in Figure 4. According to the spectrum shown in Figure 4(c), there are two resonant wavelengths for the air-clad PC cavity resonator. The first resonant mode at wavelength ($\lambda \sim 1521\text{nm}$) is preferentially in the silicon in the carrier modulation region which extends $\sim \pm 1\mu\text{m}$ from the center of the nanocavity, as shown in Figure 4(a). The second mode at wavelength ($\lambda \sim 1542\text{nm}$) is confined in the etched holes in the carrier modulation region as shown in Figure 4(b). The doping profile and hence the dimensions of the carrier modulation region is selected to optimize the influence of free carriers on the cavity Q-factor. The second resonance has negligible overlap with the carrier modulation region of the nanocavity. Therefore, the second resonant shifts negligibly with the change of applied voltage to the cavity. It was observed that use of elliptical holes instead of circular holes could also help to optimize designs that minimized the second resonance. The major axis radii of all the elliptical holes are identical in the -y direction, which is $0.4a$. In addition, device optimized designs also modify the gap between the silicon bus waveguide and the silicon cavity.

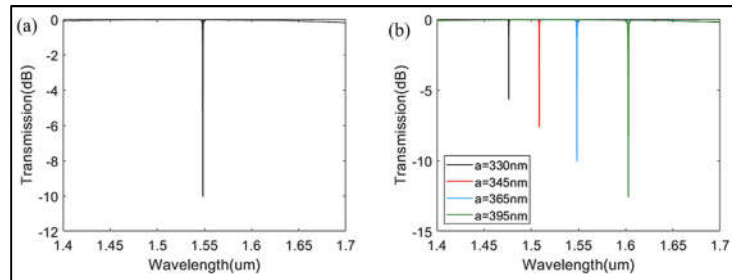


Figure 5. The simulated transmission spectrum for bus coupled oxide-clad p-n doped PC switch with gap of 350nm in a wide range from $1.4\mu\text{m}$ to $1.7\mu\text{m}$ (a) with lattice constant of 365nm; and (b) with lattice constant varied from 330nm to 395nm

Doping concentrations and profiles are designed using Multiphysics simulations in Lumerical CHARGE with electrodes mounted at the extreme ends of the PC microcavity. The second resonance mode that was observed in the transmission spectrum of the air-clad PC nanocavity can also be observed with an extinction $\sim 0.1\text{dB}$ in the transmission spectrum of the oxide-clad PC nanocavity at $\lambda \sim 1570\text{nm}$. However, the second resonance mode is not observable for the doped PC bus-coupled oxide-clad nanocavity. Fig. 5(a) also shows a large free spectral range (FSR), which thus indicates feasibility of multiplexing several PC resonators in series. The doped structure reduces the ER by $\sim 5\text{dB}$ compared to the undoped cavity in Fig. 3(b). Figure 5(b) shows the simulated transmission spectrum when multiplexing several PC nanocavities in a circuit by tuning the lattice constant of each cavity. It is also observed that the ER increases with the increasing lattice constant.

3.2 Doping Profile Design

The doping profile and concentration influence the wavelength shift of the transmission resonance by changing the refractive index of the central taper region. An ideal doping profile is one which results in the largest change in the depletion region, potentially covering the entire available waveguide cross-section, for the smallest bias voltages that leads to a largest wavelength shift. However, a large dQ implies a large $C = dQ/dV$ and hence a larger capacitance which thus translates to a larger energy-per-bit requirement. The electrodes are situated outside of the mirror region.

A gradient doping concentration is utilized to ensure a low resistance biasing. Figure 6 shows the 3D schematic of the doping profile, where the P-type doping is represented by yellow, and the N-type doping is represented by purple. Note that the boundary of the taper region and the mirror region is at $x = \pm 2.92\mu\text{m}$ ($8a$) and the mirror holes end at $x = \pm 8.6\mu\text{m}$ ($8a + 15a = 23a$). Under the electrodes, maximum doping concentrations for both N-type and P-type $\sim 1 \times 10^{19}\text{cm}^{-3}$ is considered to ensure low contact resistance. The structure is doped over a $2\mu\text{m}$ width centered on the center hole. The doping concentration in this modulation region is kept at $1 \times 10^{18}\text{cm}^{-3}$ for N-doping and $5 \times 10^{17}\text{cm}^{-3}$ for P-doping. The simulations assume a constant doping profile within their respective boundaries.

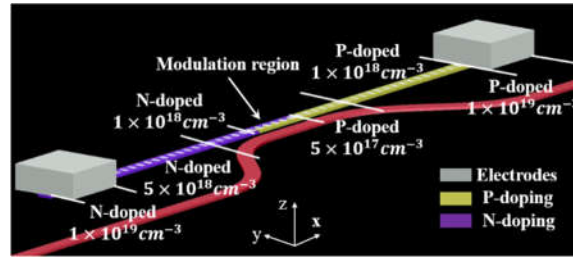


Figure 6. Schematic of the gradient doping concentration distribution

Assuming that the PC holes are etched in the y - z plane, (with the cavity defined along the x -axis), an U-shape junction is formed by sandwiching a P-doped region between 2 N-doped regions in the vertical plane, normal to the waveguide transmission axis. U-junctions have been experimentally demonstrated previously in the context of MRR modulation [15]. The doping profile with two (2) p-n junctions doubles the volume of the depletion region. With increasing applied voltage, the depletion region occupies a greater fraction of the available semiconductor volume till there can be no further increase of the depletion region. In our research, the p-doping region extends vertically from $+60\text{nm}$ to -60nm around the center of the cavity. The doping profile and the corresponding change in the carrier concentration profile are shown in Figure 7.

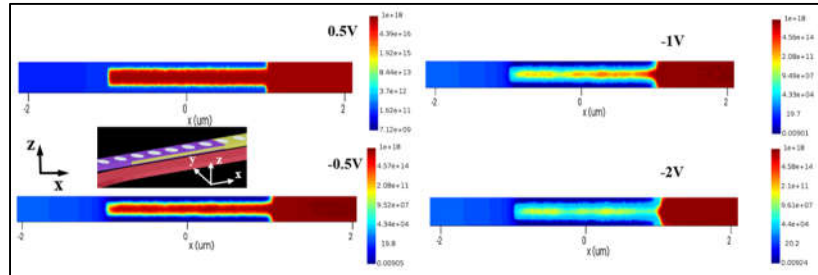


Figure 7. P-doping concentration profile in x - z plane of 0.5V, -0.5V, -1V, and -2V for U-shape vertical doping case with the PN junction interfaces located at $z = \pm 60\text{nm}$ (geometric junctions at $\pm 60\text{nm}$ from the center (along the vertical))

3.3 Cavity Optimization for low-energy switching

Figure 8 shows the wavelength shift when switching the applied bias from 0.4V to -0.5V for the bus-cavity coupling gap width of 350nm in an oxide-clad and an air-clad PC microcavity. A 5.3dB extinction ratio and 1.2dB insertion loss is achieved for the oxide-clad PC nanocavity. The extinction ratio for air-clad cavity is ~3dB with an insertion loss ~1dB.

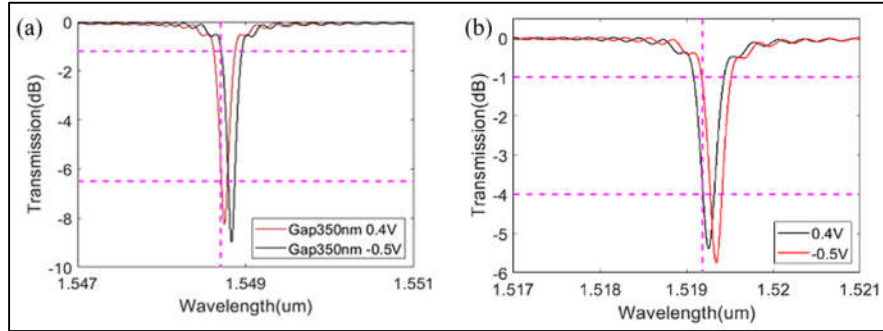


Figure 8. U-junction design for (a) oxide-clad PC cavity with gap width of 350nm and lattice constant of 365nm, with 1.2dB insertion loss and 5.3dB extinction loss for a voltage swing from 0.4V to -0.5V. (b) air-clad PC cavity with gap 200nm and lattice constant of 385nm

The average energy consumption is given by $E = \frac{1}{2}E_s = \frac{1}{4}(C_1V_1^2 + C_2V_2^2)$, where E_s is the switching energy, V_1 and V_2 are the switching boundary voltages, C_1 and C_2 are the capacitance of the structure at the corresponding voltages respectively. Figure 9 presents the capacitance for oxide-clad and air-clad PC cavities respectively. In forward bias, the capacitance increases with increasing voltage. Figure 9 (a) shows an inflexion at applied voltage around -1.5V, where the capacitance would not change too much with the increased reversed bias since the carriers are already depleted from the semiconductor slab. Based on this property and the fact that the energy consumption is related to the product of capacitance and square of the voltage, a voltage range centered on 0V is considered to ensure enough wavelength shift with a low energy consumption. Since the capacitance is proportional to the dielectric constant, the air-clad PC cavity has a lower capacitance compared with the oxide-clad PC cavity of the same geometry, as shown in Figure 9(b), leading to a switching energy as low as ~80.7aJ/bit. In contrast, the switching energy is 262.25aJ/bit at the operating wavelength of 1548.7nm for the oxide-clad PC nanocavity. Further simulations and experiments are in progress to optimize the design for the air-clad PC cavity to achieve the same extinction ratio and insertion loss as the oxide-clad PC cavity.

From the doping profile, the calculated change of junction capacitance ΔC is ~3fF when switching was from -0.5V to 0.5V for oxide-clad and ~1.2fF when switching was from -0.5V to 0.4V for air-clad. By applying a linearization of the resistance and capacitance changes over the range of applied voltages [16], we calculated $R_{eff} = \frac{(R_{min} + R_{max})}{2} \approx \frac{(72k\Omega + 154k\Omega)}{2} \approx 113k\Omega$. From these values, the calculated 3dB switching frequency is ~1.34GHz for oxide-clad and ~3.35GHz for air-clad PC nanobeam cavity switch devices.

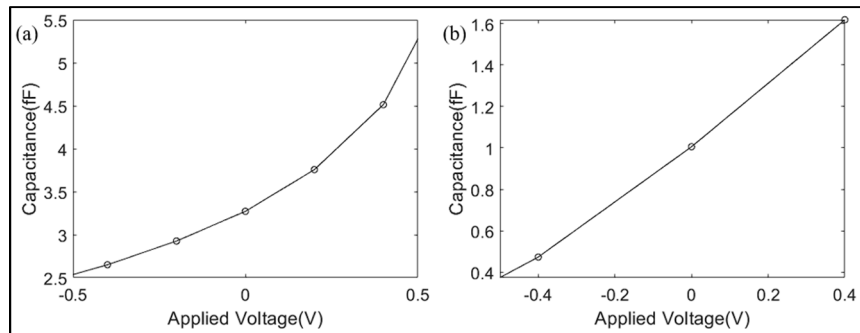


Figure 9. The simulated capacitance changing with the applied voltage for the U-junction doping profile structure of (a) oxide-clad PC cavity in the range of -0.5V to 0.5V and (b) air-clad PC cavity in the range of -0.5V to 0.4V

4. RESULTS

Scanning electron microscope (SEM) images of fabricated devices are shown in Figure 10 showing the array of PC air holes etched into silicon and tapering outward in radius from the central air hole. The PCs are covered with $\sim 5\mu\text{m}$ thick silicon dioxide in oxide-clad devices.

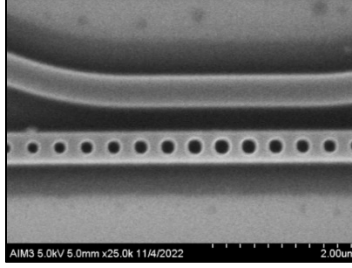


Figure 10. The 1D bus-coupled cavity design under scanning electron microscope (SEM)

The normalized experimental spectrum of oxide-clad PC cavity with lattice constant 365nm and gap 350nm is shown in Figure 11(a). The experimentally observed Q-factor is 5746 with extinction 15.7 dB at wavelength 1551.55 nm which matches very closely with the simulated design for the undoped oxide-clad PC nanocavity shown in Figure 3(b). Figure 11(b) shows the normalized spectrum for oxide-clad PC cavity with different lattice constant (355nm, 365nm, and 375nm), which demonstrates the potential possibility of multiplexing several PC microcavities in series in large matrix multiplication architectures. The spectrum of an air-clad PC cavity resonator with lattice constant 385nm and gap 150nm is shown in Figure 12. Two resonant wavelengths are observed experimentally, as seen from simulations.

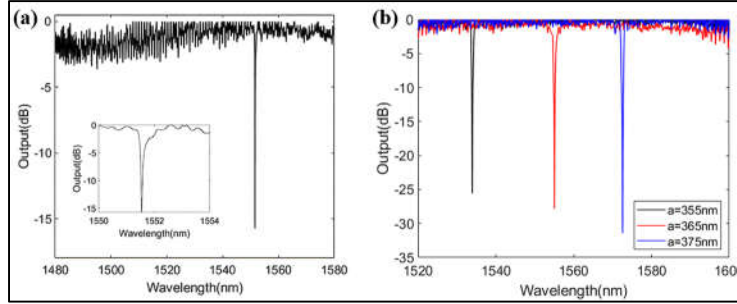


Figure 11. The normalized experimental transmission spectrum for the oxide-clad bus coupled PC switch with gap of 350nm for (a) undoped cavity with lattice constant of 365nm; (b) undoped cavity with lattice constant 355nm, 365nm, and 375nm

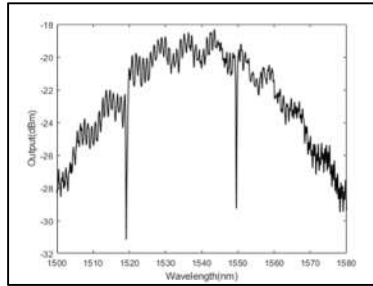


Figure 12. The experimental transmission for air-clad bus coupled PC switch with gap of 150nm and lattice constant 385nm

5. CONCLUSION

A compact high Q-factor, low energy consumed U-type p-n junction based EO switch is realized in an oxide-clad and oxide filled bus-coupled 1D photonic crystal nanocavity. While previous demonstrations were in passive structures [10]

with thermo-optic switching[11] or in air-clad carrier doped inline geometries in carrier injection [6] or carrier depletion modes [7], to our knowledge, this is the first design study of the oxide-clad bus-coupled 1D PC waveguide nanocavity switch using carrier depletion electro-optic effect for electro-optical switching applications. Together with large FSR(>300nm), our compact resonators can achieve high Q (~6,000), low insertion loss (~1dB), large extinction ratios (~5dB), and attojoule switching energies (~260aJ/bit for oxide-clad PC cavities and ~80.7aJ/bit for air-clad PC cavities) ideal for photonic computing and transceiver applications. Future designs will seek to further lower the switching energies and improve the switching speed in the bus-coupled structures while still achieving low IL and large ER. Fabricated devices will be doped to experimentally demonstrate the designed attojoule switch performance metrics.

6. ACKNOWLEDGEMENTS

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