

A 0.71-mW Antenna-Coupled On-Off-Key Receiver for Gbps Millimeter-Wave Wireless Communications

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Abstract—This article presents a 39-GHz 800-Mb/s antenna-coupled ON-OFF-key (OOK) receiver with a baseband output capable of driving a $50\text{-}\Omega$ load. The antenna-coupled receiver demonstrates a bit error rate (BER) of 10^{-3} over a range of 18 cm while dissipating only 0.71 mW for a record energy efficiency per distance metric of 0.049 pJ/bit/cm. A wireline version of the receiver achieves a record sensitivity level of -36 dBm without preamplification while dissipating only 1.15 mW, resulting in an energy efficiency of 1.44 pJ/bit at a BER of 10^{-3} . Including 11.5 dB of RF gain prior to the wireline receiver, 800-Mb/s communication is demonstrated at 3.67 m for a BER of 10^{-5} . The low power consumption and long range make this receiver suitable for scaling to hundreds or thousands of elements in massive multi-in-multi-output (MIMO) arrays for next-generation millimeter-wave wireless communications systems.

Index Terms—Antenna arrays, millimeter wave (mmW), multi-in-multi-output (MIMO), nonlinear wireless communications, receivers, rectifier, Schottky diodes, wireless communication systems.

I. INTRODUCTION

OVER the last decade, there has been a flurry of activity in increased deployment of wireless systems in the high microwave and millimeter-wave (mmW) bands, e.g., 802.11ac/aj/ay WiGig and 3GPP NR FR2 [1], [2]. The motivation is clear. Increasing carrier frequencies allows the use of large amounts of available bandwidth, mitigating the spectrum crunch and enabling gigabit-per-second

Manuscript received 18 July 2022; revised 12 October 2022; accepted 22 October 2022. Date of publication 5 December 2022; date of current version 4 April 2023. This work was supported in part by the National Science Foundation Grant ECCS-1731056 and in part by AT&T Labs. (Corresponding author: Jonathan D. Chisum.)

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Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TMTT.2022.3222424>.

Digital Object Identifier 10.1109/TMTT.2022.3222424

(Gbps) data rates for cellular and other wireless devices. However, as carrier frequencies rise, more directive antennas are required and power consumption rises drastically due to reduced passive Q and transistor performance, which is especially concerning for small battery-powered devices such as smartphones. Mobile platforms have predominantly used phased arrays for dynamic link acquisition, which employ anywhere from a few to hundreds of low-gain antennas and mmW front ends. Moreover, these systems typically employ high-resolution quadrature signaling, requiring phase-coherent receivers and multibit (“linear”) analog-to-digital converters (ADCs). Neither comes for free—LO distribution is difficult and power consuming, and ADC power consumption scales exponentially with the number of bits [3]. The power and cost barriers of mmW telecommunications will only worsen as carrier frequencies continue to rise and have prompted considerable industry interest in sustainable wireless systems [4], [5]. Alongside device- and circuit-level improvements, changes to mmW radio architectures and paradigms should also be seriously considered. In particular, we investigate a receiver that is not (super) heterodyne in this work.

One potential approach to reduce power consumption and cost is to reduce signaling complexity, the simplest of which is ON-OFF keying (OOK). OOK waveforms may be demodulated by noncoherent receivers, which are substantially simpler than the predominant quadrature superheterodyne architecture used today. Moreover, single-carrier OOK is robust against nonlinear effects and exhibits a relatively constant envelope, reducing equalization/predistortion complexity and allowing for higher amplifier efficiency. OOK has most recently been of interest for high-data-rate extremely short-range applications such as wireless chip-to-chip interconnects or device-to-device data transfer. Here, we consider the applicability of a noncoherent OOK receiver for room-scale wireless networks. Although OOK exhibits low spectral efficiency, it is of great interest to study the channel efficiency achievable when a high number of antennas are employed, especially when considering hardware impairments that will arise from minimum-cost, minimum-complexity, minimum-power receiver architectures. To date, studies of 1-bit multiantenna networks [see Fig. 1(a)] have exclusively been limited to simulations [6], [7], [8] and

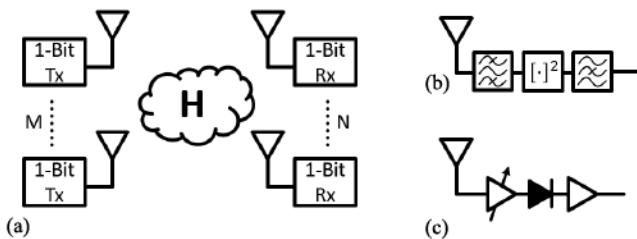


Fig. 1. (a) Envisioned 1-bit architecture with M 1-bit transmitters and N 1-bit receivers separated by a wireless channel H . (b) Minimal complexity antenna-coupled receiver comprising RF matching, a square-law envelope detector to convert amplitude-modulated RF to baseband, and 2nd harmonic filter. (c) Practical RF envelope detector is implemented as a cascade of a (commercial) RF LNA, zero-bias Schottky diode operating in the square-law regime, and a baseband amplifier.

very rarely consider impaired-hardware scenarios. This work investigates and characterizes a simple-as-possible envelope detector for an ultralow-power (mW level) noncoherent mmW receiver, which is suitable for scaled massive multi-in–multi-output (MIMO) testbeds with hundreds of elements in order to study algorithms and performance limits of realistic impaired 1-bit systems.

Noncoherent OOK transceivers typically share very similar architectures. The transmitter comprises an oscillator, either directly at the carrier frequency or a subharmonic thereof (which is then multiplied as needed). The oscillator is modulated at the data rate by a switch or switched amplifier and possibly sent through a power amplifier (PA) before the antenna. The typical receiver, shown in Fig. 1(b), comprises an RF LNA and an envelope detector, which, under low-power conditions, effectively behaves as a square-law device. The envelope detector output is low-pass filtered, and then, the resulting baseband signal is amplified. The amplified signal is then delivered to a comparator or limiting amplifier for interfacing with digital logic circuitry.

Existing Gbps OOK receivers are generally of three varieties. The first is fully integrated active receivers in CMOS or SiGe Bipolar CMOS (BCMOS) that consider RF and baseband amplification, sometimes including limiting amplifiers or comparators at baseband [9], [10]. In [9], they demonstrate an energy efficiency of 2.65 pJ/bit over a 5-cm link, extending to 10 cm for a bit error rate (BER) of 10^{-3} , but the receiver consumes 21 mW. In [10], they demonstrate 0.5 pJ/bit, but this omits the baseband amplifier and has a sensitivity limit of -17 dBm (for short-range communications). Total power consumption, including the output buffer, is 21.5 mW. The second variety is discrete envelope detectors based on, e.g., Schottky diodes [11], [12]. While this class of detector benefits from high intrinsic diode responsivity, they do not fully consider the importance of the baseband circuitry and therefore exhibit low sensitivity. Often, the high power consumption of commercial-off-the-shelf (COTS) baseband amplifiers used in measurement testbeds is neglected, despite the fact they are an essential component of an integrated solution. The third application employing Gbps OOK is optical receivers, which focus on simultaneously achieving multi-Gpbs operation while miti-

gating receiver noise [13]. Generally, these links are wireline with relatively high incident power levels and represent the wideband extreme requiring sophisticated transimpedance amplifiers (TIAs) to buffer and amplify the baseband signal.

The receiver used in this work is a discrete envelope detector combining a very high responsivity zero-bias diode (ZBD) with a low-bias, high input impedance baseband amplifier (BBLNA), designed to simultaneously achieve low baseband noise and support wide bandwidth into a low-impedance load while providing an extremely high sensitivity. The carrier is chosen to be 39 GHz to demonstrate operation in a commercial 5G band. While some of the fully integrated systems (e.g., [9], [10]) demonstrate a very impressive energy per bit, their sensitivity (and therefore range) is limited and their total power consumption (~ 20 mW) is prohibitively high for scaling the receiver to hundreds of cells in a massive MIMO array. The key novelty of this work is a careful rectifier design methodology and application of a low-power baseband LNA (BBLNA) to diode-based noncoherent receivers in order to achieve high-data-rate communications. The design approach culminates in extremely low total power consumption and high sensitivity mmWave receivers with buffered wideband outputs in a compact 2.05-cm² area. Because of the low power consumption and compact form factor, the proposed receiver can be readily scaled to very large massive MIMO arrays. The receivers employ high-quality zero bias diodes, efficient mmW circuit layout (e.g., conjugate-matched antennas to omit lossy matching networks prior to the diode) combined with a system-level optimization, which yields the optimal RF gain to achieve a balance of data rate, range, and low total power consumption. A wireline version of the receiver exhibits a record sensitivity of -36 dBm (BER of 10^{-3}) for a non-preamplified receiver and an energy efficiency of 1.44 pJ/bit. An antenna-coupled receiver dissipating only 0.71 mW demonstrates communication over a range of 18 cm (BER of 10^{-3}) for a record energy efficiency per distance [9], [14] of 0.049 pJ/bit/cm.

Section II details the receiver design method beginning with a theoretical efficiency analysis and describes the design of three prototypes: 1) a standalone detector for rectifier evaluation [Fig. 6(a)]; 2) a wireline receiver with integrated BBLNA [Fig. 6(c)]; and 3) an antenna-coupled receiver with integrated BBLNA [Fig. 6(e)]. Section IV describes the wireline and over-the-air (OTA) measurement results of each detector.

II. RECEIVER DESIGN

In this section, we first consider a minimum-complexity wireless OOK receiver comprising an antenna and an envelope detector (approximate square-law detector), as shown in Fig. 1(b). Later, the performance with an RF LNA will be considered as in Fig. 1(c). The core detector uses a W-band zero-bias Schottky diode from Virginia Diodes Inc. (VDI) though any general nonlinear element [15], [16], [17] may be used as well. Even though the receiver operates in the *Ka*-band, the VDI W-band GaAs ZBD is used for its commercial availability, low cost, low noise, high cutoff frequency, simple flip-chip integration, and high rectification efficiency at mmW

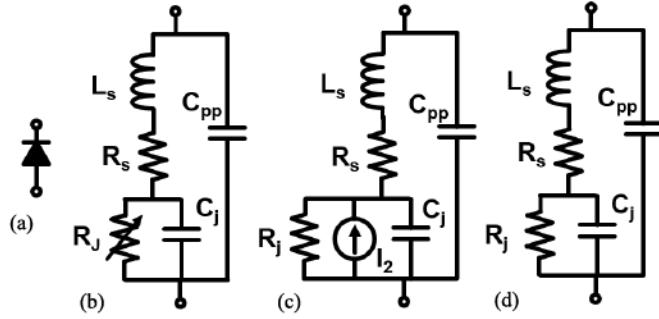


Fig. 2. (a) and (b) Diode is represented as an intrinsic nonlinear resistance embedded in a linear network. C_j is assumed linear. (c) Second-order Taylor representation is used to approximate the nonlinear response, and the linear portion is given by R_j . (d) Linearized representation is used for impedance matching purposes.

TABLE I
DIODE MODEL ASSUMED FOR DESIGN [18]

R_j	C_j	C_{pp}	R_s	L_s
$935\ \Omega$	$10\ fF$	$16\ fF$	$6.5\ \Omega$	$50\ pH$

frequencies for a passive device. The lumped-element model (Fig. 2) and parameters (Table I) assumed for the design process are taken from [18]. The nonlinearity of the junction capacitance C_j is assumed to be negligible and will not be considered here [19], [20].

The most important function of the receiver is to convert a mmWave signal at 39 GHz to baseband as efficiently as possible and to maintain this efficiency over a wide 1-GHz bandwidth into a low-impedance baseband load (e.g., $50\ \Omega$). In the following, we derive the total conversion efficiency of the receiver in terms of component efficiencies and point out key design implications along the way. Then, we discuss the high-level design requirements to support a 1-GHz baseband signal into a low-impedance load.

A. RF Efficiency

Rectification efficiency of square-law detectors is of particular interest in RF/THz detection and energy harvesting [20], [21], [22]. Although detection and harvesting differ from envelope detection in their video bandwidths, noise treatment, and baseband power transfer characteristics, this article largely follows the approach used for energy harvesters in [20] for enumerating the RF-to-baseband efficiency terms:

$$\eta_{\text{tot}} = \eta_m \eta_p \eta_0 \eta_r. \quad (1)$$

As shown in Fig. 3, η_m represents the loss from the RF input to the diode terminated by the rejection network. η_p represents the loss due to diode parasitics. η_0 represents the RF-to-dc conversion of the intrinsic nonlinear element. η_r represents the loss in the finite- Q rejection network and is a new term added by the authors to account for losses due to the finite- Q transmission lines, which become more significant at higher frequencies (as in this work). Both η_0 and η_p are device-level metrics, whereas η_m and η_r address both the chosen device and the circuit topology. The bandwidth and noise behavior of the system at baseband are more complicated and

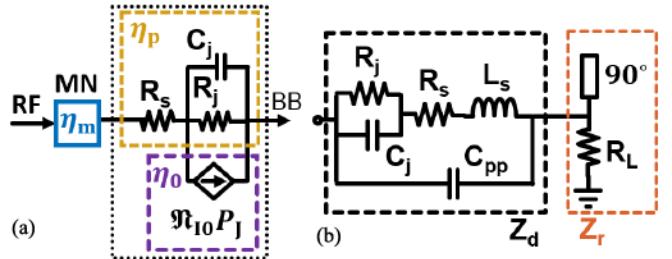


Fig. 3. (a) Efficiency model of a receiver including match efficiency η_m , parasitic efficiency η_p , and intrinsic efficiency η_0 . (b) η_r is a result of the interplay between the diode model Z_d and the load impedance of the rejection network Z_r .

treated differently for wideband detectors. This is the subject of our previous work [23], in which we analyze the effect of nonlinear mixing between signal and noise and derive the optimal RF gain level to maintain the maximum SNR while expending a minimum of dc power.

η_m is defined as the proportion of available power at the antenna (P_{in}) that is delivered to the detector (P_{dr}), which is the combination of the rejection network and diode. Assuming no reflection, η_m for a one-stage (L-section) matching network is given by [24]

$$\eta_m = \frac{P_{\text{dr}}}{P_{\text{in}}} \approx \frac{1}{1 + Q/Q_c} \quad (2)$$

where Q is the required matching network quality factor (or the maximum Q of the trajectory taken across the Smith chart for matching). When matching to a complex load Z_L from a real-valued source impedance R_{src} , if Z_L lies within either the $G = 1/R_{\text{src}}$ or $R = R_{\text{src}}$ circles, $Q > Q_L$; otherwise $Q = Q_L$. Z_L refers here to the driving point impedance of the rejection network and diode [shown in Fig. 3(b)]. Q_c is the unloaded quality factor of the matching components. For transmission line matching networks, Q_c is addressed by ensuring that the metallization thickness is on the order of several skin depths. If the mismatch is considered, then (2) becomes

$$\eta_m = \frac{1 - |\Gamma|^2}{1 + Q/Q_c} \quad (3)$$

where Γ is the reflection coefficient between the RF source and the driving point impedance of the matching network.

Loss due to the rejection network, characterized by η_r , depends on whether a shunt or series topology is employed (Fig. 4). Although both were fabricated, the series topology has a couple of key benefits and is the only one measured in this work. As will be discussed later, minimizing the baseband shunt capacitance C_{Tot} is critical for achieving high data rates. C_{Tot} comprises both capacitance due to the detector circuit (C_p) and the BBLNA (C_A). It is important to consider the relative magnitude of C_p for the series and shunt topologies, assuming that C_A is fixed and C_A does not dominate C_{Tot} .

In the shunt case, a blocking capacitor C_B is required to prevent the baseband signal from propagating toward the antenna and dissipating in R_{src} . The shunt topology also requires two quarter-wave sections (contributing shunt capacitance C_R). The first quarter-wave stub shorts out the baseband amplifier (Z_A) at f_0 , and the second ensures that the diode itself is

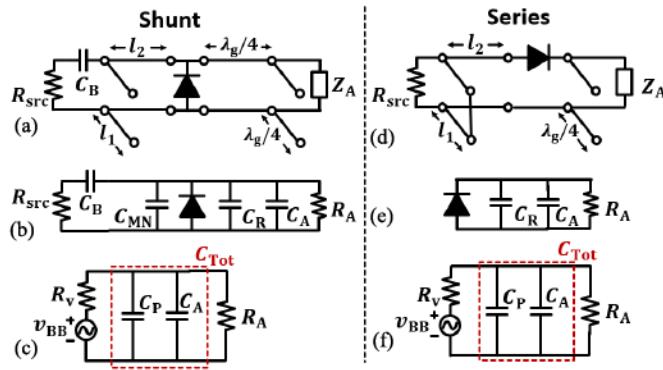


Fig. 4. Two topologies for single-diode detectors, assuming shunt stubs. Z_A is assumed to be well-modeled by an RC circuit. (a)–(c) Shunt diode requires an open-circuit matching stub and blocking capacitor C_B to keep the dc shorting out. (d)–(f) Series topology is more compact as the rejection stub is half the length, and no C_B is required. Instead, the shunt matching stub is terminated in a short. C_R (similarly, C_P) is reduced compared to the shunt topology.

not shorted out. Moreover, the matching network contributes a capacitance C_{MN} to C_p .

Conversely, the series detector does not require C_B . Instead, the matching network employs a shorted stub to connect the diode to ground at baseband. As a result, neither C_{MN} nor C_B contributes to C_p . In addition, the series detector has a more compact layout because the rejection network requires only a single quarter-wave section located at the diode terminal on the baseband side (not displaced by a quarter-wave line as in the shunt configuration). This is because shorting out Z_A does not short out the diode in the series topology. This halves the length of line in the rejection network and therefore approximately halves C_R . In general, C_{MN} , C_B , and C_R are the principal components of C_p . Therefore, the series topology can reduce C_p by about a factor of 4 relative to the shunt topology

$$C_p \approx \begin{cases} C_B + C_{MN} + C_R + C_j + C_{pp}, & \text{shunt topology} \\ C_R + C_j + C_{pp}, & \text{series topology.} \end{cases} \quad (4)$$

An auxiliary benefit of the series detector is that it is more conveniently integrated with the slot dipole antennas used in this work, which has R_{src} of 0Ω at dc. We will assume a series rectifier for the remainder of this work.

With a series topology selected, it is now possible to calculate η_r . η_r is the ratio of the power delivered to the diode (P_{diode}) to the power available from the matching network (P_{dr}). Some of the available RF power will not make it into the diode impedance (Z_d), but will instead be delivered to the rejection network/baseband load with driving point impedance Z_r . Therefore,

$$\begin{aligned} \eta_r &= \frac{P_{diode}}{P_{dr}} \\ &= \frac{\text{Re}\{Z_d\}}{\text{Re}\{Z_r\} + \text{Re}\{Z_d\}} \\ &= \frac{R_d}{R_d + R_r} \end{aligned} \quad (5)$$

where R_d and R_r are the real parts of the diode and rejection network/baseband load impedances, respectively, at f_0

(39 GHz in this work). Note that R_d is not the linearized junction resistance R_j [see Fig. 2(c) and (d)] and is highly dependent on the reactive parasitics. Both η_m and η_r are maximized in a series topology by using high Q_c passives and selecting a diode with low parasitics.

η_p is defined as the proportion of P_{diode} that is delivered to the intrinsic diode junction ($P_{junction}$) and is given (approximately) as [20]

$$\begin{aligned} \eta_p &= \frac{P_{junction}}{P_{diode}} \\ &= \frac{1}{1 + (\omega C_j)^2 R_s R_j}. \end{aligned} \quad (6)$$

For the diode and frequency considered here, this approximation is correct to within half a percent [see Fig. 5(a)]. It generally predicts slightly too high an efficiency but only diverges significantly from the rigorous expression when $R_s \sim R_j$ (in this work, $R_j \sim 1 \text{ k}\Omega$, much greater than $R_s \sim 10 \Omega$). The lumped-element model of Table I predicts a parasitic efficiency of 0.92 (or -0.36 dB). Assuming a constant C_j and fixed f_0 , the parasitic efficiency is typically improved by lowering R_j (forward biasing the diode). Our high η_p is due to using a W-band diode despite operating at 39 GHz.

The intrinsic diode conversion efficiency η_0 is the ratio of baseband power P_{BB} to RF power, which is incident upon the internal junction of the diode ($P_{junction} = \eta_m \eta_r \eta_p P_{RF}$). For a low-power excitation, η_0 may be approximated iteratively by Volterra operators through the nonlinear current method [25], which is often truncated to the second-order term(s) only. Considering the intrinsic nonlinear junction of Fig. 2(b) and assuming sufficiently low RF input power

$$I(V) \approx I(V_{dc}) + i'(v)v + \frac{1}{2}i''(v)v^2 \quad (7)$$

where $i'(v)$ and $i''(v)$ denote the first and second derivatives of $I(V)$ about the bias point, respectively. The intrinsic diode is assumed to follow the Shockley equation:

$$\begin{aligned} I(V) &= I_s \left(e^{\frac{qV}{nV_T}} - 1 \right) \\ &= I_s \left(e^{\frac{V}{nV_T}} - 1 \right). \end{aligned} \quad (8)$$

The ac derivatives are given by

$$\begin{aligned} i'(v) &= \frac{dI}{dV} \Big|_{V=V_{dc}} \\ &= \frac{I_s}{nV_T} e^{\frac{V_{dc}}{nV_T}} \\ i''(v) &= \frac{d^2I}{dV^2} \Big|_{V=V_{dc}} \\ &= \frac{I_s}{n^2 V_T^2} e^{\frac{V_{dc}}{nV_T}}. \end{aligned} \quad (9)$$

The small-signal change in current due to a change in junction voltage is the linear junction conductance, the reciprocal of which is the linearized junction resistance R_j [see Fig. 2(c) and (d)]. Using the trigonometric identity

$$A(t) \cos^2(\omega t + \phi(t)) = \frac{A(t)}{2} + \frac{A(t)}{2} \cos(2\omega t + 2\phi(t))$$

the quadratic term in (9) produces currents at both baseband and $2f_0$ in response to a narrowband excitation. The phase information is destroyed at baseband, and thus, only the envelope is retained. The intrinsic current responsivity, \mathfrak{R}_{10} , is defined here as the ratio of the short-circuit dc output current to RF power delivered to the diode junction. This quantity (as opposed to the open-circuit voltage responsivity \mathfrak{R}_{V0}) is especially convenient to describe Schottky diodes, for which it is ideally invariant with bias.¹ Given an input signal $A\cos(\omega t)$, where A is a constant, the power is given by $P_{\text{RF}} = A^2/2R_j = i'(v)A^2/2$ and the (dc) output current is given by $i_{\text{dc}} = i''(v)/2 * A^2/2 = i''(v)A^2/4$. This leads to

$$\begin{aligned}\mathfrak{R}_{10} &:= \frac{i_{\text{dc}}}{P_{\text{RF}}} \\ &= \frac{i''(v)A^2}{4} \cdot \frac{2}{A^2i'(v)} \\ &= \frac{i''(v)}{2i'(v)} \\ &= \frac{1}{2nV_T}.\end{aligned}\quad (10)$$

For an ideal Schottky diode ($n = 1$) at room temperature, this quantity is equal to 19.35 A/W. This is a fundamental limit of any diode obeying the Shockley equation.² The baseband amplitude is proportional to the square of the carrier's amplitude. Having discussed the mechanism of rectification, we now consider the power efficiency of the rectification process.

Modeling the diode at baseband as a Norton equivalent circuit [Fig. 2(c)], the intrinsic nonlinear efficiency is the ratio of the baseband power available from the diode to the RF power delivered to the intrinsic diode junction

$$\begin{aligned}\eta_0 &= \frac{P_{\text{BB}}}{P_{\text{junction}}} \\ &= \frac{\mathfrak{R}_{10}^2 P_{\text{junction}} R_j}{4} \\ &= \frac{\mathfrak{R}_{10}^2 \eta_m \eta_r \eta_p P_{\text{in}} R_j}{4}.\end{aligned}\quad (11)$$

Combining (1), (3), (5), (6), and (11)

$$\eta_{\text{tot}} = \left[\frac{(1 - |\Gamma|^2)}{1 + Q/Q_c} \frac{R_d}{R_r + R_d} \frac{1}{1 + (\omega C_j)^2 R_s R_j} \right]^2 \cdot \frac{\mathfrak{R}_{10}^2 P_{\text{in}} R_j}{4}. \quad (12)$$

Likewise, the open-circuit voltage expected for a given input power is

$$\mathfrak{R}_V = \frac{(1 - |\Gamma|^2)}{1 + Q/Q_c} \frac{R_d}{R_r + R_d} \frac{\mathfrak{R}_{10} R_j}{1 + (\omega C_j)^2 R_s R_j}. \quad (13)$$

¹This is notably not the case for tunnel diodes.

²Or rather, any diode whose operation is solely governed by thermionic emission.

B. Receiver Design Guidelines

From the preceding analysis, an efficient receiver circuit should consider the following points.

- 1) Proper selection of a low-parasitic diode, appropriate to the band of interest (package and integration parasitics must be included in the analysis).
- 2) Thick metal must be used to increase Q_c of the transmission lines used in matching networks and filters.
- 3) Matching network and rejection filter size should be minimized to reduce a loss (e.g., here, we recommend a series topology because it allowed the rejection stub to be placed right at the diode terminals).
- 4) As will be discussed shortly, the total capacitance in the baseband interface should be minimized.

For the diode described in Fig. 2 and Table I, an operating frequency of 39 GHz, a series topology, and neglecting nonlinear capacitance, the only tunable parameters controlling η_{tot} are R_j and Q_c . Higher Q_c is always preferable. Fig. 5(b) shows η_{tot} as a function of R_j (or video resistance, since $R_v = R_j + R_s \approx R_j$), assuming Q_c of 50, which corresponds to the coplanar waveguide (CPW) used in this work. The peak value of η_{tot} for this diode occurs around $R_j = 5.5$ k Ω (a very weak reverse bias). As will be shown, this resistance is not suitable for the desired baseband bandwidth with the baseband amplifier architecture selected, but this efficiency result demonstrates that forward biasing the diode to improve η_p and η_m is not necessarily the optimal approach. This is in contrast to the literature on energy harvesting, where lower junction resistance is often desirable to improve dc power transfer to a (typically relatively low impedance) load [26].

In addition to conversion efficiency, the receiver must also support a baseband output sufficient for the intended data rate. For the detectors used, $R_v \sim 2$ k Ω and $C_p \sim 200$ fF; thus, assuming a single-pole response and infinite BBLNA input impedance, the minimum cutoff frequency (assuming $C_A = 0$) is only 400 MHz (0.4 f_{sym}), where f_{sym} is the symbol rate. Optical receivers, which often use photodiodes with similar impedances to Schottky ZBDs, generally require that their TIAs have a bandwidth of $0.6f_{\text{sym}} < f_c < f_{\text{sym}}$ [13]. The TIA bandwidth is a compromise between limiting the noise bandwidth and being able to support fast data transitions, where f_c includes the effects of both the input pole and gain roll-off of the amplifier itself.

TIAs in optical receivers very often rely on low-input-impedance input stages (common-gate or shunt-feedback topologies) to improve operating bandwidth at the expense of gain. In this case, however, the operating bandwidth is much lower than in an optical system, and thus, the stringent tradeoff between gain and bandwidth can be navigated using a high-impedance amplifier topology. This enables a simpler architecture and biasing scheme while taking advantage of a more aggressive impedance transformation from generator to amplifier load. However, it is critical that the parasitic baseband capacitance C_{Tot} is as low as possible. Although the bandwidth may also be obtained by lowering R_v (through R_j), the RF performance degrades as R_j decreases (Fig. 5), and thus, reducing both C_p and C_A is the first priority. The high input

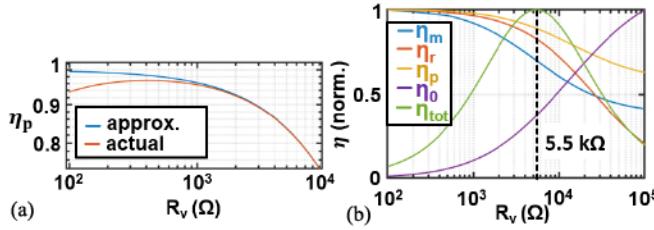


Fig. 5. (a) Approximate value of η_p is given by (6), which is accurate as long as $R_j \gg R_s$. R_s of 6.5Ω is assumed. (b) Parametric analysis of this model using simple approximations for efficiency as a function of R_j indicates an optimal R_j of $5.5 \text{ k}\Omega$.

impedance amplifier can compensate for the low-frequency pole in the input network, as discussed in Section III-C.

III. RECEIVER PROTOTYPES

Three detectors were designed and optimized in Ansys HFSS (see Fig. 6): a detector with two GSG probe pads for probe-station characterization (referred to as the standalone detector), a detector with one GSG probe interface at RF, a wirebond pad for BBLNA integration (referred to as the wireline receiver), and an antenna-coupled detector also for BBLNA integration (referred to as the antenna-coupled receiver).

A. Detector

Following the design guidelines from Section II-B, a series topology was chosen to reduce C_p . The detectors were designed on $500\text{-}\mu\text{m}$ quartz ($\epsilon_r = 3.9$) with a nominal $3.8 \mu\text{m}$ TiW-Au metallization for low loss ($Q_c \approx 50$) and easy wirebonding. The rejection stubs have a high Z_0 of almost 130Ω to reduce C_R and are terminated in a lumped capacitance to reduce the stub length. Symmetrical stubs are used in the probed detectors to suppress the CPW odd mode at the cost of larger C_R . Impedance matching to 50Ω was implemented using single symmetrical stubs for the probed detectors and direct antenna conjugate matching for the antenna-coupled receiver.

B. Antenna and Matching Network

In order to improve η_m and form factor, the antenna was designed to be directly conjugate matched to the rectifier circuit. Fig. 7(a) shows the impedance looking into the diode and rejection stub for the antenna-coupled receiver of Fig. 6(e) (pink dot). The conjugate impedance (black star) can be modeled as a resistor-inductor pair at the center frequency. Considering the following identity for complementary antennas [27]:

$$\begin{aligned} Z_{\text{comp}2} &= \frac{Z_{\text{FS}}^2}{4Z_{\text{comp}1}} \\ &= 38 - j230 \Omega \end{aligned}$$

where Z_{FS} is the impedance of free space, and the desired antenna may be designed as a wire antenna and then converted back into a slot design. The desired complementary impedance

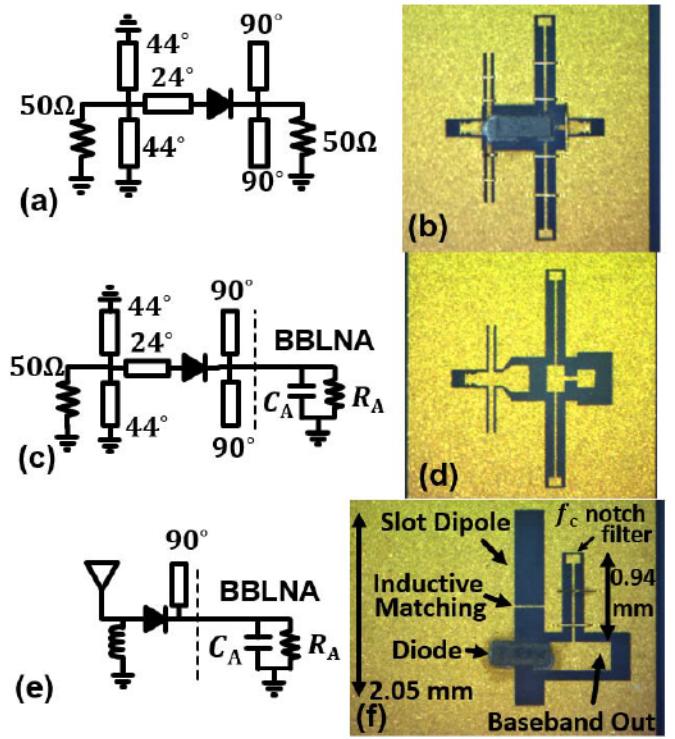


Fig. 6. Three detectors measured in this work (BBLNAs not shown). (a) and (b) Standalone detector, primarily used to measure impedance characteristics. (c) and (d) Wireline receiver, used for both wireline and OTA BER measurements with variable Ka -band RF LNA (shown before diode soldering and wirebonding). (e) and (f) Antenna-coupled receiver, used for passive front-end BER measurements.

(green square) is capacitive and may be achieved using a series or parallel RC . The series representation has a more achievable R_{rad} , and thus, a gap-coupled dipole was chosen as a possible implementation [Fig. 7(b), top]. It was confirmed that a practical (fabricable) version of this antenna could reach the desired complementary impedance. The complement of the dipole structure is the desired antenna, which is a shunt-inductor-loaded slot dipole [Fig. 7(b), bottom, and (c)]. Optimization of dipole asymmetry, dipole length, dipole width, and inductor location was employed to ensure good matching to the diode. The simulated 3-dB bandwidth is 3 GHz and the baseband-referred 3-dB bandwidth (including the quadratic effect of rectification) is 2 GHz, which is deemed sufficient bandwidth to mitigate intersymbol interference (ISI) [28].

The simulated radiation pattern of the slot dipole is shown in Fig. 7(d). The electric field is polarized in x [see Fig. 7(c)], across the short dimension of the dipole. The antenna as designed preferentially radiates through the substrate with a front-to-back ratio of 5 dB and a directivity of 5 dB. For this reason, OTA measurements were conducted with the antenna-coupled receiver “facing away” from the transmitter, as shown in Fig. 22(a).

C. BBLNA

Due to the high video resistance R_v of the passive diode detector, driving a $50\text{-}\Omega$ load directly would result in an excessively poor mismatch at baseband. As such, a BBLNA is

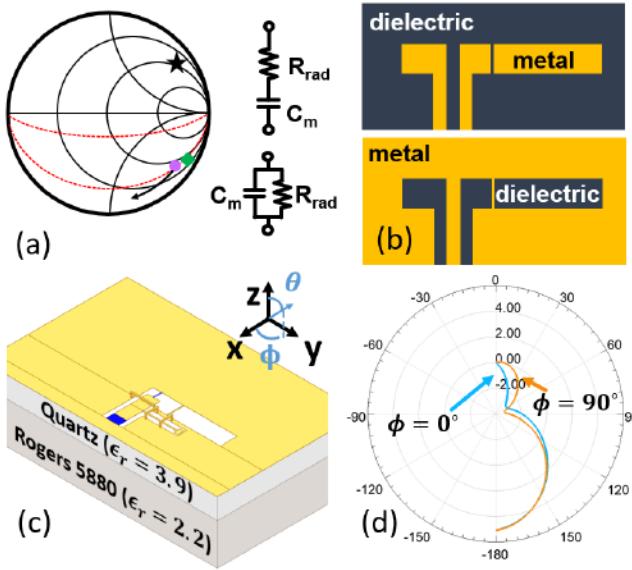


Fig. 7. (a) We wish to conjugate match to the diode (purple dot, conjugate is black star). The complementary antenna must therefore have the impedance given by the green dot. (b) Capacitively coupled dipole (top) and its complement, the inductive slot dipole used in this work (bottom). (c) Antenna is seated not only on the chip substrate but also on the carrier printed circuit board (PCB) for the BBLNA. (d) Antenna preferentially radiates in the $-z$ -direction due to the high permittivity of the quartz substrate and PCB.

necessary to provide voltage gain and to buffer the diode from a low-impedance load as well as from the significant capacitance that may be present on a PCB trace or downstream circuit. While low-impedance TIAs are necessary for extremely wideband optical communication systems, a high input-impedance topology is used in this work. The BBLNA, shown in Fig. 8(b), is a three-stage common-source amplifier employing shunt peaking [29] to counteract the input stage pole at

$$f_{3\text{ dB, input}} = \frac{1}{2\pi R_v C_{\text{Tot}}} = \frac{1}{2\pi R_v (C_p + C_A)}. \quad (14)$$

At the interface between the mmWave detector chip and the BBLNA, care is taken in design and layout to reduce C_A and maintain bandwidth. Specifically, the layout [Fig. 8(c)] employs thin traces, a thick low- ϵ_r substrate (60-mil Rogers 5880, $\epsilon_r = 2.2$), and the ground plane is removed from underneath the first stage [see red dashed line, Fig. 8(c)]. Biasing consists of an inductive RF choke at each stage (to reduce power consumption compared to resistive biasing often employed in RFICs), ac coupling between stages, and pull-down bias resistors at the transistor gates. All three transistors are nominally connected to the same V_{DD} but in fabrication were broken out to individual drain bias voltages for stability.

The same transistor is used for T1, T2, and T3, the Diramics pH-100 2f25 2-channel InP pHEMT, and was selected for its extremely low total gate capacitance (for a discrete device) of $C_g = 50 \text{ fF}$, which supports the wide bandwidths necessary for Gbps communications. In addition, it provides a relatively

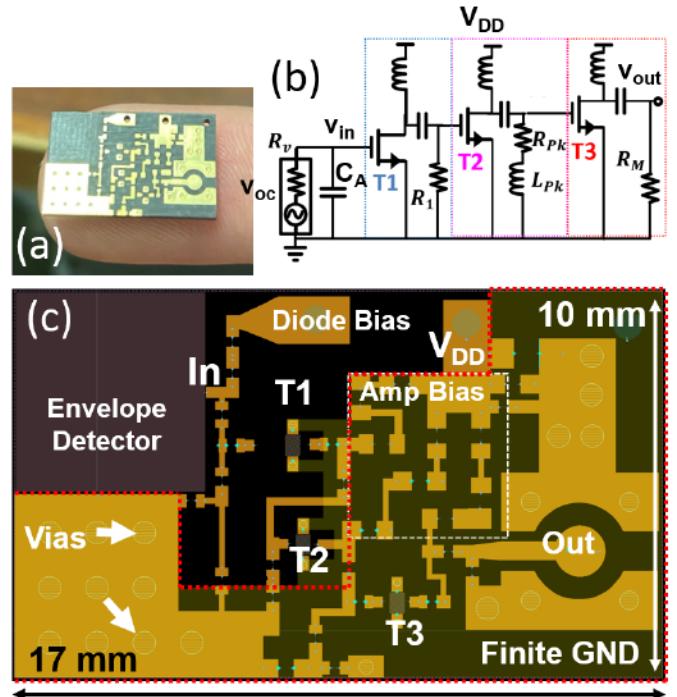


Fig. 8. (a) PCB (unpopulated) of the high-impedance BBLNA used in this work. (b) Three-stage cascaded common-source architecture. (c) PCB layout with an overall size of $17 \times 10 \text{ mm}$ showing the milled pocket for the "Envelope Detector," a reduced-size ground plane (outlined in red dashed line), dense routing, and compact discrete elements (many 0201 packages).

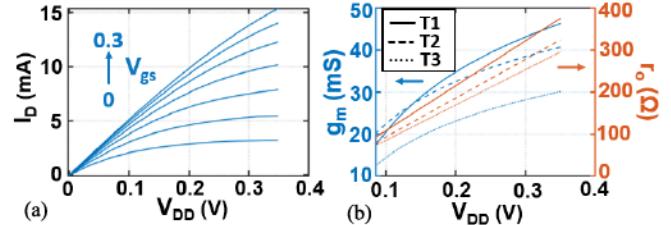


Fig. 9. (a) DC I - V 's measured for transistor T1 used in the wireline receiver. (b) Transistors used exhibit a high g_m and very low r_o .

high transconductance g_m (and hence power gain) at a low bias power, which is critical to the BBLNA design since the BBLNA represents the entirety of the power consumption of this non-preamplified receiver. As can be seen from Fig. 9(b), the transistors exhibit g_m of between 10 and 45 mS and r_o of between 80 and 400 Ω , for $V_{DD} < 0.35 \text{ V}$ and $I_{ds} < 15 \text{ mA}$. The high g_m makes them especially suitable for driving the 50- Ω line output. Stage T1 provides a low- C_p input stage to reduce the roll-off of the input pole as much as possible, T2 boosts the gain at high frequency using shunt peaking to counteract the remaining roll-off, and T3 is a buffer stage providing a match to an external 50- Ω line. The cascade provides a high input impedance, a large impedance transformation ration (40:1), and flat voltage gain across the band.

Because the InP transistors exhibit an extremely high f_t/f_{max} of 220 GHz/500 GHz, well beyond the valid frequency range of the lumped models used for design, instability was

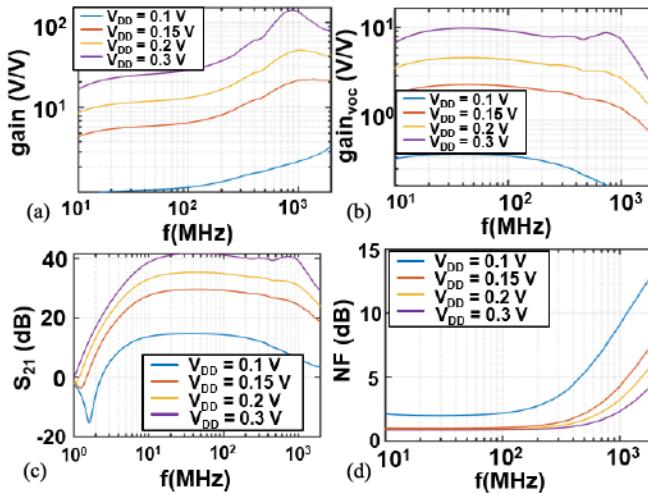


Fig. 10. (a) Amplifier gain peaks across the band by a factor of 4. (b) Significant gain flattening is observed when the input RF pole is considered. (c) Even for low-voltage gains, power gain is high due to the impedance transformation. (d) Low noise (NF < 5 dB) performance is observed for $V_{DD} \geq 0.15$ V.

a significant concern. Therefore, simulations across multiple bias values are shown in Fig. 10, assuming an R_b of 2 k Ω . For the lowest bias level ($V_{DD} = 0.1$ V), the amplifier has voltage gain below unity [see Fig. 10(b)], but, due to the large impedance transformation ratio of 40, the power gain for all biases is greater than 10 dB, as shown in Fig. 10(c). The simulated noise performance is also very good, with noise figure (NF) < 5 dB across the band for $V_{DD} \geq 0.15$ V. In order to stabilize the amplifiers, bias voltages anywhere from $V_{DD} = 0.1$ to 0.3 V were predicted.

RF chokes are used to minimize power dissipation in the bias network. Due to size constraints and parasitics, the chokes have a limited inductance of 2.7 μ H, substantially reducing low-frequency gain. As a result, the amplifier has a bandpass response with a low-frequency cutoff around 10 MHz. This cutoff is 1% of the desired data rate of 1 Gb/s, which results in dc wander [13]. The 8b/10b encoding is here used to increase the number of bit flips and suppress dc wander at a 4/5 code rate, which makes the effective data rate 800 Mb/s at f_{sym} of 1 Gs/s.

IV. RESULTS

A. Standalone Detector

The fabricated standalone detector comprises a detector with no BBLNA and is used for characterization [Fig. 11(a)]. Its diode's I - V characteristics are shown in Fig. 12(a)–(c). The diode shows a high \Re_{10} (very near the theoretical limit) of 16.2 A/W and a notably high R_j of 6.8 k Ω , which would be likely to cause bandwidth problems if used for data detection, as the BBLNA was designed assuming $R_j = 2000$ k Ω . The S -parameters of the probed detector show a maximum zero-bias return loss of 16 dB at 38.7 GHz, slightly shifted from the design frequency of 39 GHz. Applying a forward bias of 30 mV improves the return loss to better than 40 dB, due to a reduction in R_j to 2 k Ω . Suppression of the fundamental frequency at the output is measured as S_{21} in Fig. 12(d), which

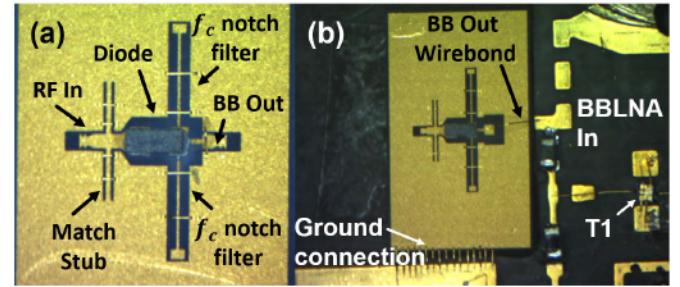


Fig. 11. Fabricated probed detectors. (a) Standalone detector, used for evaluation of matching and rejection. (b) Wireline receiver, designed for integration into the fabricated BBLNA. It is connected electrically to the BBLNA with wirebonds and held in a milled pocket with double-sided tape.

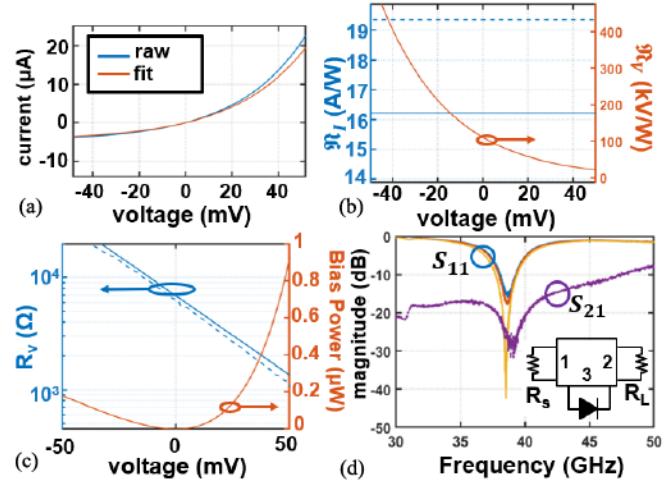


Fig. 12. (a) Measured I - V characteristics for standalone detector [Fig. 11(a)] show good agreement with an ideal diode model for forward bias and weak reverse bias. (b) \Re_{10} of 16.2 is greater than that of the model in [18], indicating n of 1.2. \Re_{10} is extremely sensitive to R_j , whereas \Re_{10} is constant. (c) Measured zero bias R_j is 6.8 k Ω , on the high end predicted by the VDI datasheet. (d) Measured series probed detector shows good isolation between RF and baseband at 39 GHz. The input match is strongly dependent on bias through R_j and exhibits better than 40-dB return loss for a 30-mV forward bias.

is below -25 dB across the RF band, and \Re_V is 24 kV/W at 39 GHz, with 21 kV/W predicted by (13).

B. Wireline Receiver

The wireline receiver shown in Fig. 11(b) is used for end-to-end model verification, as well as both wireline and preamplified OTA BER measurements. Its matching network is designed for an input impedance of 50 Ω . I - V s taken of the diode (\Re_{10} , R_j) and one-port detector S -parameters are shown in Fig. 13(a)–(d). R_b is approximately 3100 Ω and the measured \Re_V is 22 kV/W, with 21 kV/W predicted by (13).

The BBLNA PCB (see Fig. 14) was fabricated by Cirexx International, Inc., with an ENEPIG finish for wirebonding. With the exception of the bias inductors and bypass capacitors, the surface-mount devices (SMDs) have 0201 packages. The chokes were each implemented using three Coilcraft 0402DF-901XJR 900-nH ferrite inductors in series. SMDs were hand-soldered using Sn–Pb solder paste. The transistors

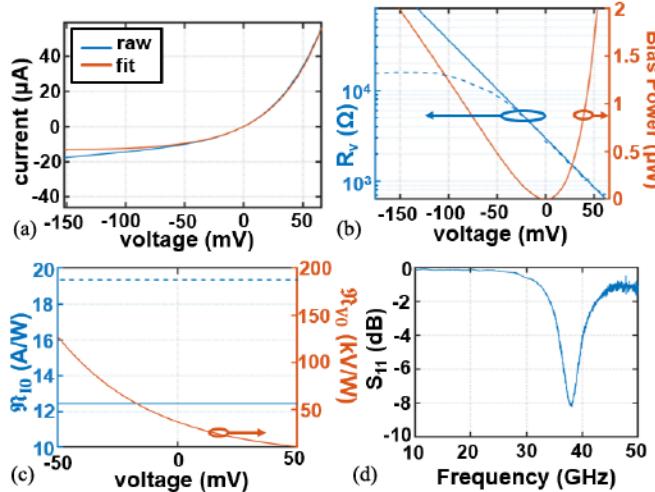


Fig. 13. I - V data and S -parameters for the wireline receiver [see Fig. 11(b)]. (a) Good agreement with Shockley model for forward bias and low reverse bias. (b) R_{i0} of 12.4 corresponds to n of 1.55. (c) Zero bias R_j is around 3100 Ω and saturates to about 16 k Ω as reverse bias increases. (d) Match performance is degraded relative to the standalone detector.

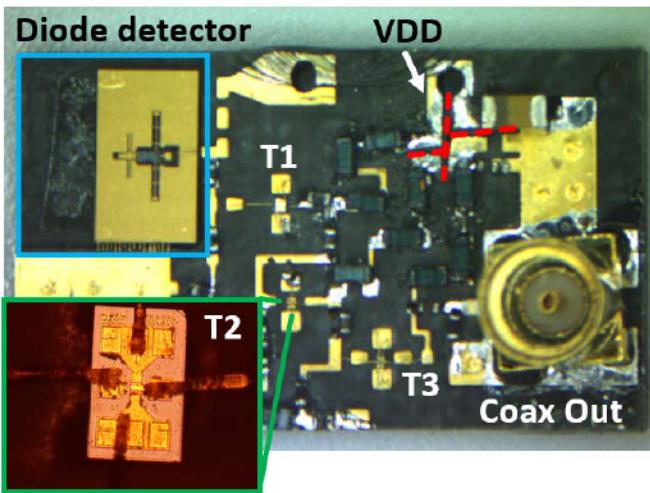


Fig. 14. Wireline receiver (top left, blue rectangle) is mounted in the milled pocket on the BBLNA. The V_{DD} node has been sliced in three to allow different drain bias voltages. The bottom-left inset shows a wirebonded Diramics transistor.

were mounted using glue and micrometer-controlled tweezers, with electrical connection achieved by wedge bonding.

The amplifier initially oscillated, so drain bias voltages were reduced for stable operation—the bias used is summarized in Table II. The low current draws of T1 and T2 indicate single-channel operation (as opposed to two channels under normal operation), which is likely due to damage incurred during oscillation. This bias, along with the transistor damage, lowers g_m and gain, but the corresponding total power consumption is an ultralow 1.15 mW. The performance of this amplifier is shown in Fig. 15 and is compared with a simulation considering the stable transistor bias points of Table II. It exhibits a low saturated output power of $P_{sat} = -16$ dBm (sufficient for the anticipated low receiver

TABLE II
BIAS DETAILS FOR BBLNA OF FIG. 15

Transistor	V_{ds} (V)	I_{ds} (mA)	Power (μ W)
T1	0.3	1.29	387
T2	0.2	1.2	240
T3	0.2	2.6	520

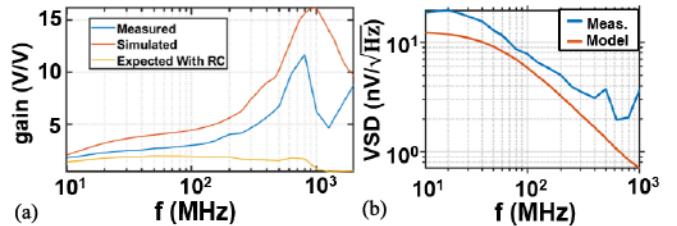


Fig. 15. (a) Gain relative to the amplifier input peaks by a factor of approximately 4 across the operating bandwidth and agrees well with a simulation set at a stable bias. Low-voltage gain is compensated by the large impedance transformation. (b) Input-referred amplifier noise follows the model well, which assumes a noiseless amplifier.

powers in wireless communication links) and a noise voltage spectral density (VSD) within a factor of 2 of that predicted through simulation.

Since the integrated detector mounted to the heterogeneous microwave integrated circuit (HMIC) BBLNA does not provide standard RF probe ports on both sides, a nonstandard two-tone approach, shown in Fig. 16(a) and (b), is used to measure the frequency response of the end-to-end system at both the RF band and across the baseband frequencies. The measurement consists of a two-step process in which two tones centered at f_0 with a frequency separation of Δ , each nominally -40 dBm, are fed into the detector-BBLNA system and the resulting baseband tone at Δ is measured. In a first sweep, Δ is held constant at 10 MHz, and f_0 is swept from 38.5 to 39.5 GHz. Since Δ is constant, the frequency at baseband is held constant, and thus, the gain at baseband is constant. Thus, any marginal variation in the output tone at Δ is due to variation in the RF-and-rectification loss. A second sweep holds f_0 constant at 39 GHz, while Δ is swept from 10 MHz to 1 GHz. Since the RF frequency is held constant, any measured frequency variation can be attributed to the baseband response. Results indicate very good agreement between the model predictions and measurement [Fig. 16(c)]. Moreover, the response versus f_0 is demonstrated to be quite flat [Fig. 16(d)], varying by less than ± 1 dB across the band, whereas the end-to-end efficiency decreases significantly as Δ increases—this nonflat response is attributed to the higher than expected R_v of the diode in use. This results in a more pronounced RC roll-off than expected, and therefore, the BBLNA gain peaking is insufficient to maintain a flat response across the band. This could be addressed in a future design with a different BBLNA design or could possibly be mitigated by forward biasing the diode to reduce R_v .

Probe-station-based BER measurements were conducted as per the block diagram in Fig. 17(a). An 8b-/10b-encoded PRBS sequence is generated with a 12-GSa/s Keysight M8190 AWG and upconverted to 39 GHz using wideband

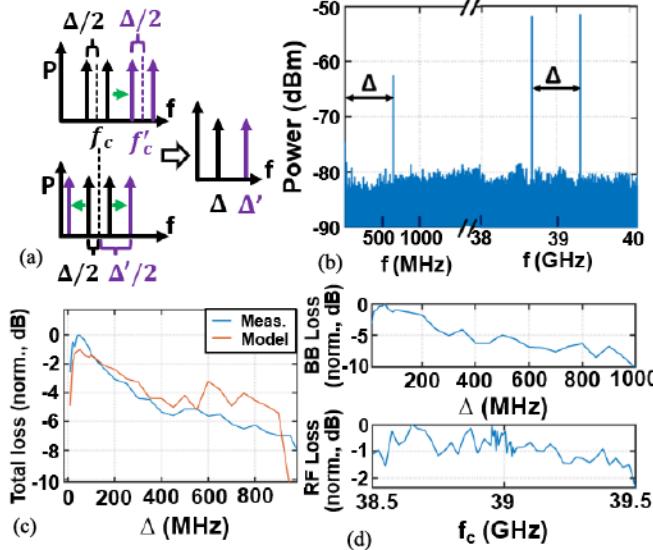


Fig. 16. (a) Two-tone approach for separating the frequency dependence in RF detector and baseband amp. A fixed f_0 gives an aggregate RF-BB response, whereas a fixed Δ essentially gives just the BB response to within a multiplicative constant. (b) Example baseband and RF spectra showing Δ of 650 MHz, f_c of 39 GHz. (c) Comparison between model (including measured BBLNA gain and diode parameters) and measured end-to-end frequency response shows good agreement. (d) Performance across Δ indicates significant RC roll-off due to high R_j , whereas the response across f_0 is relatively constant.

I/Q inputs on a Keysight E8267D VSG.³ The output of the wireline receiver is measured directly by a Keysight MSOS604A oscilloscope operating at 10 GSa/s with a 50- Ω input impedance. The received high-resolution oscilloscope data are rectified about 0 V, and then, a brute-force synchronization algorithm is used to ensure good alignment at the symbol level as well as determining the correct set of samples to keep when downsampling the data by 10 \times . The reported number of errors is the number of errors between the transmitted and received 8b/10b-encoded sequences. A relatively short 8b/10b sequence (length of sequence $N_s = 10^6$) is used because the oscilloscope method used here produces large amounts of data needed to be saved and processed digitally. Assuming that a practical implementation will use an error correcting code, we target a raw BER of 10^{-3} (as high as 10^{-1} may be acceptable for certain applications [30]). Therefore, the measurement setup is sufficient for the application. Fig. 17(b) shows a measured sensitivity of -36 dBm for a BER of 10^{-3} at 1.44 pJ/bit and a sensitivity of -43 dBm for a BER of 10^{-1} .

C. Wireline Receiver With RF LNA

To demonstrate the OTA performance as a function of RF LNA gain, the testbed of Fig. 18(a) was used. The same AWG producing a 1-Gs/s ($N = 6.25E^5$) data stream is upconverted to 39 GHz with the VSG, amplified with a Marki Microwave A-2050 PA, and transmitted with a 12-dBi WR-28 horn antenna to the receiver, situated 3.7 m away. The receiver comprises another 12-dBi WR-28 horn antenna and a COTS

³The I/Q inputs are ac-coupled, so the VSG interprets the input as BPSK by default. I/Q adjustments are needed to produce an OOK signal.

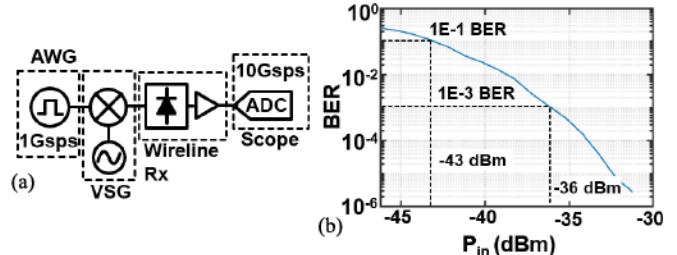


Fig. 17. (a) Wireline receiver BER block diagram. Synchronization and thresholding are performed by postprocessing in MATLAB. (b) BER as a function of power into the detector [analogous to P_{in} in (12)]. The sensitivity of -36 dBm for a BER of 10^{-3} is a record for nonpreamplified Gbps detectors.

Ka -band RF LNA (Pasternack PE15A3300, NF = 2–2.4 dB) followed by a variable attenuation to provide variable RF LNA gain prior to the 50- Ω input impedance wireline receiver. The measured BER versus RF LNA gain from -10 to $+40$ dB and for transmit power levels from -20 to $+10$ dBm is shown in Fig. 18(b). BER initially drops significantly as a function of RF LNA gain due to improvement in SNR, that is, initially, with no preamplification, the circuit is back-end noise dominated [23] due to the extreme conversion loss of the diode detector. As RF LNA gain increases, SNR increases as the circuit becomes increasingly front-end noise dominated (see region between points “c” and “d”). Eventually, a minimum BER of 10^{-5} was reached with 11.5-dB RF LNA gain and transmit power level of $+10$ dBm (at point “d”). As RF LNA gain increases further, BER begins to rise (between points “d” and “e”), which is due to higher order nonlinear effects (exiting the square-law regime) as well as saturation of the BBLNA, resulting in data-dependent errors.

Eye diagrams obtained at each point (“c,” “d,” and “e”) in the BER measurements of Fig. 18(b) are shown in Fig. 18(c)–(e) and help to explain the trends in BER. For low RF LNA gain (point “c”), the SNR is low and there is no opening in the eye diagram—the result is low SNR and high BER of about 10^{-1} . For the optimal RF LNA gain of 11.5 dB (point “d”), the eye has a large opening corresponding to high SNR and a minimum BER of 10^{-5} . For higher RF LNA gain (point “e”), the eye diagram transitions from an SNR-limited regime to an ISI/jitter-limited regime. The region in which ISI becomes significant coincides with both a failure of the square-law assumption for the diode and a saturation of the baseband amplifier. Sequence-dependent BER is observed. In high-gain (SNR) regimes [see Fig. 19(c) and (d)], errors occur almost exclusively for sequences in which the current bit differs from the preceding bit, indicating that performance degradation may be due to poor high-frequency response. Even for low gain, a preference for, e.g., “001” and “110” sequences is shown. Although error-free uncoded BER is not necessarily desirable at the expense of receiver power consumption, future BBLNA prototypes should more thoroughly consider the role of receiver dynamic range on BER. One architecture worth considering is a limiting amplifier, which can be biased to a low level and allowed to saturate but must recover within much less than a symbol period.

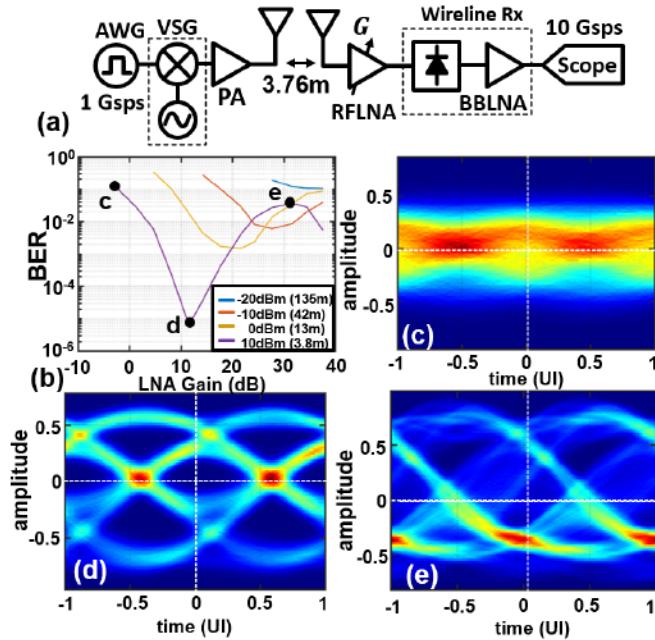


Fig. 18. (a) Block diagram of OTA measurement setup. The antennas are nominal 10-dBi horns, and the receiver has variable RF LNA gain. (b) BER versus RF LNA gain for various transmit power levels indicating points “c,” “d,” and “e” corresponding to eye diagrams in (c)–(e). (c) Eye diagram plotted for a low-gain state at point “c” shows no discernible eye opening, indicating low SNR. (d) Optimal LNA gain of 11.5 dB for high transmit power (point “d”) shows a wide eye opening. (e) In very high-gain states (point “e”), multiple traces are seen crossing the eye opening indicating ISI.

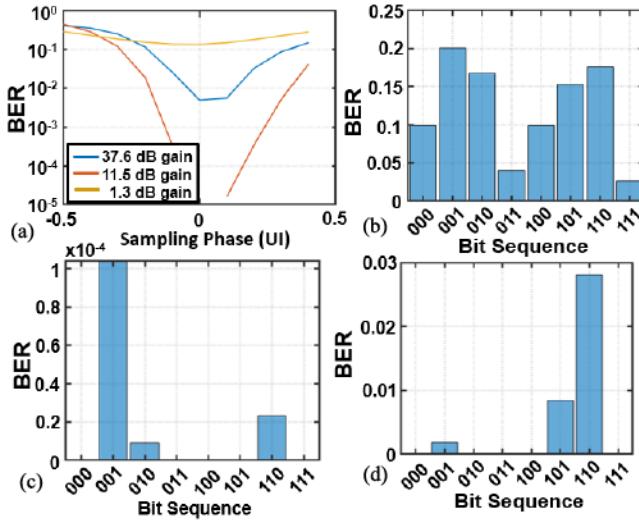


Fig. 19. (a) Bathtub plots showing BER timing dependence for points “c” (yellow), “d” (red), and “e” (blue) from Fig. 18(a). (b–d) Distribution of bit errors (on last bit) across the eight possible 3-bit sequences, normalized to sequence frequency. “b,” “c,” and “d” correspond to the eyes in Fig. 18(c)–(e), respectively. A strong preference for errors where the current symbol differs from the one immediately preceding is observed.

D. Antenna-Coupled Detector With BBLNA

The antenna-coupled receiver shown in Fig. 20(a) integrates a conjugate-matched antenna with the rectifier (without the need for an explicit matching network) and BBLNA and represents the final candidate circuit for scaling in an array.

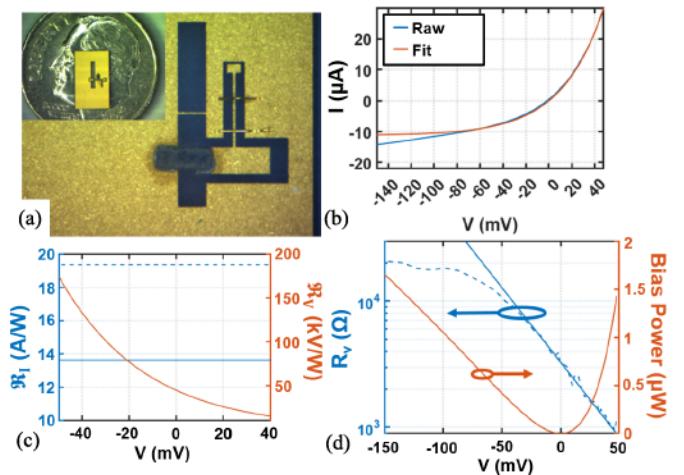


Fig. 20. (a) Fabricated series antenna-coupled receiver. The antenna is conjugate-matched to the diode, which directly spans the slot. (b) In-circuit I – V curves. (c) Derived current and voltage responsivities, \mathfrak{R}_{I0} and \mathfrak{R}_{V0} . (d) $R_v \approx R_j$ and total bias power versus diode bias voltage.

Four of these circuits were fabricated and integrated into a four-element linear array [shown in Fig. 21(a) and (b)]. The elements were staggered to allow for a 0.75λ array spacing. Even with a discrete BBLNA, the array does not require fan-out from the antennas to the circuitry and can therefore be infinitely arrayed along the horizontal axis with modulated mmWave in and buffered Gbps baseband data out. The array pitch is limited by the BBLNA form factor so that, if the BBLNA were monolithically integrated, a 0.5λ pitch could be easily achieved. Due to challenges in manual BBLNA assembly, only one of the four receivers demonstrated satisfactory performance. It is marked with a white rectangle in Fig. 21(a) and (b). The other three receivers in the array will not be discussed further in this article.

I - V curves are shown in Fig. 20(b) and indicate a slightly lower \mathfrak{R}_{I0} [Fig. 20(c)] than the other prototypes of 13.6 A/W, corresponding to n of 1.4. In addition, R_j is also lower (3.2 kΩ), resulting in a significantly lower overall \mathfrak{R}_{V0} of 44.6 kV/W. As with the wireline receiver, the antenna-coupled receiver BBLNA initially oscillated and had to be stabilized. Due to significant variation in the BBLNA fabrication, the antenna-coupled receiver has a different stable bias and dissipates 0.71 mW during operation as opposed to 1.15 mW of the wireline receiver.

From Fig. 20(d), as reverse bias increases, the measured R_v (dashed trace) saturates to approximately 20 kΩ that differs from the model (solid trace), which limits the degradation in η as reverse bias increases. Thus, the detector performance should also saturate with reverse bias. It is unclear precisely why this saturation occurs but could be due to nonuniformity in the Schottky contact or some other parasitic shunt conductance [31]. The radiation pattern is shown in Fig. 21(c) and was measured by normalized angle-dependent \mathfrak{R}_V . It differs significantly from the original simulated pattern of Fig. 7(d) due to the presence of board metallization and the surrounding measurement fixture. Notably, the front-to-back ratio has degraded significantly, and the expected maximum directivity

TABLE III
ENVELOPE DETECTORS IN THE LITERATURE

Detector Type	Ref.	Technology	f_0 (GHz)	Data Rate (Gbps)	RF LNA Gain (dB)	Sensitivity @ 10^{-3} BER (dBm)	P_{DC} (mW)	Efficiency (pJ/bit)
Active	[10]	130nm SiGe BiCMOS	60	22	0	-19	11	0.5
	[33]	130nm CMOS	60	5	0	-24 ^a	14.7	2.94
	[34]	90nm CMOS	60	5	0	-28 ^a	49	9.8
	[35]	250 nm SiGe BiCMOS	60	11.5	0	-15 ^c	27.5	2.4
	[36]	130nm SiGe BiCMOS	60	10	0	-32 ^a	21	2.1
	[11]	200nm GaAs pHEMT	7	2.5	0	-18	N.R. ^b	N.R.
	[37]	40nm CMOS	56	11	18	-30 ^a	41	3.7
	[38]	90nm CMOS	45	4	21	-51 ^a	53.6	13.4
	[39]	65nm CMOS	71	5	10	-37 ^a	40.3	8.1
	[40]	90nm CMOS	60	3.5	24	-40 ^c	108	30.8
	[41]	65nm CMOS	60	3	26	-46	22	7.3
	[42]	180nm SiGe BiCMOS	43	6	30	-56 ^a	57	9.5
	[43]	130nm SiGe BiCMOS	53	6	25	-55 ^c	11 ^b	1.8
Passive	[44]	Si ZBD	9	2.5	0	-17.5	0 ^b	N/A
	[45]	50nm InGaAs mHEMT Schottky	108	24	20	-33 ^a	14.4 ^b	0.6 ^b
	[46]	35nm InGaAs mHEMT Schottky	85	24	0	-1 ^d	0 ^e	N/A
	This Work ^f	GaAs ZBD	39	0.8	0	-36	1.15	1.44

^aEstimated assuming noncoherent Gaussian model

^bNeglects COTS baseband amplifier

^cEstimated from plot

^dInsufficient information to estimate sensitivity for 10^{-3} BER – claimed input power shown instead

^eSampling oscilloscope used directly

^fRefers to the wireline receiver

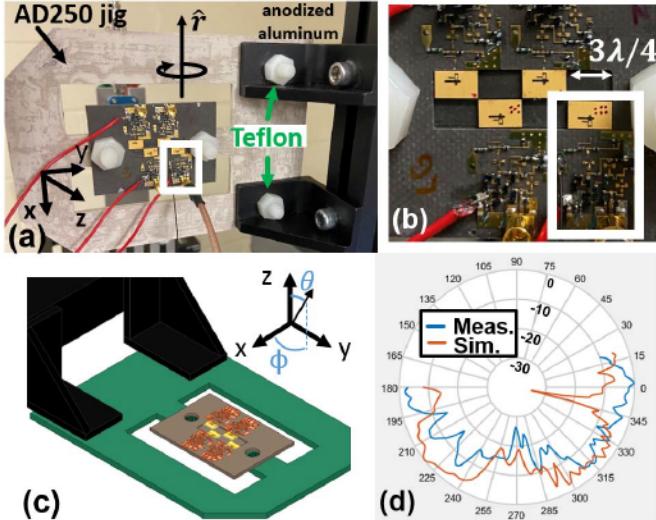


Fig. 21. (a) Actual measurement jig used in BER measurements. Besides the BBLNA metallization, the mounting post is made of aluminum. (b) Antenna array is compact, with only $3/4\lambda$ spacing, with the size dominated by amp design. The functional receiver is indicated with a white box in (a) and (b). (c) Full-wave simulation for in situ radiation simulation showing detail in inset. (d) Simulated and measured radiation patterns show better agreement than measured and original radiation patterns. Disagreement may be due in part to devices on BBLNA board.

from full-wave simulations, including the surrounding board and fixture [Fig. 21(d)], is about 3 dBi.

BER measurements ($N_s = 6.25E^5$) as a function of range and bias were taken for the antenna-coupled receiver, as was

done with the wireline receiver. The experimental setup is shown in Fig. 22(a) and (b), where a 12-dBi WR-28 horn antenna transmits a 39-GHz, 1-Gs/s 8b/10b-encoded OOK waveform at +10 dBm, corresponding to an effective isotropic radiated power (EIRP) of 22 dBm. The element indicated by the white rectangle in Fig. 21 is used as the receiver. A coaxial cable delivers the BBLNA output to the oscilloscope for digitization. The BER results are shown in Fig. 22(c). A modified coherent BER model is used to predict the BER as a function of range. Although the receiver itself is noncoherent, noncoherent OOK BER analysis typically assumes that the noise and the signal are processed identically, i.e., an absolute value operation is applied to the complex baseband representation of the signal and noise [32]. For this system, two revisions to this assumption need to be made.

- 1) For a diode-based envelope detector without preamplification, the predominant source of noise will be thermal additive white Gaussian noise (AWGN) from the diode and baseband amplifier.⁴ In other words, the NF of the system is very high such that the noise received by the antenna is negligible. We say that the noise is dominated by the back end of the system [23].
- 2) The function employed on the complex baseband signal is a squaring function, not an absolute value.

From a detection standpoint (ignoring ISI and the baseband amplifier's frequency selectivity), the immediate consequence of the AWGN is to make the system look like a coherent

⁴As opposed to the typical noncoherent case where the noise distribution is Rician.

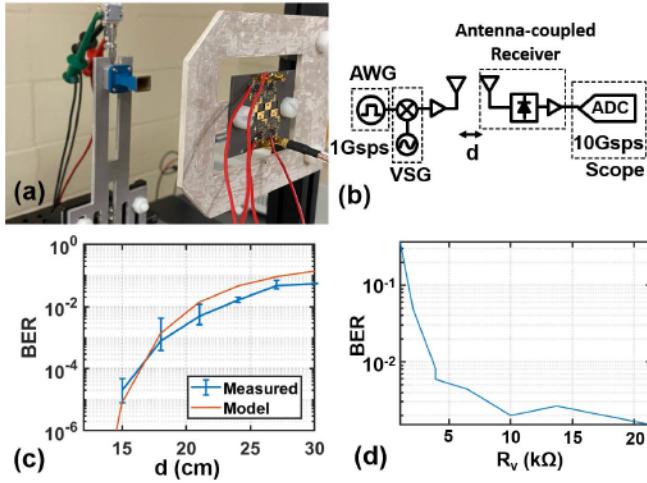


Fig. 22. (a) and (b) Setup for the non-preamplified OTA BER measurements. (c) BER versus range and measured versus coherent BER model (solid trace). The bars show the max and min BERs measured for five BER measurements per range each with PRBS length 1.25E⁵ (for total $N_s = 6.25E^5$). The line is the geometric mean of the individual BER measurements. (d) Non-preamplified BER at 20 cm as a function of R_j obtained by biasing the antenna-coupled receiver.

receiver, even though it is not.⁵ The squaring operation of the rectifier is considered in the following way. The power available at the receive antenna drops as d^{-2} , where d is the distance between transmit and receive. However, the quadratic behavior of the diode causes linear efficiency in received power. Thus, the baseband power falls off as d^{-4} . To first order, the BER of the non-preamplified square-law detector as a function of the SNR at the comparator is given by

$$\text{BER} = Q\left(\sqrt{\frac{E_b}{N_0}}\right) \propto Q\left(\sqrt{\text{SNR}}\right) \quad (15)$$

where Q is the Q -function. For a back-end dominated detector system, the output-referred noise variance is constant with respect to the input signal power [23]. However, the baseband signal power is proportional to the square of the input signal power. Moreover, the power density (and therefore the power received) of a far-field electromagnetic wave falls off as $1/d^2$, where d is the distance between the transmit and receive antennas, and thus,

$$\text{SNR} = \frac{P_{\text{BB}}}{N_{\text{BB}}} \propto \frac{P_{\text{RF}}^2}{N_{\text{BB}}} \propto \frac{P_t^2 d^4}{N_{\text{BB}}}. \quad (16)$$

We, therefore, anticipate that, in an ideal, ISI-free, flat-fading channel, the BER of our square-law detector will fit the following:

$$\begin{aligned} \text{BER} &= Q\left(\sqrt{\beta P_t^2 d^4}\right) \\ &= Q\left(P_t d^2 \sqrt{\beta}\right) \end{aligned} \quad (17)$$

⁵It is well known that coherent receivers outperform noncoherent receivers at a given SNR because of the difference in noise distribution. In this case, however, any possible performance benefit accorded due to the Gaussian noise distribution is compensated by the severely degraded SNR, i.e., the SNR at the comparator is significantly worse than at the antenna. Put another way, the favorable noise distribution is a direct consequence of the unfavorable NF.

where the N_{BB} term is included in the fitting parameter β , which accounts for distance and transmit power, representing the true ratio between received power P_{RF} and $P_{\text{BB}}/N_{\text{BB}}$. Fig. 22(c) shows very good agreement between the observed BER model and (17). Measurements indicate a BER of 10^{-1} out to 30 cm, with an error rate below 10^{-4} below 14 cm. The energy efficiency of the antenna-coupled receiver is 0.88 pJ/bit as it dissipates only 0.71 mW at its stabilized bias. BER under different diode bias conditions was also performed for the antenna-coupled receiver at a range of 20 cm [see Fig. 22(d)]. The BER falls as R_j increases. As shown in Fig. 20(d), R_j for the diode saturates, and thus, the BER remains relatively constant as the diode is further reverse biased. Since the baseband bandwidth is reduced as R_j increases, ISI is expected to worsen, and thus, the BER improvement is probably due to improved baseband SNR.

V. CONCLUSION

Table III compares the performance of the wireline receiver to other state-of-the-art Gbps envelope detectors between X- and W-bands, and it demonstrates the highest sensitivity for non-preamplified passive detectors. This is due in part to the lower bandwidth and carrier frequency used in this work. The effect of a lower carrier frequency relative to the other presented detectors contributes an estimated 1 dB to the sensitivity. However, this sensitivity is likely primarily due to the addition of the high-impedance BBLNA. Moreover, when considering baseband amplification, this receiver dissipates the lowest static power of all published Gbps detectors, only 1.15 mW for the wireline receiver and 0.71 mW for the antenna-coupled receiver. The energy efficiency is very competitive with other presented detectors, even when considering integrated designs, where high-efficiency receivers typically exhibit high data rates (many Gbps). It is very likely that an increase in the data rate can improve energy efficiency, though it may require a more conventional TIA design involving lowered amplifier impedance. More work is also needed to consider the implementation of filtering and gain at f_0 . Moreover, the design intentionally sacrifices dynamic range for lower dc power consumption, and as such, establishing acceptable dynamic range requirements (for the desired minimum BER) is critical for a practical receiver implementation.

In this work, we demonstrated two prototype 800-Mb/s OOK receivers operating at 39 GHz: an antenna-coupled receiver and a wireline receiver. The receivers use diodes to noncoherently detect OOK signals at a carrier frequency of 39 GHz and employ wideband high-Z BBLNAs to drive a 50- Ω load. The total receiver, including the antenna, detector, and BBLNA, fits into a 17 \times 10 mm area and, with slight modifications, could fit into a half-wave array grid. The antenna-coupled receiver achieved a record energy efficiency per distance of 0.049 pJ/bit/cm for an 800-Mb/s data rate while consuming 0.71-mW total power over an 18-cm range and a transmitter EIRP of 22 dBm. The wireline receiver achieved a record sensitivity of -36 dBm (BER of 10^{-3}) for a Gbps-scale non-preamplified receiver. When connected to a horn antenna with 11.5 dB of RF gain, 800-Mb/s

communication is achieved at 3.76 m with a BER of 10^{-5} (indicating that much longer range is possible for a BER of 10^{-3} or even 10^{-1}).

This work demonstrates ultralow-energy, high-data-rate, mmW mobile wireless communication based on low-complexity modulation schemes. The results show that envelope-detector-based OOK receivers can be useful beyond the typical chip-to-chip communications regime, instead proving relevant for longer range mobile wireless networks. Perhaps more importantly, this work shows that large arrays are feasible from a size and power perspective, which is significant because, as has been shown many times, combining a large number of such nonlinear elements can further improve the sensitivity and range. For example, we have recently shown that the sensitivity level of a 1-bit OOK system improves by 2.5–3 dB for every doubling of the number of elements [23]. This scaling trend can be applied to the non-preamplified, fully integrated antenna-coupled receiver presented here, which, for a single element, consumes 0.71 mW and achieves a BER of 10^{-3} at 18 cm and 10^{-1} at 30 cm [see Fig. 22(c)]. However, an array of 1024 such elements would only consume 710 mW while maintaining a BER of 10^{-3} at a range of 6.3 m or a BER of 10^{-1} at almost 10 m—all with no-preamplification, consuming less than a watt of power, and the whole array fitting in an area of approximately 54×32 cm. Also, due to the small parts count and simplistic design, the cost would be low relative to a conventional antenna array.

In order to improve the design in this work for large-scale arrays with hundreds or thousands of elements, a fully integrated RF LNA, detector, and BBLNA should be developed. Importantly, the addition of an RF LNA rapidly increases the range but only needs to provide a modest 11.5 dB gain (in this realization) and a very low saturated output power of -30 dBm, making an ultralow-power (milliwatt scale) RF LNA possible. The BBLNA should maintain low bias levels and should be designed to robustly recover from saturation to minimize BER degradation due to ISI in high-amplitude regimes.

ACKNOWLEDGMENT

The authors would like to thank Diramics for providing the transistors used in this work.

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