

Continuous Liquid Metal Printing for Rapid Metal Oxide TFT Integration

William J. Scheideler¹, Andrew B. Hamlin¹, Youxiong Ye¹, and Simon Agnew¹

¹Dartmouth College, Hanover, NH, USA, william.j.scheideler@dartmouth.edu

Abstract

We present a rapid liquid metal printing process (CLMP) enabling fabrication of high-mobility metal oxide semiconducting channels in less than 3 seconds. We use this process to engineer heterostructure TFTs with channels consisting of 3 nm layers of In_2O_3 and Ga_2O_3 with improved subthreshold slope and enhanced on-state performance ($\mu_{\text{ave}} \sim 14 \text{ cm}^2/\text{Vs}$). We report the influence of deposition temperature and speed, investigating crystallinity and grain morphology of this class of 2D oxide semiconductors. (Keywords: Oxide TFTs, Printed Electronics)

Introduction

Transparent semiconducting metal oxides have emerged as a dominant class of materials with high electron mobility ($> 10 \text{ cm}^2/\text{Vs}$) for driving thin film electronics such as high resolution microdisplays for virtual reality[1]. Vacuum-free, rapid processing could open up opportunities for applying high performance metal oxides in new applications for large-area and mechanically flexible devices. Printed metal oxides can offer higher performance than alternative thin film semiconductors. However, past printing methods for inorganic electronic materials have two major drawbacks: 1) Low temperature processing is largely inhibited by incomplete chemical conversion 2) the process times are very slow-nullifying benefits over vacuum deposition. Here, we present a roller-based liquid metal printing method for fabricating high-mobility metal oxide channel materials at low temperatures and at unprecedented single-second time scales.

Results and Discussion

We present our method for high-mobility oxide semiconductor fabrication known as continuous liquid metal printing (CLMP) that can be operated in a roll-to-roll format at speeds greater than 10 cm/s. Here, we apply this method to generate single layer as well as heterostructure oxides for use as semiconducting channel materials. Figure 1a depicts our continuous oxidation process for producing large-area 2D oxides in nanoscale layers just 3 nm thick in a total process time of less than 3 seconds [2]. In this process, a pure molten metal meniscus is spontaneously oxidized in air while transferring the solid oxide skin to a target substrate where it is

adhered by van der Waals forces. These 2D oxides are highly conductive and highly transparent, making them ideal materials for building high performance metal oxide thin film transistors (TFTs). They also tend to exhibit large plate-like grain morphologies that correlate with their high conductivity and high electron mobility as determined by Hall measurements[2].

This paper builds off our past results by demonstrating high-performance In_2O_3 TFTs printed by roller-based CLMP. Compared to our previous results on dual-sided liquid metal printing[3], this process is novel because it requires no post-annealing. Instead, electrostatic control is achieved via the combination of ultrathin channels and by varying the deposition temperature. We characterize the dependence of TFT device characteristics on the printing temperature and speed, the determining factors in 2D oxide formation. We present a comparison of different deposition temperatures in a plastic substrate-compatible range of 180 – 240 °C. CLMP at these temperatures using liquid gallium as a precursor produces amorphous GaO_x but CLMP with pure indium metal results in polycrystalline In_2O_3 films (Figure 1b) with large grains sizes ($L_{\text{ave}} = 20 \pm 5 \text{ nm}$) relative to their thickness ($\sim 3.3 \text{ nm}$ by AFM), as shown in the histogram in Figure 1c. Multilayers of the In_2O_3 exhibit vertically overlapping grains displaying Moiré fringes – indicating that the crystallites are stacked during deposition rather than crystallized through their thickness.

Our studies of these channels by XRD (Figure 2a) indicate increasing crystallinity with increasing deposition temperature from 180 - 240 °C, but similar grain size ($\sim 7\text{-}8 \text{ nm}$) as estimated by the Scherrer equation. Interestingly, intermediate deposition temperatures (200 and 220 °C) heavily favor the (222) orientation of cubic bixbyite In_2O_3 while the 180 °C and 240 °C conditions exhibit grains with both (222) and (400) orientations. Increasing deposition temperature to 240 °C also changes the oxygen stoichiometry of the film, increasing the percentage of M-O stoichiometric bonding compared with oxygen deficient bonding resulting from oxygen vacancies, as determined by XPS.

Increasing the CLMP deposition temperature from the optimal 200 °C condition to 240 °C results

in positive shifts to the turn on voltage (V_{on}) as well lower on-current and wider hysteresis loops (Figure 2b) for substrate-gated TFTs with top contacts. We also note that increasing the CLMP deposition speed from 5 cm/s to 10 cm/s reduces the channel thickness to ~ 2 nm while reducing speed to 2 cm/s produces thicker channels (~ 4 nm) with more negative V_{on} and poor subthreshold characteristics.

We leverage CLMP to print heterostructures consisting of stacks of 2D metal oxides (In_2O_3 and Ga_2O_3) as a tool to control the electrostatics of these devices without lengthy post-annealing. Heterostructure TFTs consisting of a 3 nm Ga_2O_3 layer capping a 3 nm In_2O_3 channel (Figure 2c) yield devices with 4X steeper subthreshold slope ($SS_{ave} \sim 250$ mV/dec) (Figure 3a) than those with single layer In_2O_3 channels ($SS_{ave} \sim 1000$ mV/dec). The V_{on} is shifted positively by the heterostructure, achieving enhancement mode operation rather than depletion mode. Additionally, the Ga_2O_3 capping layer results in a moderate improvement to the average linear mobility, reaching $14 \text{ cm}^2/\text{Vs}$ compared with $12 \text{ cm}^2/\text{Vs}$ for single layer In_2O_3 channels. In combination with the steeper SS and near 0 V V_{on} , these observations suggest that Ga_2O_3 is an effective material for passivating In_2O_3 's back-channel defects.

2D oxide heterostructures provide an effective mechanism for engineering enhancement mode operation in liquid metal printed In_2O_3 TFTs that otherwise tend to exhibit highly conductive channels with negative turn on voltages as deposited [4]. The GaO_x capping layer is also observed to slightly decrease the optical bandgap (3.73 to 3.69 eV) and increase the work function (30 meV). These could also be consistent with our hypothesis that it passivates In_2O_3 back-channel defects that contribute to the high density of deep states in ultrathin In_2O_3 [5].

The main technological advantage of our CLMP process is its ability to deposit semiconducting 2D oxides directly from a spontaneous oxidation of liquid metal without need for vacuum equipment. Figure 3c compares the process time and temperature reported for other high mobility printed and solution-processed metal oxide transistors. Our work is highlighted in the yellow symbols, showing a thermal budget of just 200°C with a total process time of less than 5 seconds, approximately 2-3 orders of magnitude faster than competing methods that require lengthy anneals, often at higher temperatures

$> 300^\circ\text{C}$. Our process is well within the limits of as plastic substrates, as demonstrated in our previous work using CLMP to print flexible TCOs[2].

Conclusion

In summary, we present a strategy for rapidly fabricating ultrathin metal oxide heterostructure channel TFTs at low-temperatures by continuous liquid metal printing. We investigate the impact of process temperature on the crystallinity of these channel materials and identify their impact on transport in these devices. This ability to control the electrostatics of these channel materials without oxidative post-annealing opens possibilities for manufacturing large area devices such as flexible lightweight displays at low cost with high-volume printing.

Acknowledgments

This research was supported by the National Science Foundation Electronic and Photonic Materials program (Award #2202501) as well as the National Science Foundation Electronics, Photonics, and Magnetic Devices program (Award #2219991). A.B.H is supported by a National Science Foundation Graduate Research Fellowship.

References

- [1] H. Shishido *et al.*, "21-1: Invited Paper: 5291-ppi Microdisplay Using CAAC-IGZO FET with Channel Length of 60 nm," *SID Symposium Digest of Technical Papers*, vol. 51, no. 1, pp. 293–296, 2020, doi: 10.1002/sdtp.13861.
- [2] Y. Ye, A. B. Hamlin, J. E. Huddy, M. S. Rahman, and W. J. Scheideler, "Continuous Liquid Metal Printed 2D Transparent Conductive Oxide Superlattices," *Advanced Functional Materials*, vol. 32, no. 33, p. 2204235, 2022, doi: 10.1002/adfm.202204235.
- [3] A. B. Hamlin, Y. Ye, J. E. Huddy, M. S. Rahman, and W. J. Scheideler, "2D transistors rapidly printed from the crystalline oxide skin of molten indium," *npj 2D Mater Appl*, vol. 6, no. 1, Art. no. 1, Mar. 2022, doi: 10.1038/s41699-022-00294-9.
- [4] Y. Tang, C.-H. Huang, and K. Nomura, "Vacuum-Free Liquid-Metal-Printed 2D Indium-Tin Oxide Thin-Film Transistor for Oxide Inverters," *ACS Nano*, Feb. 2022, doi: 10.1021/acsnano.1c11205.
- [5] W. J. Scheideler, A. B. Hamlin, Y. Ye, J. E. Huddy, and M. S. Rahman, "Liquid-Metal-Printed Ultrathin Channel In_2O_3 Transistors for Large Area Transparent Electronics," in *2022 6th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)*, Mar. 2022, pp. 176–178. doi: 10.1109/EDTM53872.2022.9797927.

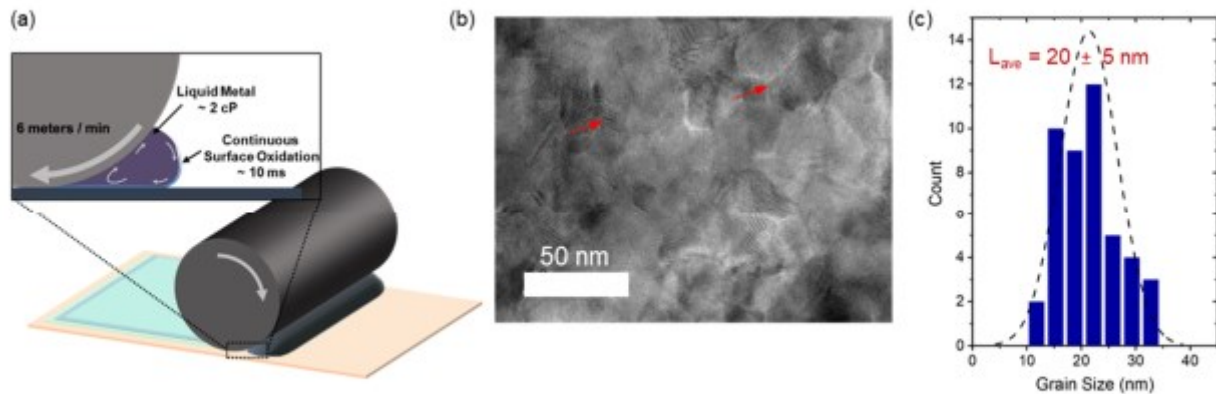


Figure 1: (a) Continuous liquid metal printing (CLMP) process transferring 2D oxide semiconductors. (b) HRTEM image of multilayer $\text{In}_2\text{O}_3/\text{Ga}_2\text{O}_3$ CLMP film with arrows highlighting Moiré fringes from overlapping crystallites. (c) Histogram of grain sizes and normal distribution fit observed from multiple HRTEM images of CLMP In_2O_3 films.

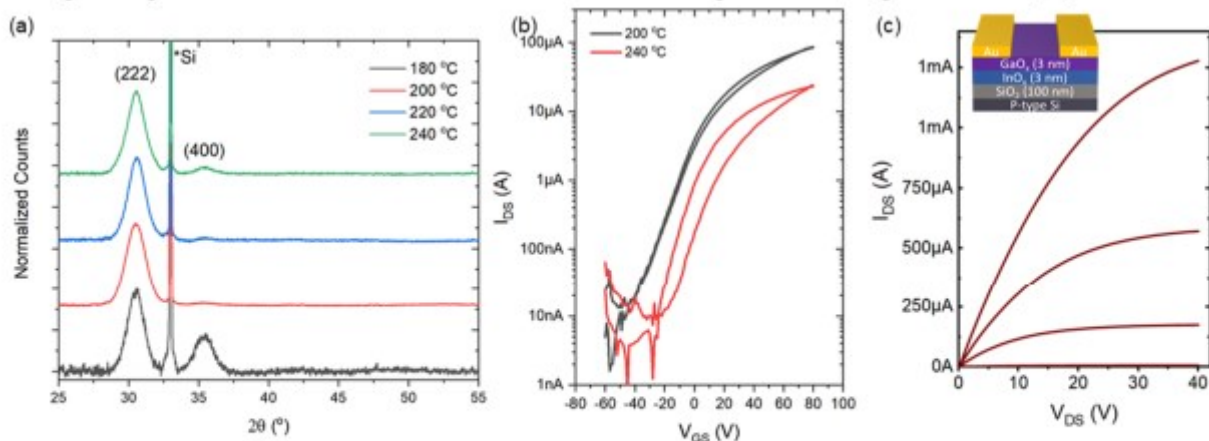


Figure 2: (a) XRD spectra of CLMP 2D InO_x as deposited at various temperatures. (b) Transfer curves of TFTs with 3 nm thick In_2O_3 channels deposited at 200 °C and 240 °C with no post-annealing. (c) Output curve of $\text{InO}_x / \text{GaO}_x$ TFT.

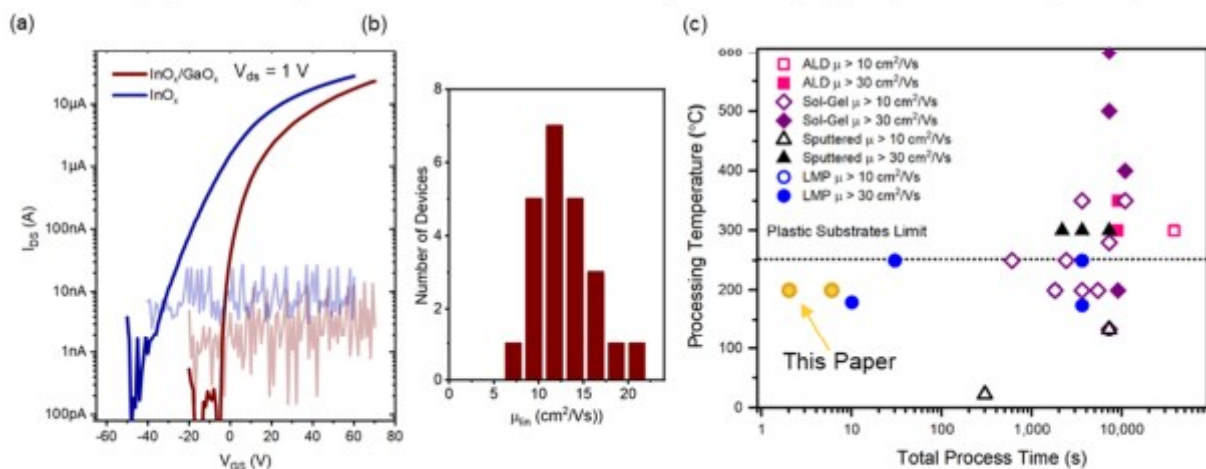


Figure 3: (a) Transfer characteristics of representative top contact substrate gated (100 nm, SiO_2) 3 nm thick In_2O_3 vs. bilayer ($\text{In}_2\text{O}_3 / \text{Ga}_2\text{O}_3$) transistors fabricated with CLMP at 200 °C with no post-annealing. (b) Histogram of linear mobility of bilayer ($\text{In}_2\text{O}_3 / \text{Ga}_2\text{O}_3$) transistors (c) comparison of processing times and temperatures for In_2O_3 -based TFTs reported in literature.