Bottom-up synthesis of mesoscale nanomeshes of graphene nanoribbons on germanium

Vivek Saraswat[1], Austin J. Way[1], Xiaoqi Zheng[1], Robert M. Jacobberger[1], Sebastian Manzo[1], Nikhil Tiwale[2], Jonathan H. Dwyer[1], Jason K. Kawasaki[1], Chang-Yong Nam[2], Padma Gopalan[1], and Michael S. Arnold[1*]

1. Department of Materials Science and Engineering, University of Wisconsin−Madison, Madison, Wisconsin 53706, United States
2. Center for Functional Nanomaterials, Brookhaven National Laboratory, Upton, New York, 11973, USA

* Author to whom correspondence should be addressed: michael.arnold@wisc.edu

Abstract

The synthesis of functional graphene nanostructures on Ge(001) provides an attractive route toward integrating graphene-based electronic devices onto complementary metal oxide semiconductor (CMOS)-compatible platforms. In this study, we leverage the phenomenon of the anisotropic growth of graphene nanoribbons from rationally placed graphene nanoseeds and their rotational self-alignment during chemical vapor deposition to synthesize mesoscale graphene nanomeshes over areas spanning several hundred square micrometers. Lithographically patterned nanoseeds are defined on a Ge(001) surface at pitches ranging from 50 to 100 nm, which serve as starting sites for subsequent nanoribbon growth. Rotational self-alignment of the nanoseeds followed by anisotropic growth kinetics cause the resulting nanoribbons to be oriented along each of the equivalent, orthogonal Ge⟨110⟩ directions with equal probability. As the nanoribbons grow, they fuse, creating a continuous nanomesh. In contrast to nanomesh synthesis *via* top-down approaches, this technique yields nanomeshes with atomically faceted edges and covalently-bonded junctions, important for maximizing charge transport properties. Additionally, we simulate the electrical characteristics of nanomeshes synthesized from different initial nanoseed-sizes, size-

polydispersities, pitches, and device channel lengths to identify a parameter-space for acceptable on/off ratios and on-conductance in semiconductor electronics. The simulations show that decreasing seed diameter and pitch are critical to increasing nanomesh on/off ratio and on-conductance, respectively. With further refinements in lithography, nanomeshes obtained *via* seeded synthesis and anisotropic growth are likely to have superior electronic properties with tremendous potential in a multitude of applications such as radio frequency communications, sensing, thin-film electronics, and plasmonics.

Introduction

The synthesis of sub-10 nm wide armchair graphene nanoribbons on Ge(001) using chemical vapor deposition (CVD) provides a metal-free, industry-compatible route toward fabricating semiconducting graphene nanoribbon devices.[1,2] Previous work has demonstrated that at temperatures ~ 900 °C, the pyrolysis of hydrocarbon precursors (*e.g.* CH_4, C_2H_4) on the Ge(001) surface leads to the anisotropic growth of armchair graphene nanoribbons that self-align along one of the equivalent, orthogonal Ge⟨110⟩ directions and that can be as narrow as 1.7 nm.[3] The devices fabricated from such CVD-synthesized graphene nanoribbons have yielded promising characteristics – on-conductance (G_{on}) = 5 μS and on/off ratio (G_{on}/G_{off}) = 2×10^4.[4,5] However, the spontaneous (or unseeded) growth of graphene nanoribbons that occurs during CVD causes polydispersity in nanoribbon length and width, presumably due to polydispersity in the size of nucleation sites that are formed from carbon-based surface residual adsorbates, unsynchronized nucleation that can occur over the duration of the CVD growth, and/or minor site-to-site variation in growth rates. Furthermore, spontaneous nucleation leads to nanoribbons that are randomly oriented toward one of the two Ge⟨110⟩ directions. Moreover, such a growth offers no control

over the placement and orientation of the nanoribbons since nanoribbons tend to nucleate at arbitrary locations on the surface.[6]

These drawbacks must be overcome to incorporate graphene nanoribbons into integrated circuits, wherein the precise location of each transistor is pre-determined in order to register the contacts and subsequent interconnect layers. Furthermore, in order to be competitive with existing technologies, each nanoribbon field-effect transistor (FET) would need to be comprised of several nanoribbons in order to deliver a high drive current – necessitating the parallel alignment of individual nanoribbons.[7] In order to overcome these drawbacks, it has been suggested that the growth and alignment of graphene nanoribbons on Ge(001) during the CVD process can be manipulated by initiating synthesis from rationally placed graphene nuclei or nanoseeds and tuning the initial size and crystallographic orientation of the nanoseed-lattice on the Ge(001) surface.[8,9] For instance, we previously reported that a graphene nanoseed with a diameter *larger* than a critical size (~18 nm), that has its lattice's armchair direction oriented within 3° of one of the equivalent Ge⟨110⟩ directions (*i.e.* $0° \leq |\theta_{seed}| \leq 3°$, in Figure 1), upon CVD growth, results in an anisotropic armchair graphene nanoribbon whose long axis (or armchair direction) is aligned toward that particular Ge⟨110⟩ direction. On the contrary, if a graphene nanoseed has its armchair direction misaligned with its nearest Ge⟨110⟩ direction (*i.e.* $7° \leq |\theta_{seed}| \leq 23°$), the CVD growth yields low aspect, parallelogram-like graphene crystals (see SI Figure 1).[8,9]

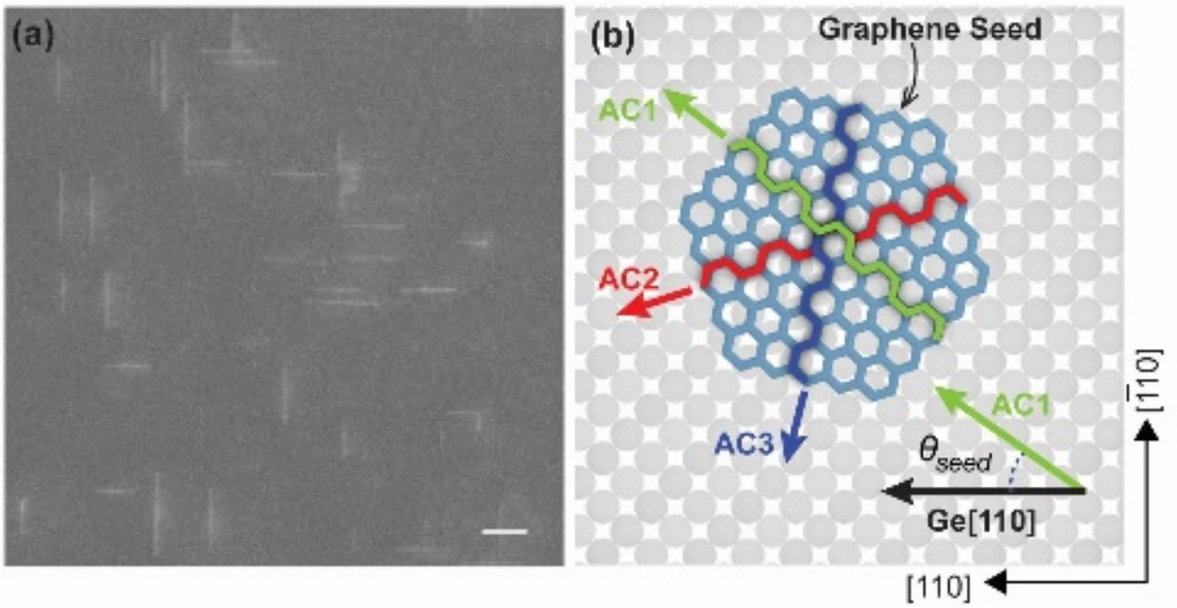


Figure 1: (a) A representative scanning electron microscopy (SEM) image of an unseeded graphene nanoribbon growth on Ge(001) via CVD. (b) Schematic of a graphene nanoseed on Ge(001). The three possible armchair directions of the nanoseed-lattice are highlighted in different colors (denoted as AC1, AC2, and AC3). Scale bar in (a) is 200 nm.

In the same work, we also reported that upon reducing its initial diameter to < 18 nm, the nanoseed, regardless of its initial orientation on the Ge(001) surface, is able to rotate and self-align its armchair direction with either of the equivalent Ge⟨110⟩ directions, resulting in a 50-50 split of nanoribbons oriented orthogonally with each other. [10] Although the driving factors dictating the seed-rotation are not yet clear, it is believed that seed rotation occurs because alignment of the armchair direction of the nanoseed parallel to Ge⟨110⟩ leads to an energetically stable orientation. [11] When the nanoseed sizes are reduced, the kinetic barrier associated with nanoseed-rotation also decreases, allowing the nanoseeds to rotate relatively freely and thus enabling the self-alignment of the armchair direction of nanoseeds with any one of the two Ge⟨110⟩ directions.[10]

Whereas use of graphene nanoribbons in high-performance logic and radio frequency (RF) devices is likely to require sub-5 nm widths with short channel lengths, [7] there are a plethora of applications wherein the semiconducting nature of graphene nanoribbons might be harnessed at longer channel lengths (L_{ch} > 1 μm); e.g., thin-film electronics, flexible electronics, biosensors, and plasmonics.[12] While aggregates of surface-synthesized [13,14] and films of solution processed nanoribbons [15,16] have been considered as promising candidates in this realm of applications because of their ease of synthesis and deposition, the lack of covalent bonding between the constituent nanoribbons degrades the charge transport mobility because of the large resistance associated with inter-ribbon hopping. Here, a graphene nanomesh with covalently bonded junctions might be a better alternative for achieving high mobility, on-current, and on/off ratios. [17–21] In the literature, several techniques to synthesize graphene nanomeshes have been demonstrated such as block copolymer lithography, [22] bottom-up polymerization, [23,24] and barrier-guided CVD.[25]

In this study, we build upon our previous work that demonstrated the phenomenon of graphene nanoseed self-rotation on Ge(001) to synthesize orthogonally oriented graphene nanoribbons that merge together into a seamless interconnected mesh. Although a similar concept has been recently demonstrated using organic seeds as initiating sites for nanoribbon synthesis, [26] we utilize graphene nanoseeds patterned at regular, rationally controlled, and tunable pitch using electron-beam lithography to obtain nanomeshes with well-defined nanoribbon periodicity, leading to better control and consistency over the resulting structure. We demonstrate that the interconnected regions of the nanomesh can provide a percolating pathway for charge carriers over lengths > 20 μm and in principle, can be scaled over an entire 300 mm wafer. Furthermore, in order to identify future avenues for improving the synthesis and semiconducting properties of the nanomesh, we simulate charge transport through the nanomeshes fabricated with nanoseeds of different sizes,

polydispersities, pitches, and arrangements and reveal reasonable pitches/seed-sizes necessary to obtain sufficiently large on/off conductance modulation and on-state conductance for different applications. Through these simulations, we reveal that nanoseed pitches < 50 nm are crucial to obtain on/off conductance modulation > 100. Surprisingly, even a substantial polydispersity in nanoseed-size does not significantly affect the on/off conductance modulation. Even higher on/off conductance modulation using smaller seeds based on organic molecules such as pentacene, C_{60}, and other polycyclic aromatic hydrocarbons might be possible, provided that viable methods to rationally place these molecules on Ge(001) are developed. Overall, we demonstrate a proof-of-concept technique for synthesizing a graphene nanomesh on a technologically relevant Ge(001) wafer using CVD. Nanomeshes synthesized by this approach possesses atomically faceted edges, which is a pre-requisite to achieve superior charge transport properties and can be readily scaled for wafer-scale integration into semiconductor electronics.[27,28]

Results and Discussion

Nanofabrication of graphene nanoseeds

Figure 2 shows an overview of the nanofabrication process to create graphene nanoseed arrays on Ge(001). To describe briefly, monolayer graphene grown on Cu foil at 1050 °C is wet-transferred to a Ge(001) wafer piece using a sacrificial polymer layer (polymethyl methacrylate (PMMA) in chlorobenzene) as a support membrane. Thereafter, PMMA is removed with acetone and acetic acid in order to obtain a relatively residue-free, pristine graphene layer on Ge(001). Next, 1% PMMA (molecular weight of 950 kg mol^{-1}) in chlorobenzene is spin-coated on graphene/Ge(001) at 4000 rpm, yielding a 50 nm thick PMMA layer which is used as an electron-beam resist. Prior to electron-beam exposure, the sample is baked at 185 °C for 90 s to remove residual solvent. The patterns used in this study are comprised of an array of nanoseeds at pitch, *P*, of 50, 75 and 100

nm, in which alternate rows are displaced by $0.5\times P$. While theoretically the extent of these patterns can be scaled over areas of several mm^2 or more, depending on electron-beam write speed, here we limited the field area of the patterns to be 30 μm × 30 μm as a proof of concept. These patterns are then developed in an isopropyl alcohol:methyl isobutyl ketone (3:1 ratio) solution at 0 °C for 70 s. The development process removes the regions of PMMA exposed by the electron-beam, creating an array of holes in PMMA, commensurate with the desired pattern. After the development, 10 nm of Ni is evaporated in these holes at a background pressure of < 2 μTorr using an electron-beam evaporator. Liftoff is then carried out by soaking the samples in hot acetone (~ 60 °C) for 1 h followed by mild sonication, yielding Ni dots on graphene, which serve as etch masks (Figure 2d). Regions of graphene unprotected by Ni dots are then removed using an O_2 reactive ion etch (RIE), at 50 W for 30 s. Lastly, Ni dots are etched in a dilute aqua regia solution (3 parts HCl : 2 parts deionized H_2O : 1 part HNO_3) for 135 s followed by three sequential deionized water rinses, exposing the underlying graphene nanoseeds.

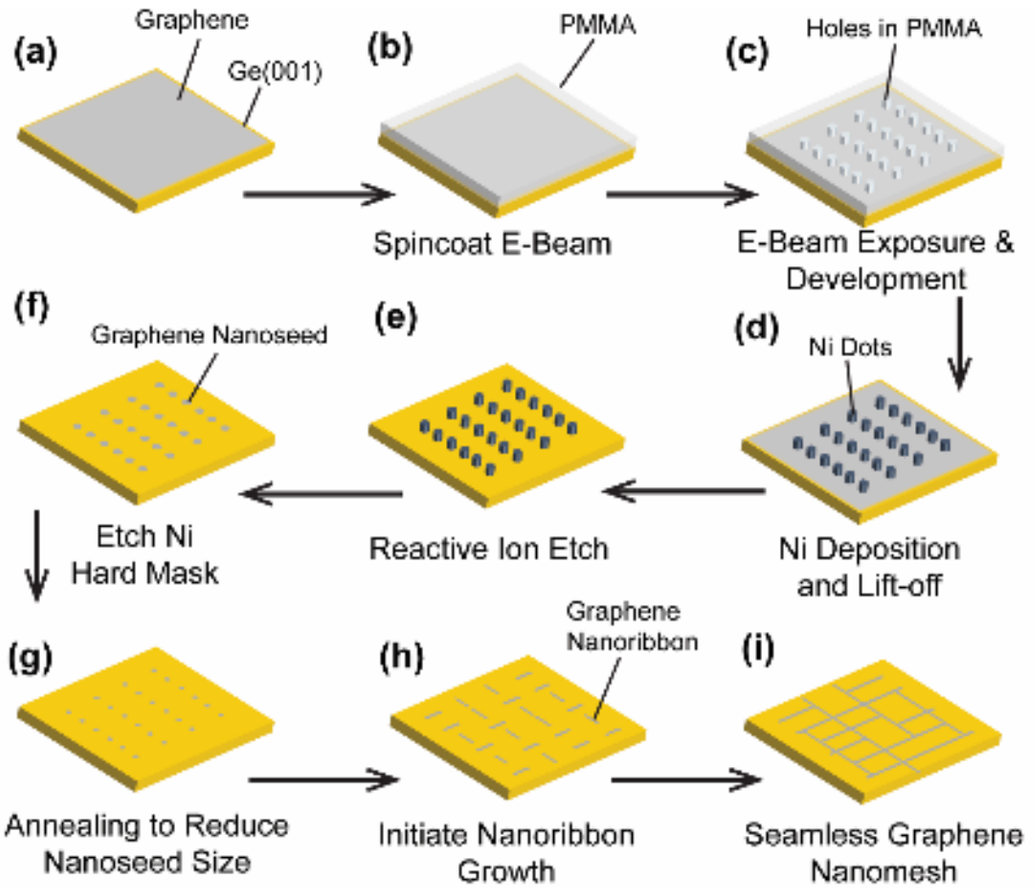


Figure 2: Schematic of nanofabrication of graphene nanoseeds on Ge(001) and subsequent CVD synthesis of graphene nanomesh.

CVD synthesis of graphene nanomesh

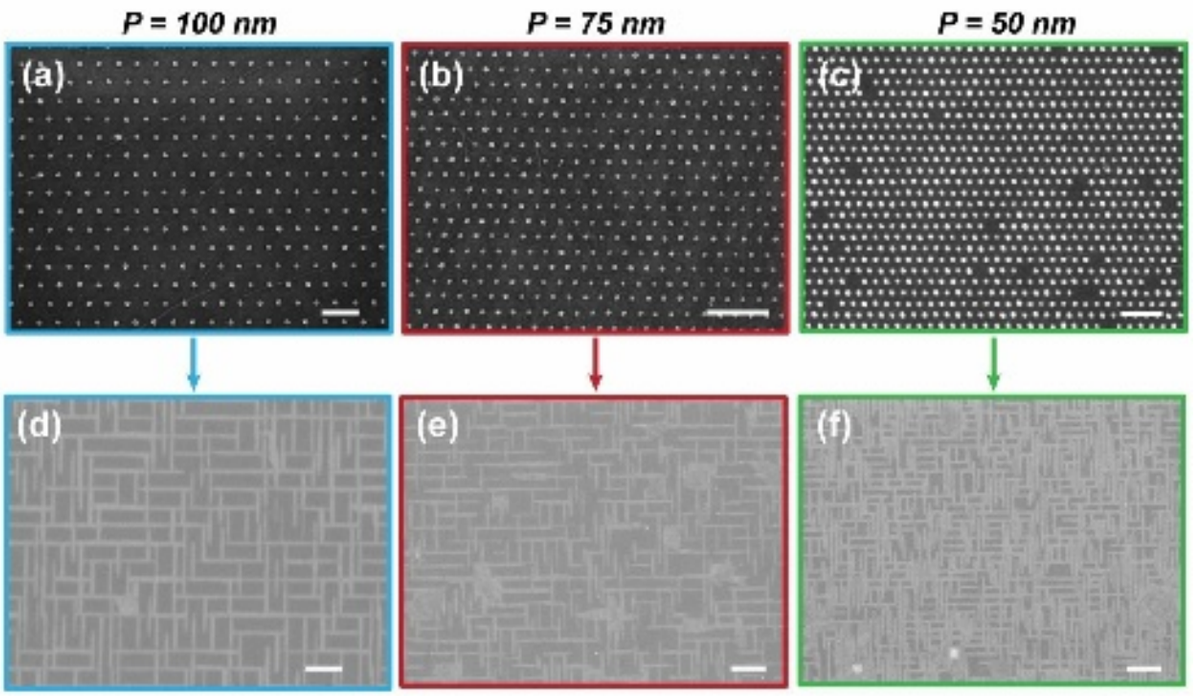
In order to synthesize nanomeshes from these nanoseed arrays, samples are first annealed in an Ar/H_2 atmosphere at 910 °C for ~ 30 min in a tube furnace of inner diameter 34 mm. Annealing not only removes residual adsorbates on the Ge(001) surface, necessary for high-quality anisotropic nanoribbon growth,[29] but also concomitantly etches and desirably decreases the diameter of the graphene nanoseeds.[30] Before annealing, the nanoseed diameter is approximately 30 nm, as analyzed from the data shown in Figure 3a-c). After 30 min of annealing, the diameter is reduced to approximately 12 nm, based on a measured diametric etch rate of 0.6 nm min^{-1}

reported previously. [9] , below the threshold of 18 nm needed for self-rotation of the seeds. Subsequently, nanoribbon growth is initiated by flowing 2 sccm of CH_4 (purity of 99.999%). The nanoribbon growth rates in the length and width directions at this CH_4 flow rate are estimated to be 17 and 0.8 nm h^{-1}, respectively. From Raman characterization of CVD-synthesized nanoribbons on Ge(001) initiated both with[31] and without[1] seeds, it is known that these nanoribbons are graphene. Furthermore, in our previous works[1,6,31] we have demonstrated that these nanoribbons have smooth, faceted armchair edges and are semiconducting in nature. A nanoribbon growth duration of 180 min is used for P = 100 nm and 150 min for P = 50 and 75 nm samples, which is sufficiently long for the nanoribbons to interconnect. The covalent bonding of the nanoribbon junctions (as opposed to van der Waals contact) is expected in these syntheses since graphene islands nucleated on all germanium facets (*i.e.*, Ge(001), [32,33] Ge(110), [34,35] and Ge(111) [36]) are proven to seamlessly grow into a monolayer with atomically continuous grain boundaries upon a sufficiently long CVD growth.

Figures 3 d-f show nanomeshes synthesized by CVD initiated from the nanoseed arrays shown in Figure 3 a-c, respectively. As expected, we see that (i) the seeds primarily evolve into high-aspect ratio nanoribbons (as opposed to low-aspect ratio parallelograms) and (ii) the nanoribbon orientations are evenly split among each of the equivalent Ge⟨110⟩ directions. Both observations (i) and (ii) verify the nanoseed rotation. Moreover, a continuous percolating path is observed at all pitches, consistent with covalent bonding at the junctions and confirming the validity of our approach.

In some instances, we see Ni nanodots are missing – presumably due to imperfect liftoff and poor adhesion of metals with graphene; [37] however, the overall yield is high enough to not lead to any major discontinuities in the nanomeshes. Graphene islands observed in some cases are likely due

177 to nanoseeds larger than the critical size of 18 nm (which do not rotate and rather evolve into
178 isotropic crystals [8]), or in some cases due to lateral nanoribbons merging into each other; the latter
179 being more profound in dense nanomeshes with P = 50 nm.
180



181

182 **Figure 3:** CVD of graphene nanoribbons from nanoseeds fabricated using Ni etch masks at
183 different pitches (P). The anneal duration is 30 min, while the growth duration is 180 min for a,d
184 and 150 min for b, c, e, f. All scale bars are 200 nm.

185 The initial nanoseed-size can also be manipulated to yield nanomeshes with varying degrees of
186 nanoseed-rotation and nanoribbon widths. SI Figure 2 shows how increasing nanoseed size leads
187 to fewer nanoseeds rotating, ultimately yielding just parallel stipes of graphene that form because
188 the nanoseeds do not rotate when they are large (as discussed in SI Figure 1). Such size-tunable
189 control over nanoseed rotation might offer promising avenues toward fabricating aligned

nanoribbon arrays and nanomeshes on a single substrate. For instance, aligned arrays of wide nanoribbons might be used as interconnects for power delivery in electronic devices.

Fabrication and measurement of nanomesh devices

In order to confirm that these nanomeshes indeed form a continuous percolating network for charge carriers and to further understand their electronic properties, we measured charge transport characteristics by fabricating long channel transistors. Nanomeshes synthesized by CVD on Ge(001) are wet-transferred to a SiO_2/Si substrate using PMMA-GMA (poly-(methyl methacrylate)- glycidyl methacrylate) copolymer as a support membrane. The details of the transfer process are described elsewhere.[31] Subsequently, we fabricated contacts by depositing 20 nm Pd using a transmission electron microscopy (TEM) grid (mesh 400) as a shadow mask. A representative image of the transferred nanomesh on 90 nm SiO_2/Si and an array of Pd contacts is shown in Figure 4a. As expected, the transfer process occasionally introduces wrinkles and tears in the nanomesh (indicated by blue and red arrows, respectively). Wrinkles may also form in the nanomesh when it is cooled from synthesis temperature (910 °C) to room temperature after growth, due to the differences in thermal expansion coefficients between Ge and graphene.[38,39] We do not expect the tears to significantly degrade the on-conductance of nanomeshes because they are sparse. With future optimization of transfer protocols, it should be viable to transfer the nanomeshes with near-perfect fidelity.

Note that nanoribbons are not clearly resolved on SiO_2 because of surface charging during SEM. Figure 4b shows the transfer characteristics of a representative nanomesh device with P =100 nm, channel length (L_{ch}) = 25 μm and channel width (W_{ch}) = 36 μm at source-drain voltage (V_{DS}) = -0.1 V. For a gate voltage (V_G) sweep between -50 and 50 V, an on/off ratio of 13 is measured, which is comparable to the on/off ratio ~ 10 seen in nanomeshes synthesized by molecule initiated

bottom-up CVD on Ge(001).[26] Furthermore, we observe an on-state conductance (G_{on}) of 1.6 μS, indicating that our nanomeshes are continuous and can be utilized in long-channel charge transport applications. As a first approximation, the lower limit of field-effect mobility (μ) of our nanomesh can be estimated using a simple parallel plate capacitor model,

$$\mu = \frac{1}{C_{ox}/_{A}} \times \frac{L_{ch}}{W_{ch}} \times \frac{dG_{DS}}{dV_G}$$

Where C_{ox} is the oxide capacitance, G_{DS} channel conductance at given V_G, and $\frac{dG_{DS}}{dV_G}$ the slope of the linear region in Figure 4b (~ 0.04 μS V^{-1}). Based on this model, we estimate the lower bound on μ as 0.7 cm^2 V^{-1} s^{-1}, which is comparable to or better than other nanoribbon thin-film transistors synthesized by bottom-up CVD or polymerization[13,14,26,40]. Nanomeshes synthesized with longer growth duration, which lead to wider nanoribbons, improve the μ by over an order of magnitude to ~12 cm^2 V^{-1} s^{-1}, but lead to degraded on/off ratio ~ 6 (SI Figure 3). While the primary objective of this paper is to demonstrate proof-of-concept synthesis of CVD nanomeshes, we anticipate that the electronic properties can be vastly improved by further refining of synthesis and device integration.

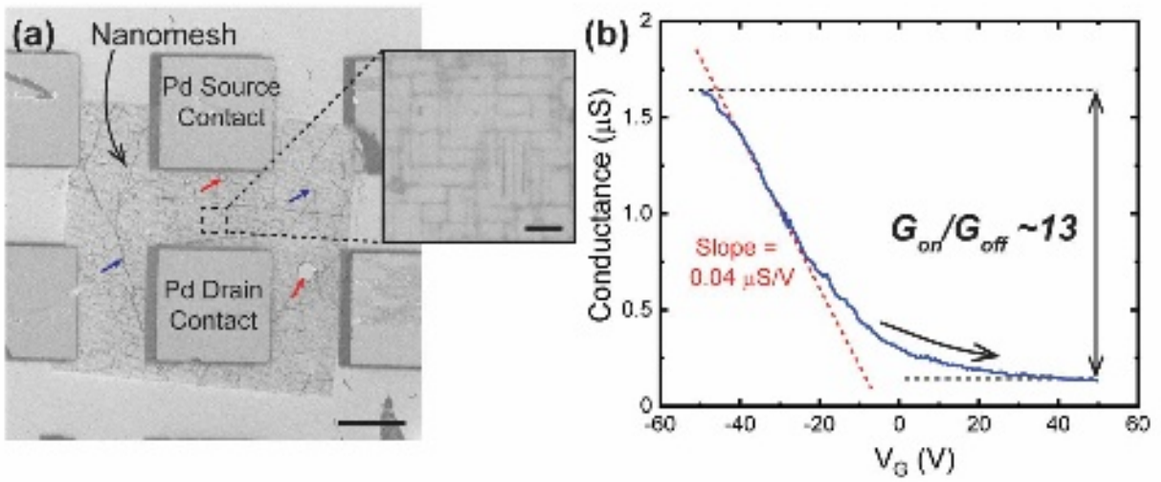


Figure 4: (a) SEM image of a 90 μm × 90 μm graphene nanoribbon mesh transferred on SiO_2/Si substrate with an array of Pd grids deposited on top. A magnified image of the nanomesh is shown in the inset. (b) Forward sweep transfer characteristics of a representative nanomesh with P = 100 nm. The scale bars in (a) and (a, inset) are 20 μm and 200 nm, respectively.

Simulation of charge transport through graphene nanomesh

To motivate research toward further improving the electronic performance of such nanomeshes, we perform simulations of charge transport through nanomeshes fabricated from nanoseeds of different sizes, polydispersities, pitches, and architectures. Additionally, the effect of FET channel length on on/off ratio (G_{on}/G_{off}) and G_{on} is investigated. Different electronic applications demand considerably different G_{on} and G_{on}/G_{off}. Therefore, it will be crucial to tune nanoseed sizes and pitches depending on the desired application.

In our model, nanoseeds are placed in a regular array and are randomly assigned a growth direction along one of the two orthogonal Ge⟨110⟩ directions, with equal weighting. To capture a broad range of possibilities, we simulate nanomeshes with mean nanoseed sizes (μ_{seed}) and

polydispersities (σ_{seed}) ranging from 1 – 9 nm and 0 – 4 nm, respectively. For a given combination of μ_{seed} and σ_{seed}, nanoseeds are generated using a normal distribution, ~$N(\mu_{seed},\sigma_{seed})$, in which negative seed sizes are assumed to be overetched and thus disappear from an array. Furthermore, we assume mean nanoribbon length-growth rate (μ_l) and width-growth rate (μ_w) as 18.2 and 0.81 nm h^{-1}, respectively, in accordance with experimentally measured data. [9] Next, we estimate the polydispersity in nanoribbon length- and width-growth rates from experimentally measured polydispersity in growth rates of nanoribbons initiated from organic molecules such as polycyclic aromatic hydrocarbons (*i.e.*, monodisperse nanoseeds). [31] This is conceivable because in the case of nanoribbons initiated from monodisperse, organic molecules, the measured polydispersity in growth rates is only due to the underlying mechanisms of nanoribbon growth (*e.g.*, nanoribbon-Ge surface interactions, surface roughness, presence of steps, and nanofaceting), in which the length and width of the nanoribbons are not perturbed by polydispersity in the size of the nanoseeds themselves. These normalized polydispersity values, σ_l and σ_w, are estimated to be 1.65 and 0.17 nm h^{-1}, respectively. Consequently, in our model, nanoseeds are randomly assigned growth rates in the length (R_l) and width (R_w) direction with normally distributed probabilities with parameters (18.2, 1.65) nm h^{-1} and (0.81, 0.17) nm h^{-1}, respectively. The nanoribbons grow along the length direction until they meet another nanoribbon and grow along the width direction for the entire duration of the growth (t_{growth}). In the model, t_{growth} depends on the pitch (P) and is given as t_{growth} = $0.0375\times P$ h–nm^{-1}. This dependence has been optimized so that the entire nanomesh forms a continuous percolating network without discontinuities. The point where nanoribbons meet is labeled as a node. Figure 5Figure shows different stages of nanoribbon evolution and nanomesh formation in the model, with nodes highlighted in blue.

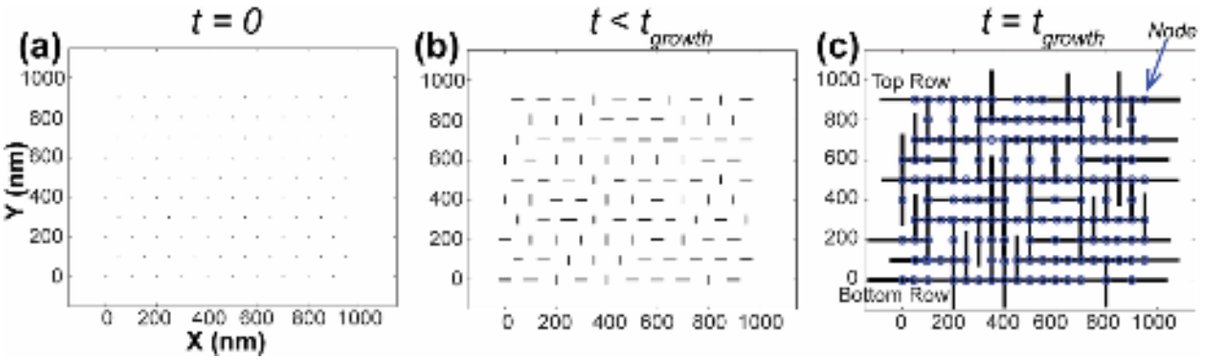


Figure 5: Different stages of nanoribbon evolution and nanomesh formation for μ_{seed} = 5 nm, σ_{seed} = 2 nm, and P = 100 nm. The blue circles in (c) indicate nodes where two nanoribbons meet and fuse.

To model the charge transport properties of the nanomeshes, we develop a node-branch resistor network model in which (1) the branches are the nanoribbon segments connecting the nodes in Figure 5c and (2) the on- and off- states are treated separately. In the on-state, the conductance of each branch is scaled by the length (L) and width (w) of the connecting nanoribbon segment as $G_{on}^{segment} = 1\frac{w}{L}$, where 1 is the normalized sheet conductance of the nanoribbon in the on-state. For a FET at small source-drain bias and in the long-channel regime (channel resistance >> contact resistance), the on-off conductance modulation ratio will scale exponentially with the bandgap, E_g, such that $G_{on}^{segment} / G_{off}^{segment} = \exp\left(\frac{E_g}{2kT}\right)$, where k is Boltzmann's constant and T is temperature, which is designated as 300 K. Empirically, it has been found that E_g varies inversely with nanoribbon width (w) as $E_g \approx \frac{\alpha}{w}$, where α is a constant equal to 3.2 eV nm.[4,41] Thus, in the off-state, the conductance of each segment is set as $G_{off}^{segment} = \exp\left(\frac{-\alpha}{2wkT}\right)\frac{w}{L}$. Kirchoff's current equations are formulated for the entire network and solved separately in the on- and off-states to calculate the small-bias on-conductance of the nanomesh (G_{on}^{mesh}) and the off-conductance of the nanomesh (G_{off}^{mesh}) between the top and bottom rows of nodes. Each

instance of nanomesh growth for a given set of conditions is simulated ten times, and median G_{on}^{mesh} and $G_{on}^{mesh}/G_{off}^{mesh}$ values are plotted in the subsequent sections.

Effect of varying nanoseed pitch and size at a fixed nanoseed polydispersity and fixed channel length

Figure 6 shows the effect of varying the P at a fixed σ_{seed} and fixed channel length and channel width ($L_{ch} = W_{ch} = 1000$ nm) on G_{on}^{mesh} and $G_{on}^{mesh}/G_{off}^{mesh}$. Here, P is varied from 20 nm to 200 nm. As P increases, both G_{on}^{mesh} and $G_{on}^{mesh}/G_{off}^{mesh}$ decrease. While the former decreases because of a reduction in the number of parallel conduction pathways at longer P, the latter decreases because of the necessity of longer t_{growth} at higher P in order to form an interconnected pathway, which leads to wider nanoribbons with smaller bandgaps and therefore lower $G_{on}^{mesh}/G_{off}^{mesh}$. A notable exception to this trend is observed for G_{on} at $\mu_{seed} = 1$ nm and $\mu_{seed} = 3$ nm, where the G_{on} increases or stays nearly constant with increasing pitch (Figure 6 b,c). This may be explained by the fact that although the number of parallel conduction pathways increase at smaller pitches, for $\mu_{seed} = 1$ or 3 nm, the conductance of the individual nanoribbon segments is also small because the nanoribbon width upon termination of the growth is still very narrow when P is small (and $G_{on}^{segment}$ scales with w/L). Interestingly, when plotted differently, these data also reveal that substantial polydispersity in nanoseed sizes (σ_{seed}) do not have a significantly adverse effect on G_{on}^{mesh} and $G_{on}^{mesh}/G_{off}^{mesh}$. Specifically, SI Figure 4 shows that for $\mu_{seed} > 3$ nm, both G_{on} and G_{on}/G_{off} remain largely invariant of σ_{seed} at a given P. We also investigate the channel length dependence on G_{on}^{mesh} and $G_{on}^{mesh}/G_{off}^{mesh}$ and show that while G_{on}^{mesh} decays inversely with channel length, $G_{on}^{mesh}/G_{off}^{mesh}$ remains largely invariant (SI Figure 5).

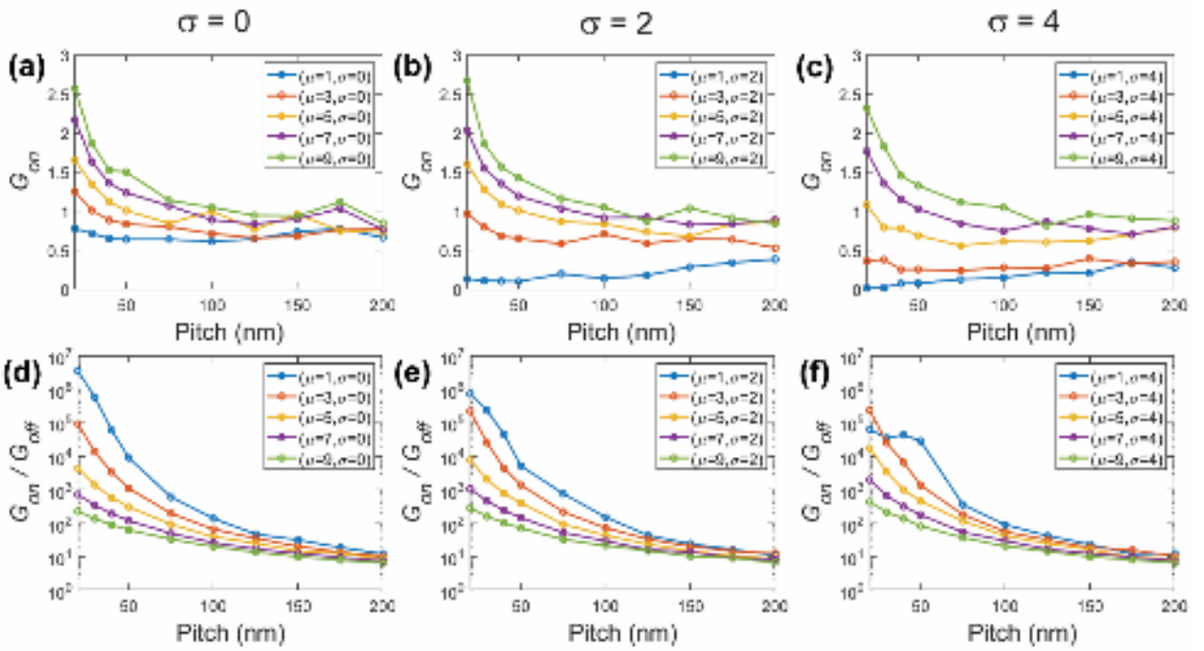


Figure 6: Plots of on-state conductance (G_{on}) and on-off ratio (G_{on}/G_{off}) at 1 nm ≤ μ_{seed} ≤ 9 nm at a fixed σ_{seed} = 0, 2, and 4 nm for (a,d), (b,e), and (c,f) respectively. G_{on} quantified with respect to the normalized sheet conductance of a single nanoribbon in the on-state.

Variables affecting the yield of an interconnected nanomesh

While factors governing the electrical performance of the nanomesh have been evaluated, yield is a crucial aspect that needs to be investigated. For instance, if polydispersity in the nanoseed size (σ_{seed}/μ_{seed}) is too large then a significant fraction of starting nanoseeds might be missing (because of overetching during annealing) leading to a disconnected nanomesh (Figure 7b,c). Other parameters that may influence a continuous path through a nanomesh are P and channel length. To this end, in Figure 7d and SI Figure 6 we plot calculate nanomesh yield *versus* σ_{seed}, P, and L_{ch}. For these plots, the nanomesh yield, Y, is calculated as $Y = c / T$ where c is the number of trials in

which a random simulation yields a continuous nanomesh (*i.e.* there is at least one continuous path for charge transport) and T is the total number of random trials performed.

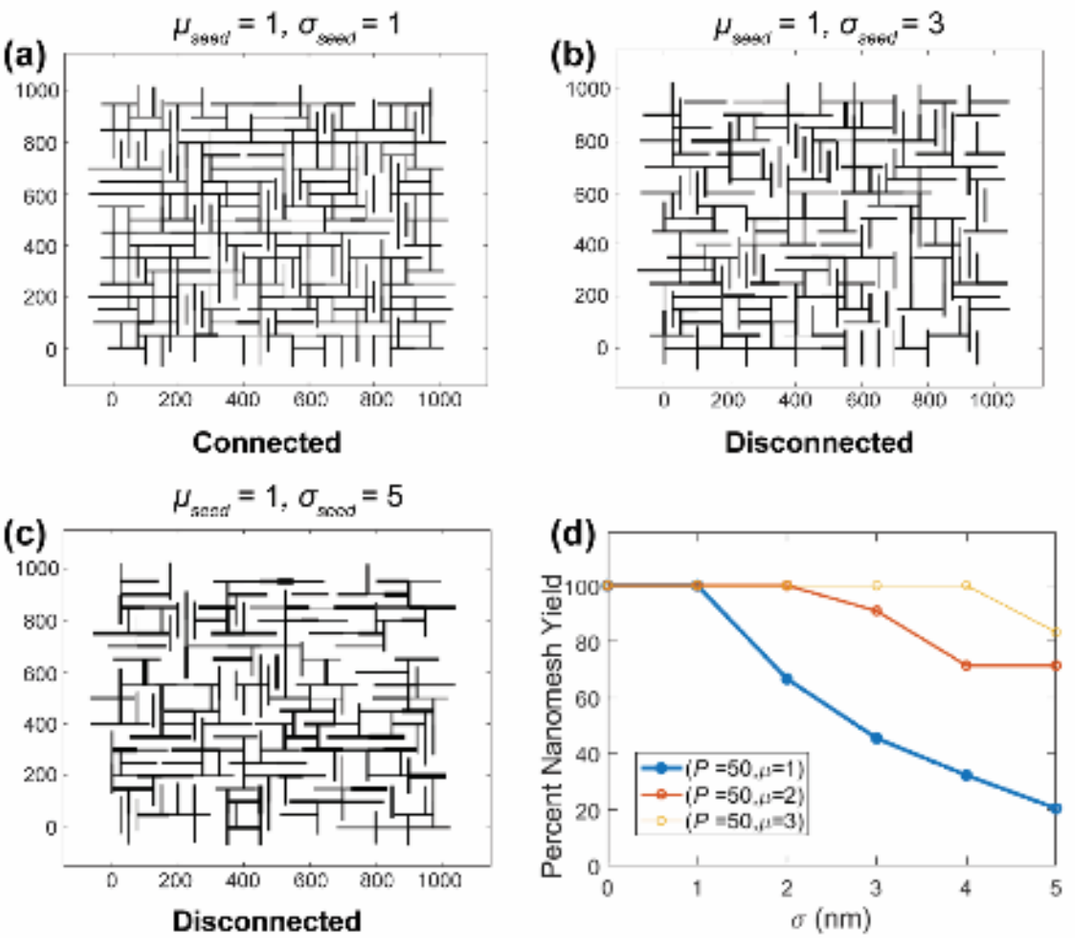
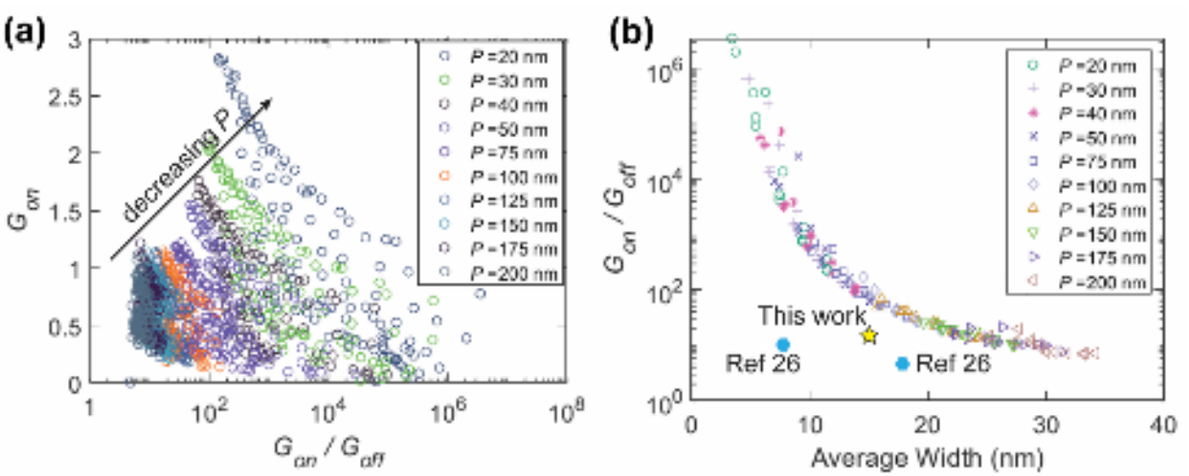


Figure 7: Deteriorating effect of nanoseed polydispersity on nanomesh yield. (a-c) Depiction of three representative nanomeshes where, μ_{seed} = 1 nm, P = 50 nm, L_{ch} =1000 nm, and t_{growth} = 3.75 h and σ_{seed} = 1, 3, and 5 nm for (a), (b), and (c), respectively. Only (a) leads to a connected nanomesh, while (b) and (c) lead to disconnected nanomeshes. (d) Quantitative summary of percent nanomesh yield as a function of nanoseed polydispersity for different seed sizes and fixed P = 50 nm. 10 random meshes are simulated at each condition.

329 In Figure 7d, Y is plotted against σ_{seed} at a fixed P = 50 nm and L_{ch} = 1000 nm and different μ_{seed}.
330 These data indicate that larger σ_{seed}/μ_{seed} is deleterious to yield and therefore, future nanomesh
331 designs likely need to consider relative polydispersity in starting seed-sizes. Similar analyses done
332 in SI Figure 6a,b indicate that Y deteriorates with increasing P and L_{ch} when σ_{seed}/μ_{seed} is large.
333 Although σ_{seed}/μ_{seed} can be reduced by increasing the μ_{seed}, larger μ_{seed} also leads to wider
334 nanoribbon segments and thus poorer G_{on}/G_{off} (see Figure d-f). Therefore a better way to reduce
335 σ_{seed}/μ_{seed} is to reduce σ_{seed} by using lithography techniques with higher resolution or by utilizing
336 organic molecules (e.g. pentacene, PTCDA, C_{60} etc.) as nanoseeds because of their
337 monodispersity. For comparison, we also simulated nanomesh growth initiated by organic
338 molecules deposited randomly, similar to that demonstrated in a previous report.[26]. These data are
339 shown in SI Figure 7.
340



341

342 **Figure 8:** (a) Cumulative plot of on-state conductance (G_{on}) versus on-off conductance
343 modulation (G_{on}/G_{off}) for all possible combinations of μ_{seed} and σ_{seed} at different pitches (P). G_{on}
344 quantified with respect to the normalized sheet conductance of a single nanoribbon in the on-
345 state. (b) Cumulative plot of G_{on}/G_{off} *versus* final average nanoribbon width in the nanomesh for

different pitches. L_{ch} is held constant at 1000 nm. Experimental data from our nanomesh device and ref 26 is indicated for comparison.

Discussion

We analyze the aggregated simulation data at all possible combinations of P, μ_{seed}, and σ_{seed} in Figure 8 (note that L_{ch} = 1000 nm for all the data shown in this plot). Figure 8a highlights an inevitable trade-off between G_{on} and G_{on}/G_{off} – both cannot be maximized simultaneously at a fixed P. This compromise is understood by considering that higher G_{on}/G_{off} is only observed in nanomeshes comprised of narrow nanoribbons (*i.e.,* small μ_{seed}), whereas high G_{on} is only observed in nanomeshes comprised of wide nanoribbons (*i.e.,* large μ_{seed}). Figure 8a shows however that the trade-off between G_{on} and G_{on}/G_{off} can be ameliorated by minimizing P. The dataset corresponding to larger P is confined to the bottom left region of the graph, which is always undesirable since both G_{on} and G_{on}/G_{off} are minimized. In contrast, as P decreases, the data move toward the more desirable upper-right corner of Figure 8a in which both G_{on}^{mesh} and $G_{on}^{mesh}/G_{off}^{mesh}$ increase. For a given G_{on}, a higher G_{on}/G_{off} is always observed with decreasing P. Thus, the importance of achieving smaller P is clearly visible from these data. Consequently, depending on the desired application (*e.g.,* high-performance versus low-power), an appropriate P and μ_{seed} will need to be selected.

Similar insight can be derived from Figure 8b wherein $G_{on}^{mesh}/G_{off}^{mesh}$ is plotted against average nanoribbon width in the nanomeshes at different P. These data clearly show how the $G_{on}^{mesh}/G_{off}^{mesh}$ is dictated by $G_{on}^{segment}$ / $G_{off}^{segment}$ and thus the width of each segment.

We compare our experimental results from Figure 4 to our simulations in Figures 6f and 8b. For the nanomesh characterized in Figure 5, the average nanoribbon width is ~ 15 nm, which should

exhibit $G_{on}^{mesh}/G_{off}^{mesh}$ of ~20 – 30. Our experimentally observed $G_{on}^{mesh}/G_{off}^{mesh}$ of 13 is on the same order of magnitude but somewhat smaller than what would be theoretically expected. This discrepancy, could be explained by several factors including a failure to fully turn-on the nanoribbon segments because of relatively thick gate-oxide or a poor description of the $G_{on}^{segment}$ / $G_{off}^{segment}$ ratio by $\exp\left(\frac{\alpha}{2wkT}\right)\frac{w}{L}$ for w > 10 nm, among other possibilities. Similar discrepancies between simulated and experimental G_{on}/G_{off} for nanomeshes have been observed previously,[26] indicating that there might be several unanswered questions with regards to the bandgap (and therefore, G_{on}/G_{off}) of super-10 nm wide nanoribbons.

Regardless, the broader conclusions from our simulations are still applicable for the design and synthesis of high-performance nanomeshes. As evident from Figure 8, it is critical to reduce the nanoseed pitch (P) to < 50 nm and nanoseed size (μ_{seed}) to < 5 nm in order to obtain a nanomesh with an appreciable G_{on}/G_{off} relevant for most semiconductor applications. While, in this study we are limited by the resolution of our electron-beam tool, recent advances in lithography for instance *via* using negative-tone resists such as HSQ or SU-8 or using multi-layer resists have made it possible to achieve much tighter pitches. Alternatively, block copolymer lithography can be used to fabricate wafer scale arrays of relatively monodisperse nanoseeds at sub-50 nm pitches.[42–44] These simulations provide ample motivation toward exploration of these techniques for fabrication of nanomeshes with improved charge transport properties. Additionally, in order to isolate the properties of the meshes from those of the Ge, we opted to transfer the nanomeshes onto SiO_2/Si substrates for our electrical measurements. However, it may be possible to create graphene nanomesh devices directly on Ge in the future if a stable oxide or insulator can be grown between the mesh and the Ge after the nanomesh synthesis.[45] In addition, hybrid graphene nanomesh-Ge

devices are also a promising option to explore in order to fully realize the potential of these nanomeshes.

Conclusion

To conclude, we demonstrate the bottom-up synthesis of graphene nanomeshes on technologically relevant Ge(001) with the potential to be adapted to a Si(001) platform.[6] We exploit the phenomena of anisotropic CVD and rotational self-alignment of graphene nanoseeds on Ge(001) to achieve a nearly even split of armchair nanoribbon directions oriented along the two perpendicular Ge⟨110⟩ directions. We fabricate ordered arrays of graphene nanoseeds on Ge(001) with different sizes and pitches using electron-beam lithography. Upon initiating CVD growth from these nanoseeds, the resulting nanoribbons grow orthogonally, fusing into each other, and forming an interconnected nanomesh spanning large areas with the potential to be scaled to any area across which seeds can be lithographically fabricated (*e.g.*, 300 mm wafer scales or larger). We characterize the charge transport properties of these nanomeshes and demonstrate an on/off ratio ~ 13 and field effect mobility ~ 0.7 $cm^2\ V^{-1}\ s^{-1}$, which is competitive with other long channel nanoribbon mesh devices reported in the literature. Using simulations, we demonstrate that charge transport properties are tunable depending on nanoseed-size, -polydispersity, and -pitch and that there is an inevitable tradeoff between achieving high on/off ratios and high on-current. Generally, however, smaller pitches (<50 nm) and smaller nanoseeds with reduced polydispersity alleviate this trade-off and result in superior charge transport characteristics and high yielding nanomeshes. Future work will be aimed at utilizing improved lithographic techniques to further enhance the electrical characteristics of these nanomeshes.

Supplementary Material

Please refer to the supplementary material for SEM images displaying nanomeshes with different degrees of nanoseed rotation, additional device electrical data related to nanomeshes, and further simulation analyses.

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Acknowledgements

Nanomesh CVD conception, synthesis, device measurements, and simulations (M.S.A, V.S., and A.J.W) and nanomesh transfer and device fabrication (X.Z. and R.M.J.) were supported by U.S. Department of Energy, Office of Science, Basic Energy Sciences, under award no. DE-SC0016007. This research used Materials Synthesis and Characterization, and Nanofabrication Facilities of the Center for Functional Nanomaterials (CFN), which is a U.S. Department of Energy Office of Science User Facility, at Brookhaven National Laboratory under Contract No. DE-SC0012704. S.M and J.K.K. aided with the deposition of Ni nanoseeds, supported by the National Science Foundation award number DMR-1752797 (JKK). J.H.D. and P.G. performed nanomesh transfer using PMMA/GMA supported by the U.S. Defense Advanced Research Projects Agency (DARPA) Grant No. D18AP00043. The authors gratefully acknowledge use of facilities and instrumentation supported by NSF through the University of Wisconsin Materials Research Science and Engineering Center (DMR-1121288, 0079983, and 0520057) and through the University of Wisconsin Nanoscale Science and Engineering Center (DMR-0832760 and 0425880).

References

[1] R.M. Jacobberger, B. Kiraly, M. Fortin-Deschenes, P.L. Levesque, K.M. McElhinny, G.J. Brady, R. Rojas Delgado, S. Singha Roy, A. Mannix, M.G. Lagally, P.G. Evans, P. Desjardins, R. Martel, M.C. Hersam, N.P. Guisinger, and M.S. Arnold, Nat Commun **6**, 8006 (2015).

[2] M. Lukosius, J. Dabrowski, J. Kitzmann, O. Fursenko, F. Akhtar, M. Lisker, G. Lippert, S. Schulze, Y. Yamamoto, M.A. Schubert, H.M. Krause, A. Wolff, A. Mai, T. Schroeder, and G. Lupina, ACS Appl Mater Interfaces **8**, 33786 (2016).

[3] B. Kiraly, A.J. Mannix, R.M. Jacobberger, B.L. Fisher, M.S. Arnold, M.C. Hersam, and N.P. Guisinger, Appl Phys Lett **108**, 213101 (2016).

[4] R.M. Jacobberger and M.S. Arnold, ACS Nano **11**, 9 (2017).

[5] R.M. Jacobberger, E.A. Murray, M. Fortin-Deschênes, F. Göltl, W.A. Behn, Z.J. Krebs, P.L. Levesque, D.E. Savage, C. Smoot, M.G. Lagally, P. Desjardins, R. Martel, V. Brar, O. Moutanabbir, M. Mavrikakis, and M.S. Arnold, Nanoscale **11**, 11 (2019).

[6] V. Saraswat, Y. Yamamoto, H.J. Kim, R.M. Jacobberger, K.R. Jinkins, A.J. Way, N.P. Guisinger, and M.S. Arnold, Journal of Physical Chemistry C **123**, 30 (2019).

[7] V. Saraswat, R.M. Jacobberger, and M.S. Arnold, ACS Nano **15**, 3 (2021).

[8] A.J. Way, R.M. Jacobberger, and M.S. Arnold, Nano Lett **18**, 2 (2018).

[9] A.J. Way, E.A. Murray, F. Göltl, V. Saraswat, R.M. Jacobberger, M. Mavrikakis, and M.S. Arnold, Journal of Physical Chemistry Letters **10**, 15 (2019).

[10] A.J. Way, V. Saraswat, R.M. Jacobberger, and M.S. Arnold, APL Mater **8**, 091104 (2020).

[11] F. Göltl, E.A. Murray, B.W.J. Chen, R.M. Jacobberger, M.S. Arnold, and M. Mavrikakis, Appl Surf Sci **527**, 146784 (2020).

[12] A.D. Franklin, Science **349**, 6249 (2015)

[13] N. Richter, Z. Chen, A. Tries, T. Prechtl, A. Narita, K. Müllen, K. Asadi, M. Bonn, and M. Kläui, Sci Rep **10**, 1988 (2020).

[14] Z. Chen, W. Zhang, C.A. Palma, A. Lodi Rizzini, B. Liu, A. Abbas, N. Richter, L. Martini, X.Y. Wang, N. Cavani, H. Lu, N. Mishra, C. Coletti, R. Berger, F. Klappenberger, M. Kläui, A. Candini, M. Affronte, C. Zhou, V. de Renzi, U. del Pennino, J. v. Barth, H.J. Räder, A. Narita, X. Feng, and K. Müllen, J Am Chem Soc **138**, 47 (2016).

[15] Y. Huang, Y. Mai, U. Beser, J. Teyssandier, G. Velpula, H. van Gorp, L.A. Straasø, M.R. Hansen, D. Rizzo, C. Casiraghi, R. Yang, G. Zhang, D. Wu, F. Zhang, D. Yan, S. de Feyter, K. Müllen, and X. Feng, J Am Chem Soc **138**, 32 (2016).

[16] M. Shekhirev, T.H. Vo, M.M. Pour, A. Sinitskii, S. Munukutla, and J.W. Lyding, ACS Appl Mater Interfaces **9**, 1 (2017).

[17] Z. Geng, H. Bernd, R. Granzner, M. Auge, A.A. Lebedev, V.Y. Davydov, and M. Kittler, Annalen der Physik **529**, 11 (2017).

[18] J. Bai, X. Zhong, S. Jiang, Y. Huang, and X. Duan, Nat Nanotechnol **5**, (2010).

[19] Y. Lin, Y. Liao, Z. Chen, and J.W. Connell, Mater Res Lett **5**, 4 (2017).

[20] M. Wang, L. Fu, L. Gan, C. Zhang, M. Rümmeli, A. Bachmatiuk, K. Huang, Y. Fang, and Z. Liu, Sci Rep **3**, 1238 (2013).

[21] J. Yang, M. Ma, L. Li, Y. Zhang, W. Huang, and X. Dong, Nanoscale **6**, 22 (2014).

[22] M. Kim, N.S. Safron, E. Han, M.S. Arnold, and P. Gopalan, Nano Lett **10**, 4 (2010).

[23] C. Moreno, M. Vilas-Varela, B. Kretz, A. Garcia-Lekue, M. v. Costache, M. Paradinas, M. Panighel, G. Ceballos, S.O. Valenzuela, D. Peña, and A. Mugarza, Science **360**, 6385 (2018).

[24] Z. Mutlu, P.H. Jacobse, R.D. McCurdy, J.P. Llinas, Y. Lin, G.C. Veber, F.R. Fischer, M.F. Crommie, and J. Bokor, Adv Funct Mater **31**, 47 (2021).

[25] N.S. Safron, M. Kim, P. Gopalan, and M.S. Arnold, Advanced Materials **24**, 1041 (2012).

[26] N. Kim, S. Choi, S.J. Yang, J. Park, J.H. Park, N.N. Nguyen, K. Park, S. Ryu, K. Cho, and C.J. Kim, ACS Appl Mater Interfaces **13**, 24 (2021).

[27] T. Fang, A. Konar, H. Xing, and D. Jena, Phys Rev B Condens Matter Mater Phys **78**, 205403 (2008).

[28] D. Basu, M.J. Gilbert, L.F. Register, S.K. Banerjee, and A.H. MacDonald, Appl Phys Lett **92**, 042114 (2008).

[29] R.M. Jacobberger, A.J. Way, V. Saraswat, and M.S. Arnold, ECS Trans **93**, 129 (2019).

[30] A.J. Way, E. Murray, R.M. Jacobberger, V. Saraswat, F. Goeltl, M. Mavrikakis, and M.S. Arnold, ECS Trans **93**, 121 (2019).

[31] A.J. Way, R.M. Jacobberger, N.P. Guisinger, V. Saraswat, X. Zheng, A. Suresh, J.H. Dwyer, P. Gopalan, and M.S. Arnold, Nat Commun **13**, 2992 (2022).

[32] A.M. Scaparro, V. Miseikis, C. Coletti, A. Notargiacomo, M. Pea, M. de Seta, and L. di Gaspare **8**, 48 (2016).

[33] D. Akinwande, N. Petrone, and J. Hone, Nat Commun **5**, 5678 (2014).

[34] J.H. Lee, E.K. Lee, W.J. Joo, Y. Jang, B.S. Kim, J.Y. Lim, S.H. Choi, S.J. Ahn, J.R. Ahn, M.H. Park, C.W. Yang, B.L. Choi, S.W. Hwang, and D. Whang, Science **344**, 6181 (2014).

[35] H.W. Kim, W. Ko, W.J. Joo, Y. Cho, Y. Oh, J. Ku, I. Jeon, S. Park, and S.W. Hwang, Journal of Physical Chemistry Letters **9**, 24 (2018).

[36] B. Kiraly, R.M. Jacobberger, A.J. Mannix, G.P. Campbell, M.J. Bedzyk, M.S. Arnold, M.C. Hersam, and N.P. Guisinger, Nano Lett **15**, 11 (2015).

[37] D.S. Schulman, A.J. Arnold, and S. Das, Chem Soc Rev **47**, 9 (2018).

[38] G. Wang, M. Zhang, Y. Zhu, G. Ding, D. Jiang, Q. Guo, S. Liu, X. Xie, P.K. Chu, Z. Di, and X. Wang, Sci Rep **3**, 2465 (2013).

[39] L. Persichetti, M. de Seta, A.M. Scaparro, V. Miseikis, A. Notargiacomo, A. Ruocco, A. Sgarlata, M. Fanfoni, F. Fabbri, C. Coletti, and L. di Gaspare, Appl Surf Sci **499**, 143923 (2020).

[40] V. Passi, A. Gahoi, B. V. Senkovskiy, D. Haberer, F.R. Fischer, A. Grüneis, and M.C. Lemme, ACS Appl Mater Interfaces **10**, 12 (2018).

[41] X. Li, X. Wang, L. Zhang, S. Lee, H. Dai, **319**, 5867 (2008).

[42] G.G. Yang, H.J. Choi, K.H. Han, J.H. Kim, C.W. Lee, E.I. Jung, H.M. Jin, and S.O. Kim, ACS Appl Mater Interfaces **14**, 10 (2022).

[43] S.M. Lewis, M.S. Hunt, G.A. Derose, H.R. Alty, J. Li, A. Wertheim, L. de Rose, G.A. Timco, A. Scherer, S.G. Yeates, and R.E.P. Winpenny, Nano Lett **19**, 9 (2019).

[44] A.E. Grigorescu and C.W. Hagen, Nanotechnology **20**, 292001 (2009)

[45] P. Braeuninger-Weimer, O. Burton, R.S. Weatherup, R. Wang, P. Dudin, B. Brennan, A.J. Pollard, B.C. Bayer, V.P. Veigang-Radulescu, J.C. Meyer, B.J. Murdoch, P.J. Cumpson, and S. Hofmann, APL Mater **7**, 071107 (2019).