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Research Article

Integrated Papertronic Techniques: Highly Customizable Resistor, Supercapacitor, and Transistor Circuitry on a Single Sheet of Paper

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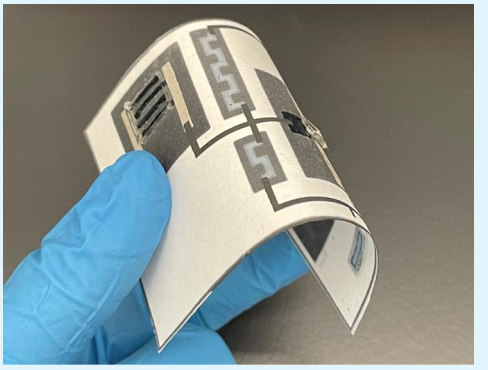
ABSTRACT: Humanity's excessive production of material waste poses a critical environmental threat, and the problem is only escalating, especially in the past few decades with the rapid development of powerful electronic tools and persistent consumer desire to upgrade to the newest available technology. The poor disposability of electronics is especially an issue for the newly arising field of single-use devices and sensors, which are often used to evaluate human health and monitor environmental conditions, and for other novel applications. Though impressive in terms of function and convenience, usage of conventional electronic components in these applications would inflict an immense surge in waste and result in higher costs. This work's primary objective is to develop a cost-effective, eco-friendly, all-paper, device for single-use applications that can be easily and safely disposed of through incineration or biodegradation. All electronic components are paper-based and integrated on paper-based printed circuit boards (PCBs), innovatively providing a realistic and practical solution for green electronic platforms. In particular, a methodology is discussed for simultaneously achieving very tunable resistors (20 Ω to 285 kΩ), supercapacitors (~3.29 mF), and electrolyte-gated field-effect transistors on and within the thickness of a single sheet of paper. Each electronic component is completely integrated into functionalized paper regions and exhibits favorable electrical activity, adjustability, flexibility, and disposability. A simple amplifier circuit is successfully demonstrated within a small area and within the thickness of a single sheet of paper, displaying component versatility and the capability for their fabrication processes to be performed in parallel for efficient and rapid development.



KEYWORDS: *papertronic, tunable, disposable, resistor, supercapacitor, transistor*

1. INTRODUCTION

In recent decades, paper-based electronic circuits have gained increasing attention as a promising alternative to conventional circuit materials.[1] Currently, the standard for printed circuit board (PCB) substrate materials are centered around glass fiber, resin, and copper composites, which are rigid and bulky and require relatively intensive manufacturing processes.[2] These exhaustible materials are especially unsuitable for and misallocated to single-use, disposable electronic devices, including but not limited to those in the fields of point-of-care diagnostics, environmental biomonitoring, and wearables.[3] Replacing conventional electronic materials with cellulose paper substrates has numerous advantages. Not only would the transition make significant strides from an economic and environmental standpoint as plant-derived cellulose paper products present an affordable, abundant, renewable, and biodegradable resource, but it also offers attractive physical qualities for its functional use in electronics.[1,4,5] Paper substrates have unparalleled flexibility, conformability to uneven surfaces, biocompatibility, passive capillary transportation of liquids, and large surface areas for their thicknesses. However, paper substrates are deemed by many to be unfit for electronic applications owing to their rough surface topology and unpredictable fiber networks, which may lead to poor adherence of metallic components, uneven dispersion of coatings, and ultimately excessive defects within sensitive devices.[6]

Despite the obstacles associated with the integration of paper with electronics, some research groups, including our own,[7,8] have persevered to find ways to successfully incorporate paper substrates in circuit applications, though at arguably low-level integration. One approach centers around the concept of employing paper materials merely for supportive purposes in which off-shelf surface-mountable circuit components are adhered to the paper's surface and interconnected via metallic patterning.[9−11] Though this technique may nullify the need for a conventional PCB substrate, moderately reducing environmental effects and improving device affordability, it falls short as

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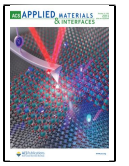

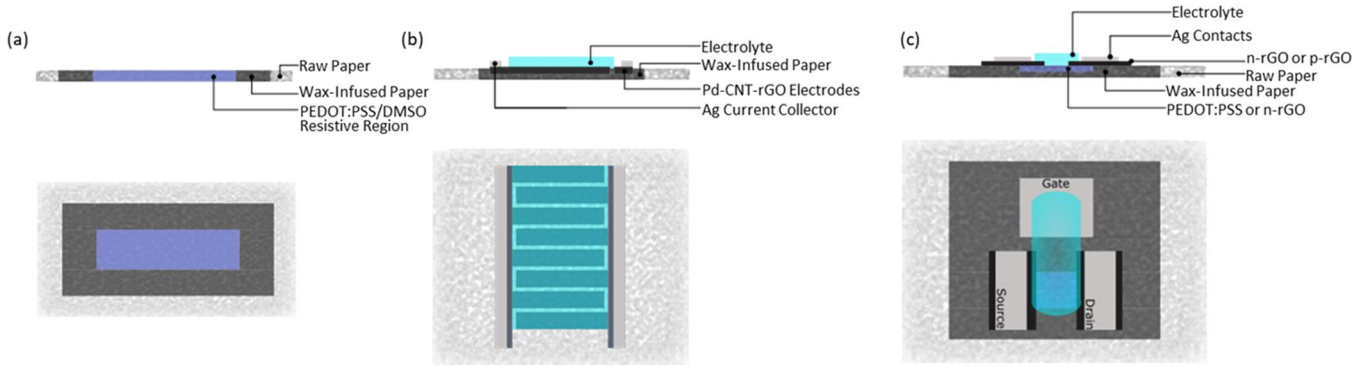

Figure 1. Modeled depictions of the top view and cross-sectional view of (a) paper resistors, (b) paper supercapacitors, and (c) paper transistors.

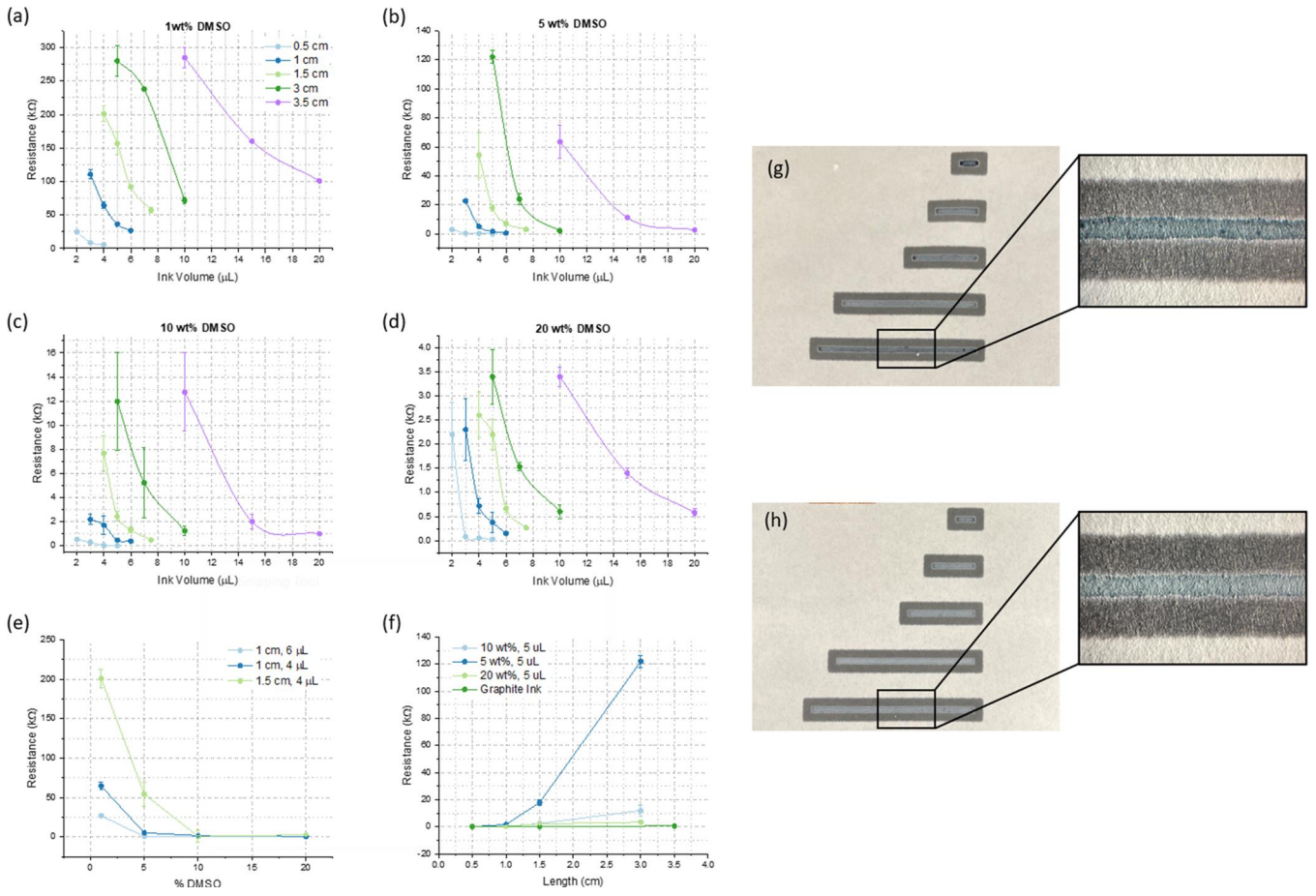

Figure 2. Measured resistance of paper resistors at lengths between 0.5 and 3.5 cm and with controlled ink volumes when the DMSO ink concentration is (a) 1 wt %, (b) 5 wt %, (c) 10 wt %, and (d) 20 wt %. Plots showing the isolated effect of (e) wt % DMSO and (f) resistor length on the resulting resistance. Photographed images of fabricated resistors at (g) maximum applied ink volumes and (h) minimum applied ink volumes for each resistor length.

an effective "paper PCB" solution on several important fronts. Primarily, off-shelf components and metal traces considerably limit the disposability and the flexibility of the device—two of the main attractions of using paper in the first place. Though perhaps, less obviously, this technique simply does not recognize any of the other aforementioned unique and potentially valuable characteristics of paper, missing an opportunity to take full advantage of its material properties.

As a step in the right direction in terms of the increased degree of integration, other researchers have investigated means of developing circuit components directly on paper. This approach is characterized by dissection, design, and from-scratch assembly of commonly used components onto the surface of the paper substrate. Most often, resistors, capacitors, and transistors are targeted as the components of interest as they are commonly deemed the most essential components with the best feasibility for paper integration. However, the most common way these components are installed involves simple adhesion or application of prepared metallic materials to the paper surface, such as aluminum foil or copper tape, or using a graphite pencil to create resistive and capacitive structures.[12,13] Other cases seek to resolve the issue of paper surface roughness by selecting an

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application-specific, commercially made paper pretreated with nonporous priming agents (p_e:smart) or by performing similar "at-home" versions of the treatment on paper.[14,15] Functional semiconductive and metallic materials can be more uniformly applied to the paper, mitigating some of the performance-reducing defects associated with paper substrates. Though they potentially improve the performance parameters for the resultant components, those methods yield a product that feels distinctly non-paper and face many of the same concerns as those discussed with the existing paper PCB techniques; simply applying a pre-prepared metal and using specialty coated paper reduce affordability and disposability. Some groups developed more meaningful approaches for individual components, but the methods can be very highly specific and intensive, and some lack full active use of the paper substrate.[16,17] No one has been able to sufficiently define a means by which to batch-fabricate multicomponent designs while maintaining circuit flexibility easily and cheaply.

In this work, relatively simple fabrication equipment and techniques are used to create and characterize fully functioning, tunable resistors, supercapacitors (SCs), and electrolyte-gated transistors (EFETs) (Figure 1). The natural compatibility of paper with wicking, printing, and stacking can allow us to minimize the fabrication processes and device design complexity by exploiting all beneficial properties of paper in a cost-effective and eco-friendly way. Via wax-printing, paper ink injection, and screen printing, the components are able to maintain flexibility while attaining complete integration with the paper substrate. The paper is functionalized to establish conductive and semiconductive properties. The unprecedented range of parameters, tunability, and stability of the paper components allow for precise component specifications and accomplishment of a wide range of customizable paper circuits, contributing to enhanced practicality in the field of "papertronics." A simple amplifier circuit is demonstrated within a small area and within the thickness of a single sheet of paper, displaying component versatility and the capability for their fabrication processes to be performed in parallel for efficient and rapid development.

2. RESULTS AND DISCUSSION

2.1. Resistor Characterization. The paper-based resistors use a unique method of tunable ink deposition on 180 μm-thick filter paper.[18] Sheets were patterned with wax to create paper wells with wax boundaries extending through the depth of the paper substrate. These wells were filled with conductive ink based on a blend of organic conductive polymer poly(3,4-ethylenedioxythiophene) and polystyrenesulfonate (PEDOT:PSS).[19] Cellulose paper fibers are inherently electrically insulative, but through saturation with the conductive ink, the paper can be functionalized to act as a semiconductor and pass electric current.[1] This attains paper resistors through ink-injection techniques. Using that method, nominal resistance values can be sensitively controlled by three distinct variables: resistor dimensions, ink conductivity, and ink volume. Comparatively, a competing method of paper resistor fabrication in which a material trace is coated on the paper surface can only be adjusted via resistor dimensions, which inevitably increases the spatial footprint and reduces the versatility of resistor tuning.

Resistors are based on the important principle that the conductivity of the PEDOT:PSS can be manipulated through the controlled addition of a conductive additive called dimethyl sulfoxide (DMSO).[20,21] There is evidence that DMSO increases the conductivity of PEDOT:PSS by removing excess PSS.[20] Therefore, increasing the ratio of DMSO to PEDOT: PSS should result in proportionally better conductivity for the resulting ink mixture. To evaluate this claim, inks containing 1, 5, 10, and 20 wt % DMSO were injected into paper wells of varying lengths (0.5, 1, 1.5, 3, and 3.5 cm) at controlled volumes, and the consequent resistance values were measured (Figure 2a–d). Plot representations of the isolated influence of DMSO weight percentage and resistor length appear in Figure 2e,f, respectively.

The influence of the first variable, namely, resistor dimensions, has already been extensively studied, and the relationship to resistance is well established. Resistance should be proportional to resistor length and inversely proportional to the resistor width and thickness. In this study, the resistor thickness and width are kept constant, allowing for resistor dimensions to be adjusted only by resistor length. The width is 1 mm, and the thickness is determined by the inherent thickness of the paper substrate, that is, 180 μm. Paper resistor designs are measured at lengths of 0.5, 1, 1.5, 3, and 3.5 cm, and the appropriate proportional relationship between the resistance and resistor length is successfully reflected in the collected data (Figure 2f).

According to the collected data, the nominal resistance of the paper resistors was found to be correlated to ink conductivity as expected; as the ink recipe became more conductive by incrementally using a larger ratio of DMSO, resistance dropped. The improved conductivity of the ink reduces the nominal resistance as more conductive pathways are formed within the paper fibers. With more conductive paper pathways, the electric current can more easily pass through the paper, experiencing less resistance. Paper resistors of greater nominal resistance can therefore be achieved by reducing the weight percentage of DMSO. Similarly, an increased ink volume increased resistance. As more conductive ink is added to the paper wells, the insulative paper fibers become more saturated with ink and are layered with a thicker coating of conductive materials once dried, resulting in lower-resistance channels. The higher density of the conductive mixture responsible for the lowered resistance can be colorimetrically observed as a darker blue (Figure 2g).

Through the independent adjustment of each of these three variables, a collective resistance range of 20 Ω to 285 kΩ was attained for the designed paper resistors, allowing for paper resistor utilization in a variety of circuit applications. For comparison, the use of screen-printed graphite ink on the surface of the paper substrate was only able to attain a resistance range of 100 Ω to 3.4 kΩ when designed with a width of 1 mm and a length variation from 0.5 to 14 cm—a maximum length that is 4 times as long as PEDOT:PSS ink-based resistors (Figure S1). At a fraction of the areal footprint, the presented PEDOT:PSS resistors can attain a much larger maximum resistance value, making PEDOT:PSS a much more efficient choice as a resistive material, though graphite ink still has relevancy for applications requiring low-resistance traces. Additionally, this range represents the results of only the presented test cases, and even higher resistance values could likely be achieved by (1) narrowing or lengthening the resistor dimensions, (2) complete deficiency of DMSO in the ink recipe, or (3) further reduction of injected ink volumes.

2.2. Supercapacitor Characterization. The paper SCs use a similar method of ink injection to functionalize the fibers of the paper substrate, establishing conductive, porous paper electrodes. The electrode ink is based on a porous carbon nanotube-reduced graphene oxide (CNT-rGO) hydrogel covered with

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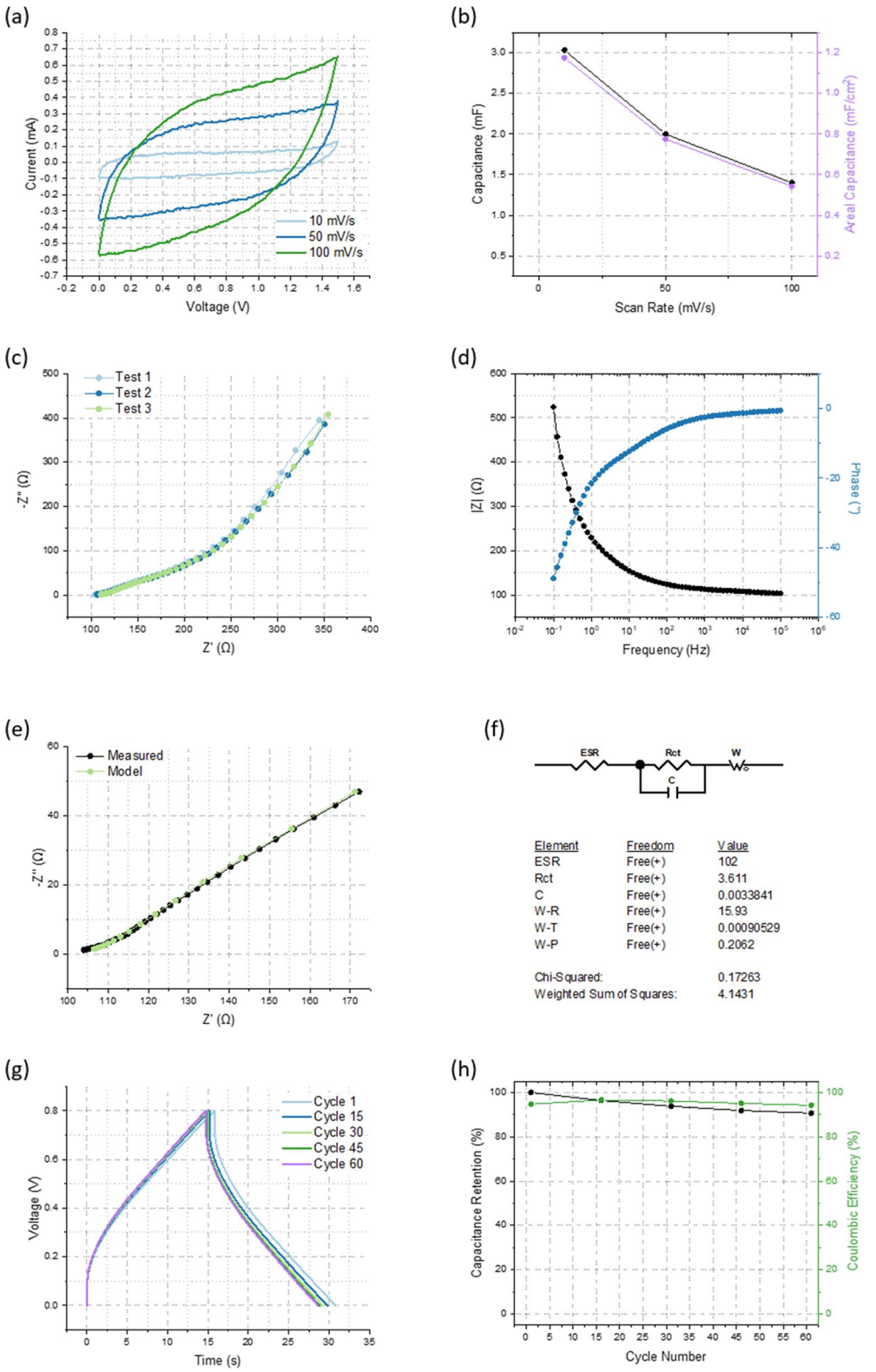

Figure 3. Characteristics for 8-fingered SC. (a) CV profiles for a voltage window of 0−1.5 V at scan rates of 10, 50, and 100 mV/s and (b) trend of capacitance values for each scan rate. EIS characterization displayed in (c) a Nyquist plot with three consecutive EIS test iterations and (d) a Bode plot. (e) EIS Nyquist plot of comparing measured data to fitted model data and (f) corresponding capacitor equivalent circuit model and fitted data estimations. (g) GCD curves at a constant current of 0.2 mA after different degrees of cycling and (h) the effect of cycling on capacitance retention and Coulombic efficiency.

palladium nanoparticles (Pd-NPs). The Pd-CNT-rGO nanocomposite is suspended in a PEDOT:PSS solution to create a soluble ink that can be absorbed by the paper fibers. The composite effectively combines rGO, CNT, and Pd to create a synergistic effect, producing a material with exceptional conductivity, rapid electron capture/transport capabilities,

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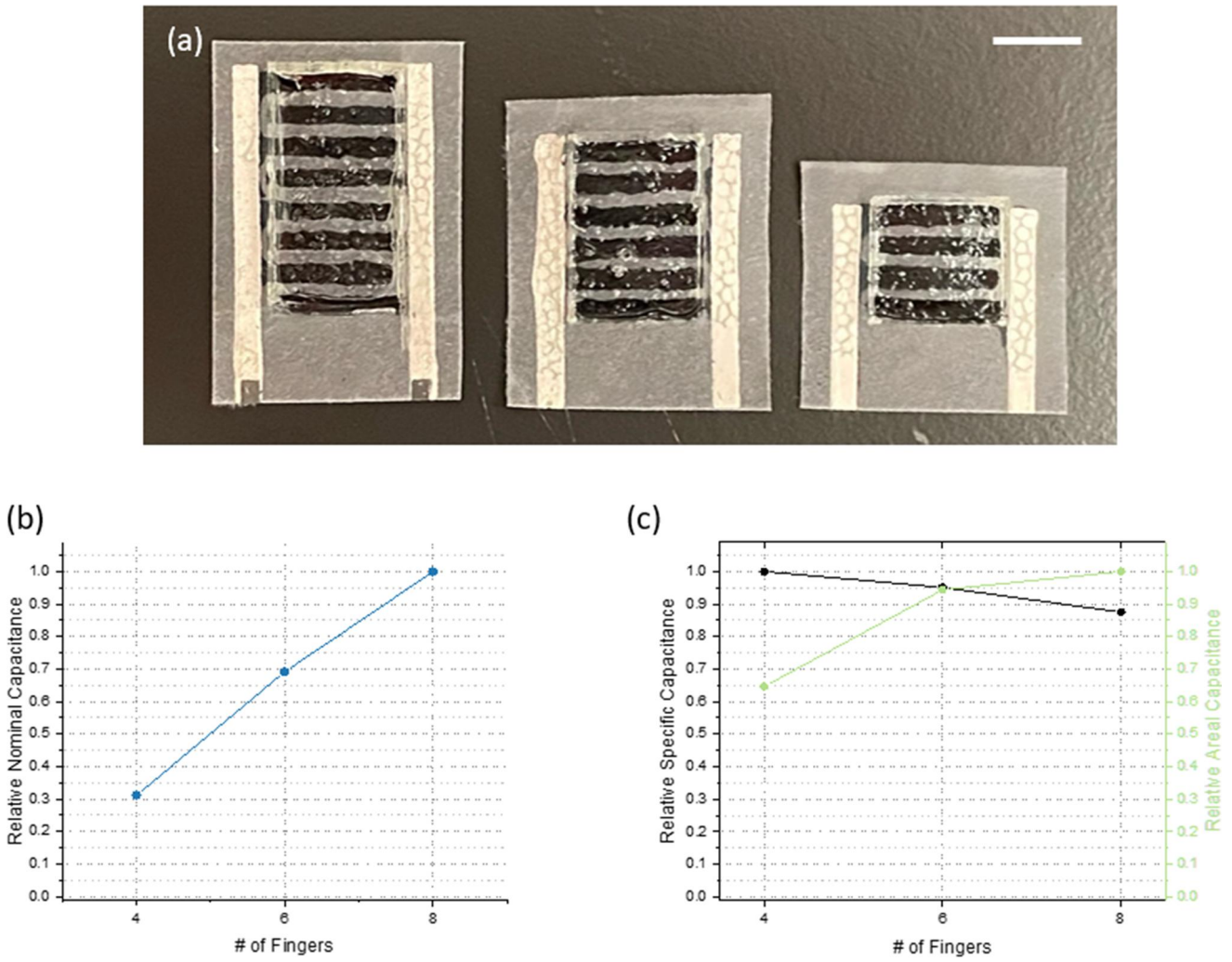

Figure 4. (a) Image of SC with 8, 6, and 4 interdigital fingers (scale bar = 10 mm). Plots showing the trends in the (b) relative nominal capacitance and (c) relative specific and areal capacitance for SC designs with different numbers of interdigital fingers.

stable catalytic activity, and a high surface area.[22−25] The rGO contributes its excellent conductivity, superior electron transport capabilities, and catalytic interactions, but graphene can face an issue of excessive aggregation and stacking interactions, limiting the surface area and reducing catalytic sites. The Pd nanoparticles, which are additionally quite conductive and catalytically active, prevent aggregation of graphene to maintain the material's high surface area. The CNTs reinforce the durability of the Pd catalyst, contribute to the prevention of excessive graphene aggregation, and further enhance electron transfer rates. Each material is meant to work in conjunction to achieve the desired characteristics for our capacitive electrode. These material properties combined with the highly porous paper network achieve conductive electrodes with a high surface area for improved capacitive characteristics. Capacitors are designed with a planar interdigitated structure featuring a semisolid electrolyte made from a polyvinyl alcohol/phosphoric acid (PVA/H_3PO_4) gel and a silver/silver chloride (Ag/AgCl) current collector. An eight-fingered version of the interdigital capacitor was assembled as described and evaluated with numerous methods to fully characterize the capacitive behavior.

First, cyclic voltage (CV) analysis was performed on the SC at scan rates of 10, 50, and 100 mV/s (Figure 3a). At the lower scan rates, the CV profile has a near-rectangular profile indicating excellent electric double layer (EDL) capacitive behavior with a low equivalent series resistance (ESR).[26] The capacitance value based on the CV profiles was calculated according to eq 1:

$$C_{CV} = \frac{\int I d\nu}{2 \times \nu \times \Delta V} \quad (1)$$

where $\int I d\nu$ is the area below the CV curve, ν is the scan rate, and ΔV is the voltage window. The nominal capacitance and areal capacitance at scan rates from 10 to 100 mV/s are calculated from the CV profiles (Figure 3b). Slight distortion and reduction in capacitance at faster scan rates likely stem from limitations on ion transport speeds.[27] The highest achieved capacitance values for the SC are attained at 10 mV/s, reaching 3.033 mF and 1.176 mF/cm^2 (Figure 3b and Table S1).

Electrochemical impedance spectroscopy is additionally performed on the SC to monitor the dynamic impedance profiles over the frequency range of 0.1 to 10,000 Hz. Nyquist plot and Bode plot representations are presented for a detailed view of the component's behavior (Figure 3c,d). The Nyquist plot representation displays a profile with a very low semicircle at high frequencies followed by an almost vertical trend toward lower frequencies, indicative of a supercapacitive device with fast electron transfer.[28] Additionally, the Nyquist Plot reveals a low series resistance value (seemingly close to 100 Ω), and

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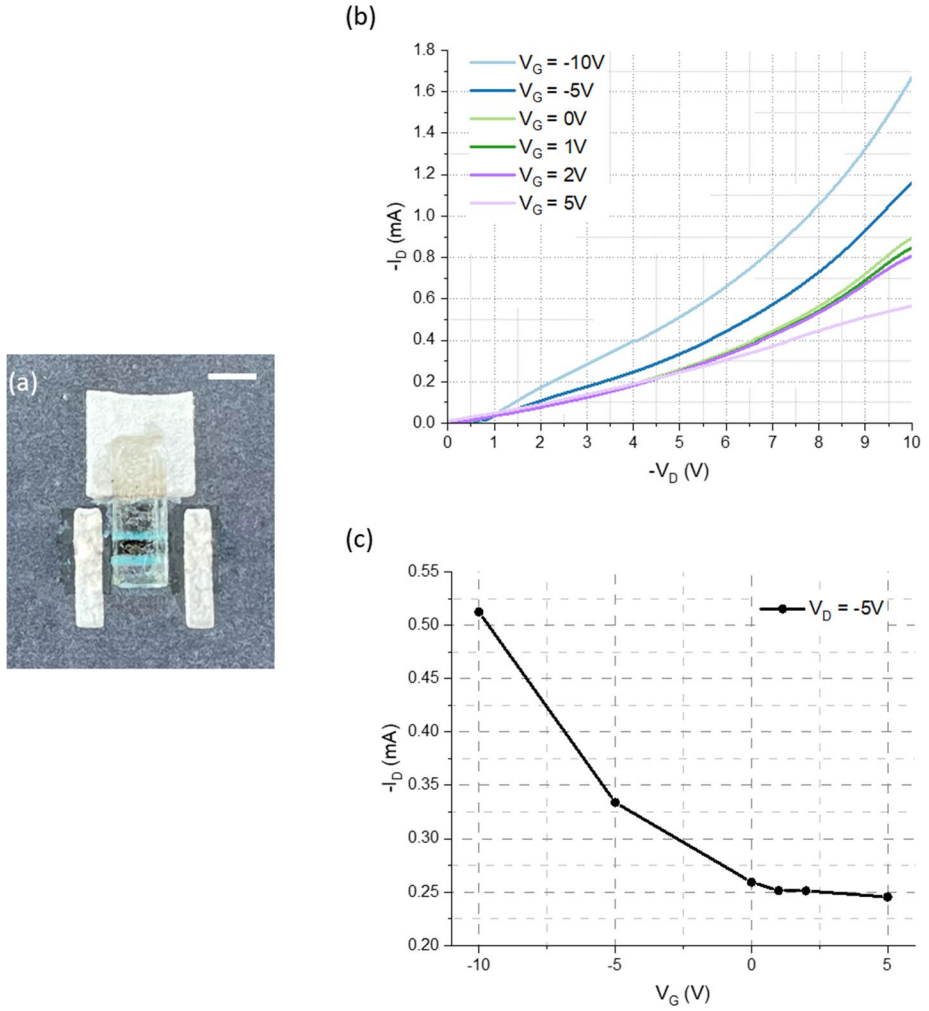

Figure 5. (a) Image of the fabricated p-type EFET (scale bar = 3 mm). (b) Output characteristic plot and (c) transfer characteristic plot of the n-type EFET.

consecutive EIS measurements result in almost identical profiles, suggesting reproducibility and stability of the SC. For a more thorough evaluation of the EIS data, an equivalent circuit model was fitted to the Nyquist profile from the initial measurement (Figure 3e). The model is a variation of a Randles circuit composed of the equivalent series resistance (ESR), system capacitance (C), charge transfer resistance (R_{ct}), and a series Warburg element (W) (Figure 3f). Based on the model fitting, the values of ESR, C, and R_{ct} were estimated to be 102 Ω, 3.38 mF, and 3.6 Ω, respectively.

Finally, galvanostatic charging/discharging (GCD) was performed at a constant current of 0.2 mA to further characterize the SC (Figure 3g). A mostly linear charge/discharge profile with some slight curvature indicates a major EDL capacitive contribution with likely some pseudocapacitive interactions.[26] The charge/discharge was repeated for 60 cycles for preliminary evaluation of cycling stability (Figure 3h). The profile of the first GCD cycle was used to calculate the capacitance via eq 2:

$$C_{GCD} = I_d \times \frac{(t_2 - t_1)}{(V_1 - V_2)}, \quad (2)$$

in which I_d is the discharge current, V_1 is 64% of the maximum voltage, V_2 is 32% of the maximum voltage, and t_1 and t_2 are the time it takes for the voltage to drop from the maximum to V_1 and V_2, respectively. Using this equation, the capacitance calculation for cycle 1 generated a value of approximately 3.61 mF. The capacitances of subsequent cycles (cycles 15, 30, 45, and 60) were similarly calculated and presented relative to the initial value, effectively displaying the capacitance retention of the SC. After 60 cycles, the capacitance retention remained above 90% and the Coulombic efficiency remained consistently greater than 94%, demonstrating fairly high cycling stability in relation to other paper-based capacitors.

Capacitor calculations using the abovementioned methods all produced similar capacitance values on the scale of 3 mF. The capacitance value was further measured via a digital multimeter, indicating a capacitance of 3.13 mF for the system, agreeing with the previously calculated values. The consensus of the four independent methods implies that the average of the four capacitance values could be an ideal expression of the actual capacitance value, and so the average was calculated and found to be approximately 3.29 mF (Table S2).

Because of the interdigitated configuration, the presented SC design can additionally be tuned via modification of the interdigital finger dimensions and number. The initial design consisted of eight fingers with a length of 12 mm, a width of 2.5 mm, and a gap distance of 0.5 mm. For preliminary comparison and proof-of-concept for the tunability of our designed paper SC, paper capacitors with six and four fingers were also prepared and measured via a digital multimeter (Figure 4a). For clarity,

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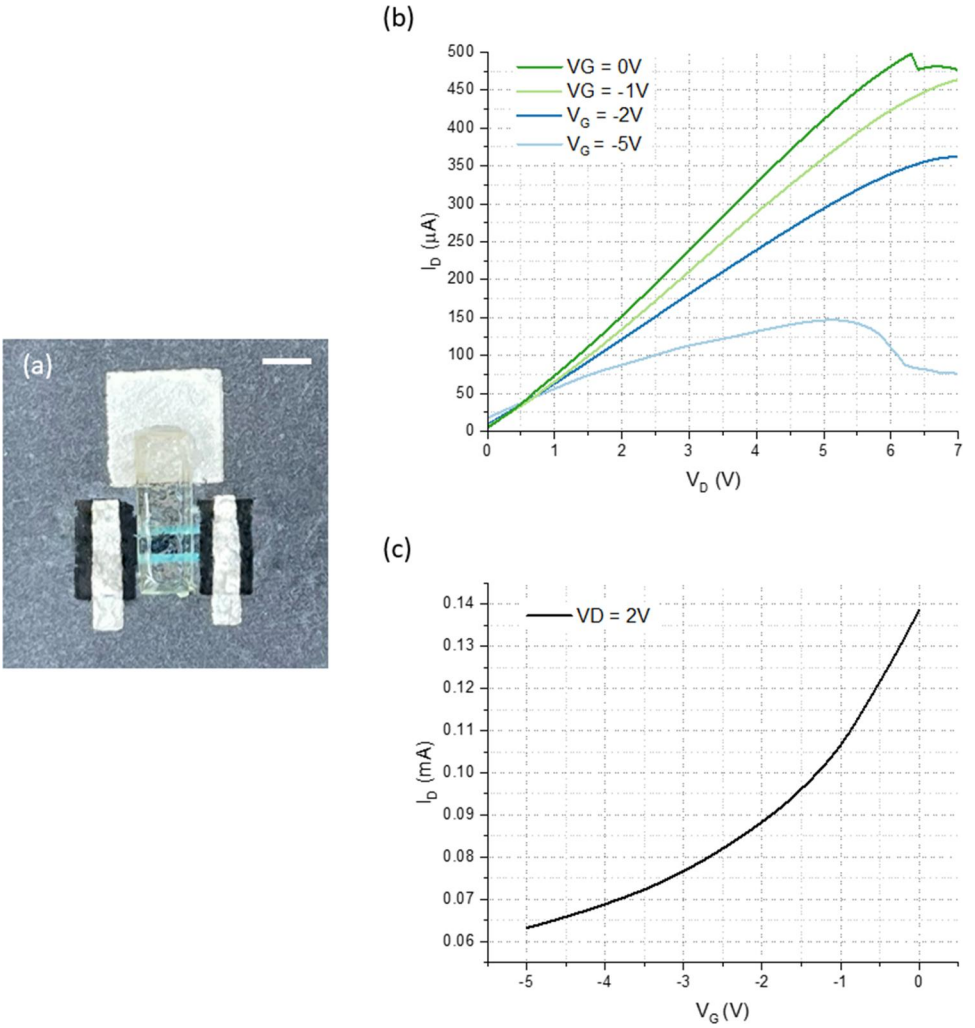

Figure 6. (a) Image of the fabricated n-type EFET (scale bar = 3 mm). (b) Output characteristic plot and (c) transfer characteristic plot of the n-type EFET.

the nominal capacitance, specific capacitance, and areal capacitance for each design are presented relatively with 1 representing the largest recorded value among the three designs (Figure 4b,c). The reduction in the number of fingers resulted in the linear decrement of the measured capacitance, while specific and areal capacitance remained relatively constant, indicating a much-desired consistency between the designs. Though not experimentally investigated in this study, increases in the finger length, width, and gap are correlated with increased capacitance, and so these design dimensions could be modified to achieve a wider capacitance range for use in a variety of custom paper circuit applications.[29]

2.3. Transistor Characterization. Paper-based lateral configuration EFETs are attained through sequential wax printing, ink injection, electrode screen printing, contact screen printing, and gel electrolyte casting. Both p-type and n-type depletion-mode transistors are designed through similar processes. The p-type EFET uses n-doped rGO as a substrate, and a p-doped rGO source and drain electrodes overlap with this n-type substrate to achieve a p-channel when in operation. Contrastingly, the n-type EFET is structured with a p-doped PEDOT:PSS-based substrate and n-doped rGO for the source and drain. Both designs incorporate Ag/AgCl for the gate electrode and the metal contacts and a PVA/ H_3PO_4 gel electrolyte between the gate and channel. The channel dimensions of the transistors are designed to be 4 mm in length and 2 mm in width with a gate-to-channel distance of 3 mm.

The fabricated output characteristics of the p-type EFET (Figure 5a and Figure S2) are obtained by applying defined gate voltages and measuring the drain current as the drain voltage is decreased from 0 V to higher negative voltages (Figure 5b and Figure S2). The transfer characteristic plot shows the relationship between the gate bias and the drain current at a constant drain potential of −2 V (Figure 5c and Figure S2). The output characteristic plot shows a p-type depletion-mode behavior as the transistor is effectively "on" and conducting negative drain current, even when there is no applied gate voltage.[30] The excessive conductivity of the n-doped rGO region between the source and drain allows conduction of electricity without a bias voltage. As the gate voltage is positively increased from 0 to 5 V incrementally, there is an observed decrease in the output characteristic slope and in the drain current, indicating that a higher gate voltage can begin turning the transistor "off." At the same time, applying more negative gate voltages can further increase the drain current beyond the unbiased state, allowing for the transistor "on" state to conduct current more effectively. This phenomenon is due to the influence of the gate voltage on the ions within the gel electrolyte, which will have an attractive

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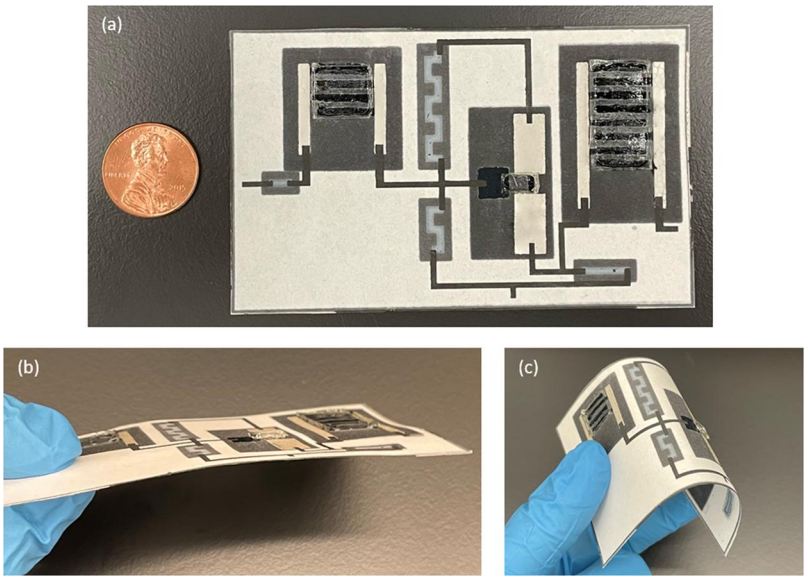

Figure 7. Images of customized amplifier paper PCB displaying (a) a small areal footprint, (b) slimness, and (c) flexibility.

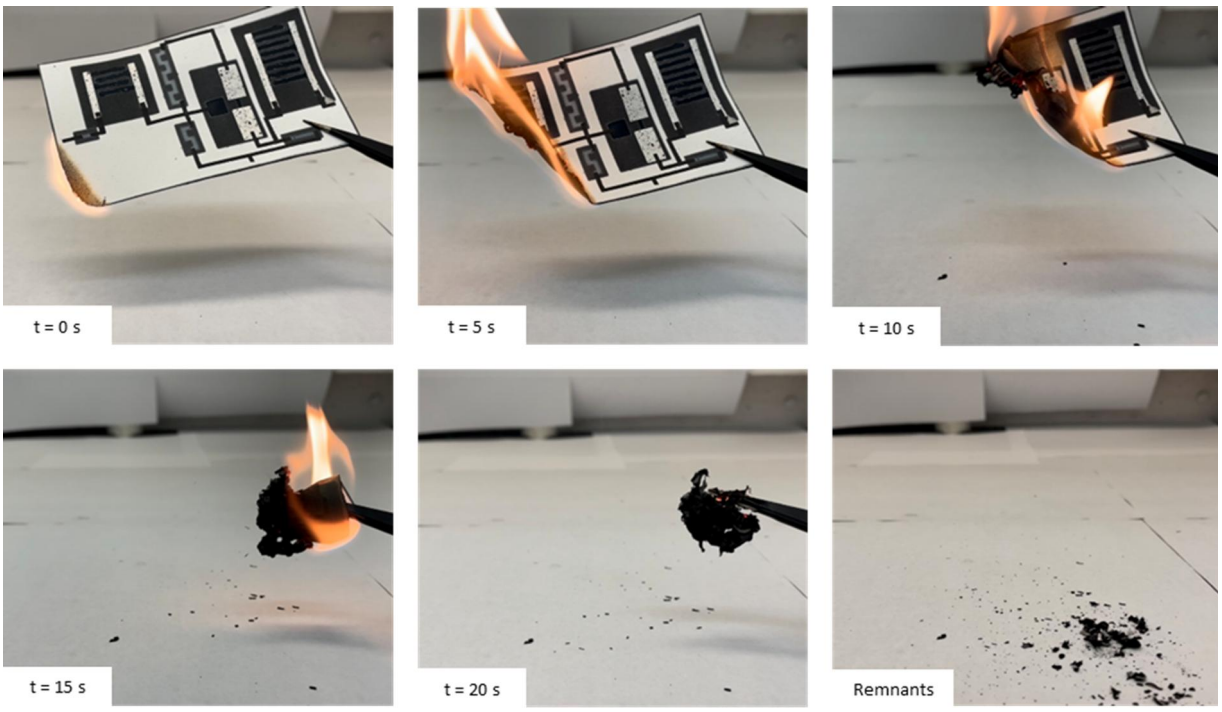

Figure 8. Time lapse of paper PCB burnability demonstration. Burning is carried out on a paper PCB with the gel electrolyte removed, and photographs are taken at 5 s intervals with the total burn time lasting 20 s.

or repellent force on the holes flowing across the channel from the source to the drain. When the gate voltage is positive, cations are driven toward the channel, repelling the flow of the positive charge carriers between the source and drain, whereas a negative gate voltage will push anions toward the channel, attracting more positive charges and increasing the observed current. Judging from the trends of the presented data, if the gate voltage was further increased beyond 5 V, the EFET may eventually reach a threshold gate voltage (V_{TH}) at which it is turned fully "off". This value is estimated by the semiconductor characterization system to be approximately 18.9 V. Additionally, when a larger gate voltage is applied, there is an observed reduction in the slope of the output characteristics as the drain voltage becomes more negative, indicating the desired behavior in which the drain current approaches a saturation point. As the gate bias is increased, appropriately, the saturated drain current decreases and the apparent corresponding pinch-off voltage at which this saturation is achieved is also lowered.

The fabricated n-type EFET (Figure 6a and Figure S2) is similarly characterized, although the drain current is measured while sweeping through positive drain voltages and negative gate voltages for the output and transfer characteristics, respectively (Figure 6b,c). The device successfully exhibits n-type depletion mode characteristics as a positive drain current is observed when the gate is unbiased. Under the same principle as explained for the p-type FET, the "on/off" state of the n-type FET is

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influenced by the applied gate voltage; though as n-type transistors rely on the flow of negative charge carriers rather than the positive, the opposite effect is observed. A negative gate voltage prompts electrolyte anions to cluster near the transistor channel, deterring the electron flow between the source and drain. This behavior is effectively observed in the characteristic data as transfer characteristics show an increase in the drain current as the gate voltage is lowered. Like with the p-type EFET, the output characteristics for the n-type EFET display a drain current saturation beyond a certain pinch-off drain voltage. Accordingly for an n-type, the trend is that a more negative gate voltage corresponds to a lower pinch-off voltage and lower saturation current. This device shows the potential to eventually be fully turned "off" beyond a threshold gate voltage, which is estimated by the characterization system to be approximately −20.3 V.

2.4. Paper PCB Design. The three types of paper components discussed previously have been specifically designed to be compatible with batch fabrication and the development of single-sheet paper printed circuit board (PCB) configurations. The paper resistors, capacitors, and transistors use the same filter paper as a substrate, employ similar functional materials and ink mixtures, and share many of the same fabrication steps. This allows for entire paper circuits to be fabricated in almost the same amount of time and steps that it takes to fabricate a single component. The whole process requires only six major steps before PCB completion: patterning of component regions via wax printing, wax infusion, functional ink application, screen printing of Ag/AgCl contacts, screen printing of conductive traces for component interconnection, and casting of the gel electrolytes (Figure 7). Practically, the only additional step required to build a paper PCB over individual components is the patterning of conductive traces appropriately to connect components, permitting the very customizable all-paper circuits to be produced at an optimal rate.

As a demonstration, a simple paper PCB was designed and effectively fabricated in just a couple of days. To integrate all three types of components, a basic amplifier circuit structure was chosen to incorporate four paper resistors (250 Ω, 450 Ω, 155 kΩ, and 285 kΩ), two capacitors (3 mF and 1 mF), and a transistor (Figures S3 and S4). Based on each component's characterization data, the physical parameters were appropriately designed and tuned to attain the desired values (Table S3). The resulting paper-based amplifier circuit features a spatially compact, exceptionally thin, and flexible design, effectively demonstrating the versatility and practicability of our proposed components for custom paper-based circuit solutions (Figure 7). The easy disposability is shown in Figure 8, where time-lapse photography shows the paper PCB being reduced to ashes 20 s after ignition. This work creates a new manufacturing paradigm for paper, which offers flexible and biodegradable properties while enabling low-cost fabrication of components and PCBs. Ultimately, it will result in a barrier-transcending advancement in integrated paper-based electronics along with the development of practical batch fabrication techniques (Figure S5).

3. FUTURE DIRECTION

The goal of this work is not to replace the conventional inorganic-based electronic industry. Rather, it offers opportunities for new techniques, applications, and markets in a way to reduce the dramatic increase in electronic waste. In this early stage of development, papertronics will not require high-tech integrated circuits with high resolution and reliability. However, once a fully paper-based system is validated, more research work for higher density and performance will be proposed. Additional packaging will be required for all paper-based devices because humidity may dramatically change paper morphology and degrade its performance and shelf life.[31] Furthermore, some potential exposure of paper to other microorganisms can biodegrade the paper through their enzymatic activities.[31] However, packaging will be a major element that will require a significant technological breakthrough. As a proof-of-concept demonstration, the amplifier was simply designed and its size was not comparable to conventional electronic circuits. However, paper's remarkable characteristics of folding and stacking will enable a multi-layered PCB with many components integrated within a small area.

4. CONCLUSIONS

This study revolutionizes the approach toward paper-based circuitry, featuring facile techniques for developing and integrating high-performance components into thin, flexible, and spatially compact paper PCBs. Our papertronic techniques describe an innovative fabrication by using the fluidic wicking properties of paper. Various conductive ink recipes are presented that can be used to functionalize a paper substrate for assembly and fine-tuning of three of the most essential electronic components: resistors, capacitors, and transistors. The characteristics of the designed components boasts a remarkably wide resistance range from 20 Ω to 285 kΩ, a high capacitance of approximately 3.29 mF, and potential for p-type and n-type FET behavior. The successful demonstration of these components on paper—without significant interference of something—shows the inherent flexibility, affordability, and disposability of the paper substrate and brings the field of paper-based circuitry one step closer to being fully embraced commercially and becoming ingrained in disposable electronic applications.

5. EXPERIMENTAL PROCEDURE

5.1. Materials and Equipment. Whatman Grade 1 qualitative filter paper, which is used as the substrate for all of the components, was purchased from Fisher Scientific. Clevios PH1000 poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS) was obtained from Heraeus. The 99% hydrolyzed polyvinyl alcohol (PVA, Mtw 89,000−98,000), 98% (3-glycidyloxypropyl)trimethoxysilane (GLYMO), graphene oxide powder (GO), multiwalled carbon nanotubes (MWCNTs), 99.99% palladium(II) chloride ($PdCl_2$), ethylene glycol (EG), ammonium chloride (NH_4Cl), and sodium hydroxide (NaOH) were all purchased from Sigma-Aldrich. The dimethyl sulfoxide (DMSO) was obtained from EMD Millipore Corp, 85% phosphoric acid (H_3PO_4) from Consolidated Chemical and Solvents LLC, Super 77 multipurpose spray adhesive from 3M, and E3449 graphite ink and E2414 silver/silver chloride (Ag/AgCl) ink from Ercon, Inc.

A Xerox Colorqube 8570 solid wax printer, Universal Laser Systems VLS 3.50 laser cutter, VWR symphony incubator, VWR analog vortex mixer, VWR hotplate/stirrer, Branson 2510 ultrasonicator, Labconco FreeZone 2.5 L −50 °C benchtop freeze dryer, and VWR C3303 laboratory centrifuge were used for device fabrication.

5.2. Component Fabrication. For each component, the paper substrate was first accordingly patterned with wax on both sides and placed in an oven at 150 °C for 10 s to melt the wax and allow for the formation of hydrophilic paper channels. All components were fabricated and tested in ambient lab conditions.

5.2.1. Resistors. To fabricate the paper resistors, pattered paper channels of both straight and zigzag configurations were functionalized with a semiconductive ink composed of PEDOT:PSS and DMSO. The

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ink was prepared by mixing 2 mL of PEDOT:PSS with the appropriate concentration of DMSO via a vortex mixer followed by additional sonication for 1 h. The appropriate volume of ink was then evenly applied to the paper channel using a micropipette, and the ink-injected paper was allowed to dry for 24 h before use. Three variables of the resistors were manipulated: length (0.5, 1.0, 1.5, 3, and 3.5 cm), ink volume (2, 3, 4, 5, 6, 7, 7.5, 10, 15, and 20 μL), and DMSO weight percentage (1, 5, 10, and 20 wt %). The resistance of each variation was measured to determine the influence of each variable and establish the resistance fine-tuning capabilities of the design. Graphite ink traces were screen-printed onto the filter paper with a fixed width of 1 mm and lengths of 0.5, 1.5, 3.5, 4.5, and 14 cm.

5.2.2. Capacitors. The hydrophilic paper channels for the paper capacitors were strategically patterned with an interdigitated structure in which the interdigital finger numbers are 8, 6, and 4, the gap between fingers is 0.5 mm, the finger length is 12 mm, and the finger width is 2.5 mm. The Pd-CNT-rGO/PEDOT:PSS ink was applied to each paper electrode. After air-drying for 24 h, the paper was incubated for an additional 20 min at 120 °C to reduce the proportion of water in the paper-applied electrode ink and enhance the stability after the addition of the gel electrolyte.[32] A laser-cut paper mask was then sprayed with adhesive and loosely applied to the paper capacitor substrate. The Ag ink was screen-printed over the mask to act as the current collector, and the paper mask was gently removed. After drying for several hours, a laser-cut plastic mold was firmly applied, and the gel electrolyte was cast over the capacitor active region. After solidification for 36 h, the mold was removed, and the paper capacitors were characterized.

The Pd-CNT-rGO functional material was prepared using a modified one-pot hydrothermal procedure.[22,23] For each sample, 10 mg of MWCNTs and 20 mL of a 1 mg/mL GO solution were mixed and sonicated for 1 h followed by the slow addition of a $PdCl_2$ suspension (733 mg in 10 mL of DIW) under constant stirring. The pH was adjusted to neutral via 1 M NaOH and sonicated for an additional 30 min. The suspension was placed in a Teflon-lined autoclave and incubated at 160 °C for 18 h, initiating a spontaneous redox reaction between the $PdCl_2$ and CNT-GO and resulting in the growth of ultrafine Pd-NPs on the surface of the CNT-GO. The purified Pd-CNT-rGO powder was obtained after repeated rinsing with DIW followed by centrifugation at 4000 rpm for 4 min and then freeze-drying for 36 h. The as-prepared powder was mixed with 2 mL of PEDOT:PSS with 5 wt % DMSO and 1 wt % GLYMO to obtain the capacitor electrode ink.

The gel electrolyte was prepared by first heating 10 mL of DIW to 90 °C using a hot plate followed by the slow addition of 1 g of PVA under constant stirring for 1 h until a clear, viscous mixture was obtained.[33] After cooling to room temperature, 0.475 mL of H_3PO_4 was added and stirred until combined.

5.2.3. Transistors. Both n-type and p-type EFET designs were fabricated in a planar arrangement with channel dimensions of 4 mm × 2 mm ($L \times W$, $W/L = 1/2$). To mimic the MOSFET architecture, the p-type EFET utilized a narrow paper region saturated with n-doped rGO-ink to act as the "substrate" and we screen-printed p-doped rGO-ink for the source and drain. The n-type EFET used a PEDOT:PSS ink with 5 wt % DMSO and 1 wt % GLYMO as the "substrate" (p-type) and an n-doped rGO ink for the source and drain. Like the capacitor, both EFET designs were further baked for 20 min at 120 °C for stabilizing the functional inks. The gate electrode and the source and drain metal contacts were achieved through Ag/AgCl ink screen printing. The PVA/H_3PO_4 gel electrolyte described for the capacitor was similarly cast over the active region of the EFETs, overlapping the channel region and the gate electrode.

The n-doped rGO ink was prepared by first sonicating 25 mL of DIW, 125 mg of GO, and 80 mg of NH_4Cl for 30 min. The mixture was then sealed in an autoclave and placed in the incubator at 200 °C for 24 h. The resulting n-rGO precipitate was then freeze-dried for 1−2 days. Once ready for application, the powder was mixed via a vortex with EG and DIW to achieve an n-rGO ink. The p-doped rGO was similarly prepared except that the NH_4Cl was replaced with 100 mg of H_3PO_4, the pH was adjusted to 7 using NaOH addition, and the p-rGO powder was blended with a PEDOT:PSS mixture with 5 wt % DMSO and 1 wt % GLYMO to make the ink.

5.3. Paper PCB Fabrication. The demonstrated paper PCB and any other desired custom PCB design can be fabricated in six basic steps (Figure S2). A wax printer is used to define different component regions, and the paper is incubated at 150 °C for 10 s to allow for the wax to absorb into the paper. The functional inks for each type of component are applied to the paper via ink injection or screen printing. After drying, Ag/AgCl contacts are accordingly screen-printed for the transistor and capacitor. Once set, the wiring between components is achieved via screen printing of graphite ink, though any conduction trace would be viable. The gel electrolyte is then cast over the capacitor and transistor active regions and allowed 36 h to solidify.

5.4. Characterization. Paper resistors were measured via a Lomvum T28B multimeter. Probes were firmly placed at opposite ends of each resistor and values were recorded once the device displayed a stable resistance. Paper capacitors were evaluated both with the multimeter and with a Squidstat Plus/Squidstat Power Supply unit. The multimeter was used for obtaining initial capacitance measurements, while the Squidstat system was used for further characterization with CV, galvanostatic EIS, and galvanostatic charge/discharge analysis. ZView 4.0 software was used for capacitor modeling. Paper transistor transfer and output characteristics were automatically measured via a Keithley 4200-SCS semiconductor characterization system.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.2c13503.

Resistance values, transistor characteristics, fabrication steps, amplifier circuit, and capacitance values (PDF)

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Notes

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