2D Materials

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Dot-product computation and logistic regression with 2D hexagonal-boron nitride (h-BN) memristor arrays

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Abstract

This work reports on the hardware implementation of analog dot-product operation on arrays of two-dimensional (2D) hexagonal boron nitride (h-BN) memristors. This extends beyond previous work that studied isolated device characteristics towards the application of analog neural network accelerators based on 2D memristor arrays. The wafer-level fabrication of the memristor arrays is enabled by large-area transfer of CVD-grown few-layer (8 layers) h-BN films. Individual devices achieve an on/off ratio of >10, low voltage operation (~0.5 V_{set}/V_{reset}), good endurance (>6000 programming steps), and good retention (>10^4 s). The dot-product operation shows excellent linearity and repeatability, with low read energy consumption (~200 aJ to 20 fJ per operation), with minimal error and deviation over various measurement cycles. Moreover, we present the implementation of a stochastic logistic regression algorithm in 2D h-BN memristor hardware for the classification of noisy images. The promising resistive switching characteristics, performance of dot-product computation, and successful demonstration of logistic regression in h-BN memristors signify an important step towards the integration of 2D materials for next-generation neuromorphic computing systems.

1. Introduction

Since the discovery of graphene [1], two-dimensional (2D) materials have been the focus of intense research and have shown great potential to advance the capabilities of future integrated electronic systems. Recent studies have proposed the possibility of adding new functionality through the hybrid integration of 2D materials with complementary metal oxide semiconductor technologies [2, 3]. Here, neuromorphic computing is recognized as one of the main applications of next-generation electronic systems enabled by 2D materials integration [2]. This unconventional computing paradigm aims at the implementation of artificial neural networks (ANNs) using compute-in-memory hardware to achieve energy-efficient data processing for machine learning and artificial intelligence (AI) applications. It requires devices that can emulate bio-inspired functions (e.g. artificial synapses and neurons) and memristors have emerged as a primary choice [4]. Memristors are electronic devices with variable resistance states that depend on their past and recent experience with external stimuli. Conventional memristor technologies are constructed from bulk materials and their resistive switching behavior can be achieved through various mechanisms (e.g. ionic transport [5], filamentary [6], phase change [7], charge trapping [8], etc). Filamentary metal-oxide resistive random-access memory (i.e. RRAM) [9] is a widely studied technology due to its non-volatility, high switching speed, low switching energy, and small footprint. Recently, several studies have reported the non-volatile resistive switching (NVRS) behavior of 2D materials down to single atomic layers [10, 11]. A variety of 2D materials were shown to exhibit NVRS properties including transition metal dichalcogenides (TMDs) [12], hexagonal boron nitride (h-BN) [13–15], black phosphorus

[16, 17], graphene [18, 19], etc. CVD-grown h-BN has attracted significant interest due to its compatibility with high-density wafer-scale integration [14, 15]. In CVD-grown h-BN memristors, the NVRS behavior is attributed to the formation and dissolution of conductive nanofilaments that result from the penetration and removal of metal ions (from the top electrode) into defects at grain boundaries in the h-BN film [20, 21].

Two-dimensional h-BN memristors have demonstrated superior properties compared to their bulk counterparts (e.g. metal-oxide memristors) [22], making them ideal candidates for future neuromorphic chips for AI applications. For example, they can extend the vertical scaling limit of oxide-based RRAM as their NVRS behavior endures even in atomically-thin h-BN monolayers [10, 22]. Moreover, the layered structure of h-BN may help alleviate programming errors and variability (e.g. stuck-at issues) associated with non-uniformity in the thickness of the resistive switching medium in bulk technologies [23]. Additionally, 2D h-BN memristors were shown to provide better analog control of conductance programmability (e.g. long-term potentiation/depression of artificial synapses) over a wide range of operating currents when compared to metal-oxide RRAM where programmability is limited only to a smaller range of high currents. This is attributed to filament formation happening in native defects surrounded by stable crystalline 2D layered h-BN [22]. In fact, the superior chemical stability of h-BN memristors is expected to also alleviate oxidation reaction to filaments and prevent the redundant formation of undesired paths, thus helping improve endurance which has been a persistent issue with oxide-based RRAM [24, 25].

Despite their great potential for neuromorphic hardware, few reports of dot-product computation using 2D memristors have appeared in the literature, even though it is crucial for most analog-based implementations of neural network accelerators [26, 27]. Previous work reported on dot-product computation in h-BN memristors (two devices in parallel) and its application towards hardware implementation of linear regression algorithms [15]. Here, we report a more extensive dot-product computation with larger arrays based on a wafer-scale process for 2D h-BN memristors. In addition to dot-product, our analysis elucidates the NVRS characteristics of wafer-scale CVD-grown h-BN memristors, including on/off ratio, low-voltage operation, endurance, retention, pulsed analog programmability. We examine the dot-product computation with respect to its accuracy, variability, and energy efficiency. This analysis, the first of its kind for a 2D memristor technology, represents significant progress towards the practical implementation of neuromorphic hardware using 2D materials. Finally, we demonstrate the implementation of a logistic regression learning algorithm to classify noisy images using our 2D h-BN memristor hardware with near-ideal performance and accuracy (by comparisons with simulations).

2. Results

Arrays of 2D memristors with a metal–insulator–metal structure are fabricated on Si/SiO_2 wafers using CVD-grown few-layer h-BN films. A photograph of a typical Si/SiO_2 wafer with the h-BN memristor arrays is shown in figure 1(a). This work reports on devices with Au bottom electrodes (BEs), and Ti top electrodes (TEs) (capped with Au). A micrograph of Au/h-BN/Ti memristor arrays under test is provided in figure 1(b), and details of a single device cross-section are depicted in figure 1(c). Each array shares a common BE while the TEs are distinct. The fabrication steps are illustrated in figure 2(a) and include the patterning and deposition/lift-off of the shared BEs (steps *i, ii, iii*), followed by transfer of the few-layer CVD-grown h-BN film (∼5 nm in thickness) and patterning of the active regions by dry-etching (steps *iv, v, vi*). Finally, the TEs are prepared by photolithography, e-beam evaporation, and lift-off (steps *vii, viii, ix*). More details on the fabrication of Au/h-BN/Ti memristor arrays are provided in the supplementary information. Figure 2(b) is a micrograph of two different fully-fabricated h-BN memristor arrays (1×3 and 1×10). We note that each fabricated sample contains over 200 h-BN memristor arrays and the majority of devices demonstrate reasonable resistive-switching behavior yielding >90% working devices. This is consistent with previous work that used similar methods for wafer-scale integration and processing of 2D memristive crossbars (reported 98% yield) [14]. A critical step in the fabrication of the arrays to achieve good resistive-switching behavior and high yield is the transfer of the CVD-grown h-BN film. Thus, to verify the quality of the h-BN film we conducted Raman spectroscopy at various randomly selected locations immediately after the transfer step. Figure 2(c) shows Raman spectra revealing peak positions at 1370 cm^{-1} for all different locations, consistent with previously published results on few-layer h-BN films [28]. Additional verification of the h-BN memristor structure is achieved via cross-sectional transmission electron microscopy (TEM) imaging (figure 2(d)) revealing the layered nature of the h-BN film. The dark and blurry regions in the TEM image may reveal lattice disorder and native defects along grain boundaries known to be responsible for conductive nanofilament formation and resistive switching behavior [29]. Compositional analysis using electron energy loss spectroscopy (EELS)

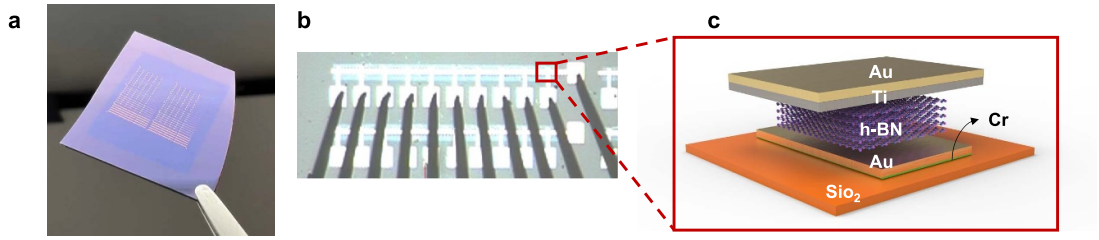

Figure 1. (a) Photograph of a typical 2D h-BN memristor array sample fabricated on a Si/SiO_2 wafer. (b) Micrograph of h-BN memristor arrays under test with shared bottom electrode and independent top electrodes. (c) Cross-sectional schematic of the few-layer h-BN memristor arrays with Ti/Au top electrode and Au bottom electrodes.

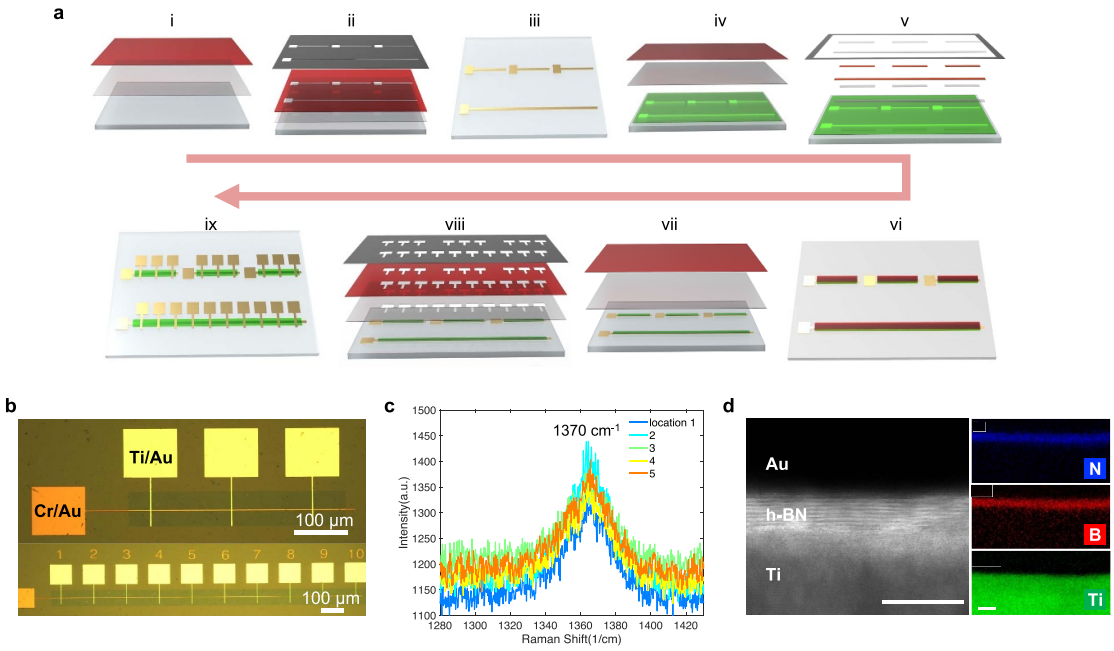

Figure 2. (a) Fabrication steps for h-BN memristor arrays on Si/SiO_2 wafers enabled by large-area transfer and processing of CVD-grown h-BN films. Steps include patterning and deposition of shared bottom electrodes, transfer, and patterning of the resistive switching few-layer h-BN film, and the patterning and deposition of independent top electrodes. (b) Micrograph of two different h-BN memristor arrays size 1×3 and 1×10. (c) Raman spectra for few-layer h-BN at 5 different locations after transfer onto Si/SiO_2 wafer. (d) Transmission electron microscopy (TEM) cross-sectional image of Au/h-BN/Ti/Au memristors, scale bar is 20 nm. Right panels show electron energy loss spectroscopy (EELS) elemental mapping highlighting regions of N, B, and Ti within the stack.

confirms the regions of N, B and Ti within the stack as highlighted in figure 2(d) (right panels).

A comprehensive analysis of the resistive switching behavior of h-BN memristors is provided in figure 3. Dual voltage sweep measurements are used to observe hysteresis in the current–voltage (I–V) characteristics associated with transitions between a high resistance state (HRS) and a low resistance state (LRS) [30]. In these measurements, a DC voltage across the top and BEs is swept (starting from zero) up to a positive value (e.g. 1.5 V), then back to a negative value (e.g., −1 V), and back to zero, all while measuring the current through the memristor. The results from 30 cycles of dual voltage sweeps are plotted in figure 3(a) for an h-BN memristor with 3 μm × 3 μm active area (area of overlap between top and BEs). The number labels indicate the sweep direction, each light gray line is data from a single cycle, and the blue line with circles is the average from all 30 cycles. A compliance (limit) is applied to the current at a value of 100 μA to control the programming of the LRS by limiting the 'strength' of the conductive path being formed. The measurements indicate repeatable results with little cycle-to-cycle variation and low set and reset voltages (approximately ±0.5 V for set/reset). Our results are consistent with previous work on thin CVD-grown h-BN memristors having forming-free bipolar resistive switching characteristics, as well as smaller set/reset voltages and on/off ratios compared to devices with thicker h-BN films [21, 29]. Figure 3(b) are cumulative distribution plots of the high and low resistance states (HRS and LRS) from all I–V measurement cycles extracted at a read voltage of $V_{read} = 0.1$ V. The cumulative distribution plots reveal an on/off ratio exceeding an order of magnitude (i.e. >10× ratio).

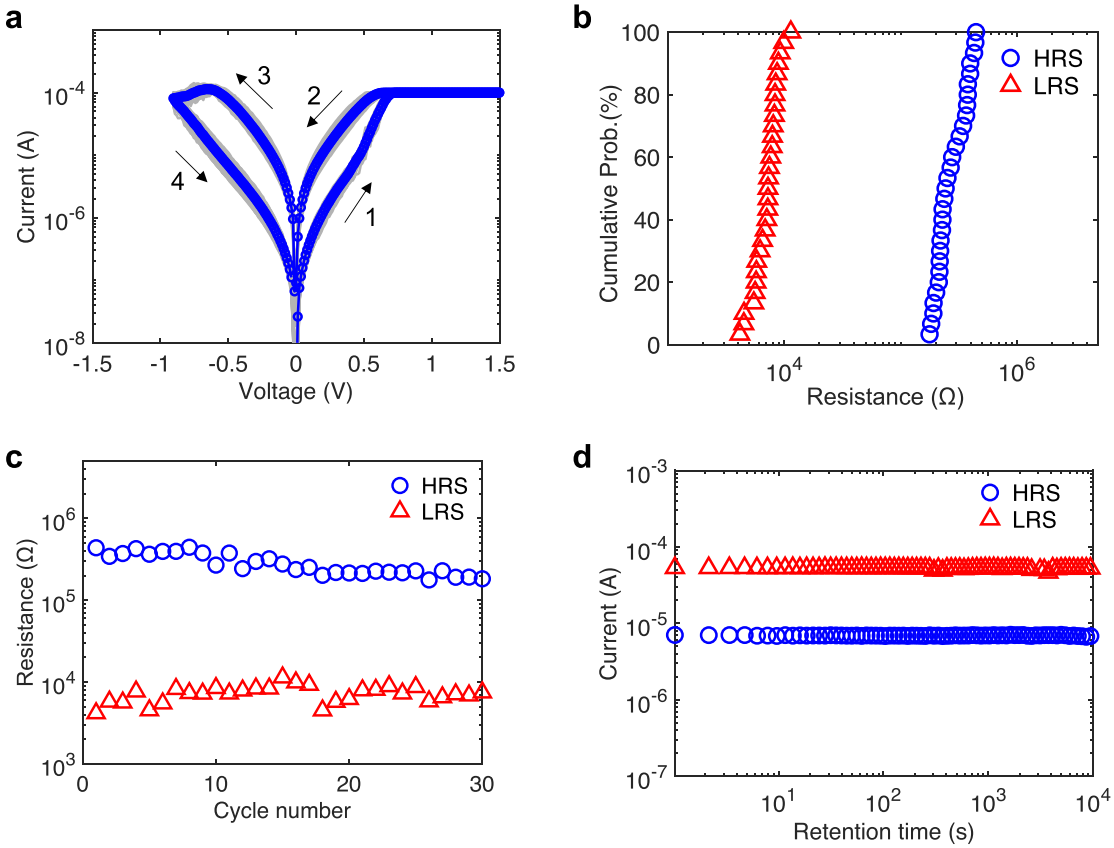

Figure 3. (a) Thirty cycles of current–voltage (I–V) characteristics measured with dual voltage sweeps on a few-layer h-BN memristor with 3 μm × 3 μm active area. (b) Cumulative distribution plot of HRS and LRS extracted at the read voltage of 0.1 V. (c) The resistance corresponding to HRS and LRS plotted as a function of cycle number. (d) Room temperature retention test on an h-BN memristor (active area of 3 μm × 3 μm) at V_{read} = 0.1 V for up to 10 000 s (LRS and HRS values shown).

Figure 3(c) shows the extracted HRS and LRS from the same device as a function of cycle number, showing good cycle-to-cycle repeatability. Finally, figure 3(d) shows the results from a room temperature retention test, where the current in an h-BN memristor is sampled at V_{read} = 0.1 V for up to 10 000 s immediately after programming to HRS and LRS. The results from the retention test show negligible drift in the programmed state of the h-BN memristors. This could suggest another potential advantage of 2D h-BN memristors over conventional (bulk) oxide-based RRAM which suffers from retention-induced conductive drift that can lead to significant degradation in inference accuracy in neuromorphic computing systems [31, 32]. We note that previous work on h-BN memristors has shown a transition from NVRS (long-term memory) to volatile behavior (short-term memory) by limiting the current (compliance). This 'threshold-type' resistive switching behavior can enable neuromorphic functions like spike-rate dependent plasticity [14, 33].

In figure 4(a), we explore the analog programmability of the h-BN memristors using 100 ns pulses. We use voltage amplitudes of 0.9 V for positive pulses and −1.1 V for negative pulses. We apply 15 consecutive positive pulses followed by 15 consecutive negative pulses and measure the current after each pulse using V_{read} = 0.1 V. The measured data is plotted for 200 cycles (a total of 6000 pulses). Here, the gray lines correspond to the individual 30-pulse cycles, and the red line with circles is the average for all 200 cycles. The results indicate good monotonic behavior with pulse polarity (i.e. current increases with positive pulses and decreases with negative pulses). Moreover, the h-BN memristors show good endurance to pulse programming as evidenced by consistent resistive switching behavior even after 6000 pulses. We note that the dynamic range in figure 4(a) (range of programmed currents) is small (∼2.5×) due to the small amplitudes of the programming pulses (+0.9 V and −1.1 V). Additional programming data with different pulse amplitudes are provided in supplementary figures 3 and 4. We can estimate the programming energy (energy used in changing conductance with a single programming pulse) assuming a current of approximately 45 μA (estimated current for V_{pos} = 0.9 V instead of V_{read} = 0.1 V) and using t_{set} = 30 ns to obtain $E_{set} = (V_{pos})(I_{set})(t_{set}) \sim 1.2$ pJ/pulse. In this calculation we use t_{set} = 30 ns instead of 100 ns (test instrument limitation), as determined by extrapolation of transient measurements indicating that

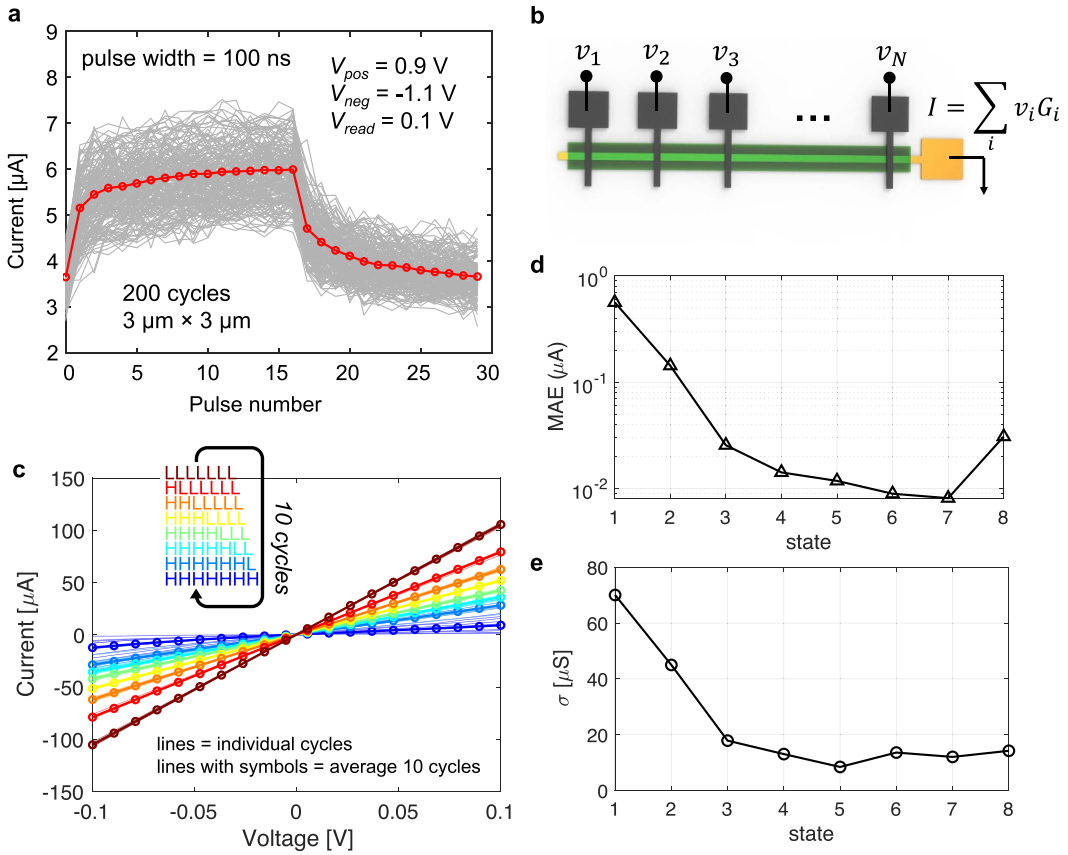

Figure 4. (a) Pulse programming of a single h-BN memristor over 200 cycles. For each cycle we apply 15 positive pulses followed by 15 negative pulses (amplitudes are +0.9 and −1.1 V respectively, all pulses are 100 ns in width). After each pulse the current is measured using $V_{\text{read}} = 0.1$ V. Red line with circles is the average of all 200 cycles. (b) Schematic of the h-BN memristor array illustrating the dot-product operation. (c) Dot product computation in hardware: we sequentially program individual devices from HRS to LRS then sweep the voltage on the top electrodes (all at same voltage) while measuring the total current on the shared BE. The measurement is repeated for 10 cycles (solid lines with circles are the average from all 10 cycles). Figures (d) and (e) are mean absolute error (MAE) and standard deviation in the dot-product computation (see text for more detailed description).

approximately 20–30 ns is sufficient to switch the h-BN memristors (see supplementary figure 5). Note that this programming energy is higher than the energy used in reading the device in a dot-product operation as will be described next.

Having verified the NVRS and analog pulse programmability of individual devices, we then test an array of h-BN memristors. Figure 4(b) is a schematic of the array, where we illustrate the voltages applied to each top electrode, and the total current through the shared BE given by the dot-product of voltages (v_i) and the corresponding memristor conductances (G_i) as $I = \sum_i v_i G_i$. For the dot-product test, we sequentially program individual devices from HRS to LRS (7 devices in a row). We conduct a voltage sweep on the TEs (all TEs at the same voltage) after programming each device. During the sweep, we measure the total current through the shared BE. Once all devices have been programmed to LRS, we reset all devices to HRS and begin the next cycle (repeated 10 times). The data is shown in figure 4(c) as current vs. the swept voltage. Here, each color represents a different 'state' corresponding to a different number of memristors in LRS. For each state, we plot the individual cycles (lines) as well as the average (thick lines with circles). This is a direct measurement of dot-product implementation on memristor hardware scanning both relevant parameters (i.e. voltages and conductances) [15]. We note that the dot-product computations show good linearity and reproducibility (quantitative analysis below). We estimate read energy from the dot-product measurements as $E_{\text{read}} = (V_{\text{read}})(I_{\text{read}})(t_{\text{read}})/N$, where N is the number of memristors in parallel. For the worst case (all devices in LRS), the energy is between 200 aJ and 20 fJ per operation (each MAC counted as two operations).

3. Discussion

Non-ideal memristor behavior (e.g. nonlinear I–V characteristics) as well as variability in conductance programming (inherent stochastic nature of filamentary resistive-switching mechanisms) can lead to inaccuracy in the computation of dot-products [34–36]. This inaccuracy can introduce significant

error in the implementation of ANNs using memristor hardware. To quantify accuracy in dot product computation, we calculate the MAE as well as the standard deviation in our implementation using h-BN memristor arrays. To obtain MAE, we perform a linear fit to the average currents (symbols) in figure 4(c) for each state (using a least-squares method). This linear fit represents a perfectly linear or 'exact' dot-product implementation for each corresponding state. We then compare the experimental values (all cycles) against the exact calculation to obtain MAE over the entire voltage range (from −0.1 V up to +0.1 V). MAE is plotted in figure 4(d) for each different state (average over all cycles). As shown, the error is largest for state = '1' which corresponds to all devices in HRS. However, this MAE is relatively small (<1 μA) compared to the range of current (up to ∼100 μA) and drops significantly (down to ∼10 nA) with more devices in LRS. We attribute the small error in the dot-product computation to good linearity in the h-BN memristor I–V characteristics over this read voltage range (from −0.1 V to +0.1 V). We also quantify cycle-to-cycle variability based on extractions of standard deviation (σ) in the *effective state conductance* from the dot-product data (i.e. the slope from the I–V characteristics in figure 4(c)). The standard deviation is plotted in figure 4(e) for each different state, where the largest deviation of ∼70 μS happens for state = '1' which corresponds to all devices in HRS. We note that this is small compared to the full range of conductance (200–1000 μS) in the dot-product implementation. Memristor instability (i.e. retention-induced conductive drift) can also lead to inaccuracy in dot-product computations. However, our retention test results (figure 3(d)) show negligible drift in HRS and LRS. Moreover, previous results [15] show good retention and stability over multiple conductive states in the same type of devices.

As a demonstration of dot-product computation in a machine learning algorithm, we present the implementation of gradient-descent-based stochastic logistic regression for image classification. Logistic regression is widely employed for object categorization and pattern identification. Here, we carry out the hardware-level computation of dot-product (including the corresponding weight updates) on an array of h-BN memristors. Gradient descent is an iterative optimization approach for minimization of a cost function associated with classification error [37]. In *stochastic* gradient descent (an online version of this technique that process data one observation at a time [38]), the weight updates (pulse-based adjustments in conductance) are exerted on the h-BN memristor array at every iteration in the training process. Since memristive crossbar arrays are unable to achieve the steepest gradient descent in an effective manner due to device limitations, we use a modified (hardware-compatible) gradient descent rule to train the h-BN memristor array [39]. In this approach, a single pulse or a set of consecutive programming pulses (with fixed amplitude and width) are applied to update the conductance of each memristor in the array as determined by the magnitude and polarity required weight updates given by the gradient descent optimization algorithm [27, 39–41]. In this demonstration, we use a dataset of size 500 containing 3 × 3 pixel noisy binary images of characters 'T', 'L' and 'n' (training images). We train a 9 × 1 h-BN memristor array to discern images of character 'T' from the other characters in a separate dataset (test images). We note that the training and test images are independently generated with one randomly flipped pixel. Figure 5(a) shows a subset of the images illustrating the ideal characters (1st image for each row) as well as some noisy samples (1 modified pixel).

The training process includes two consecutive steps during each iteration: a feedforward integration mode and a feedback update mode. In feedforward integration mode, vector-matrix multiplication (a collection of dot-products) is performed to achieve a hypothesis based on the accumulated output currents. In this hardware implementation, each binary picture pixel is translated to a crossbar input voltage equal to +0.1 V for white pixels and −0.1 V for black pixels, as shown in figure 5(b). Importantly, these input voltages are within the range in the I–V characteristics of h-BN memristors showing good linearity in dot-product computation (see figure 4(c)). Then, the image-dependent array of voltages is applied as inputs to the memristor array to obtain an output current given by $I_j = \sum_{i=1}^{9} v_i G_i$ (i.e. the dot-product of input voltages and conductance 'weights'). We then apply the logistic activation function $f_j = \frac{1}{1+e^{-I_j}}$ to the (normalized) current to obtain an output bounded between 0 and 1. This output represents the likelihood that the input image corresponds to a specific category (i.e. corresponds to a specific character like 'T'). Each training image contains a 'label' that indicates if it corresponds to a given category. In this example we are training the memristor array to recognize character 'T' from the rest, so the training images have label $y_j = 1$ for character 'T' and $y_j = 0$ for all other characters. At each training step, the classification error is calculated as $\delta_j = f_j - y_j$. In feedback update mode, the conductance update (weight update) for each memristor is calculated as $\Delta G_{ij} = -\delta_j v_i$. Here we use a simplified, hardware-compatible update rule where a single programming pulse of polarity determined by the sign of ΔG_{ij} is applied to change the conductance of each memristor in the array. We use programming pulses with fixed widths and amplitudes of 30 ns, and +2.5 V/−2.6 V respectively. Figure 5(c) provides a flow diagram illustration of one iteration in our implementation of stochastic logistic regression on h-BN memristor

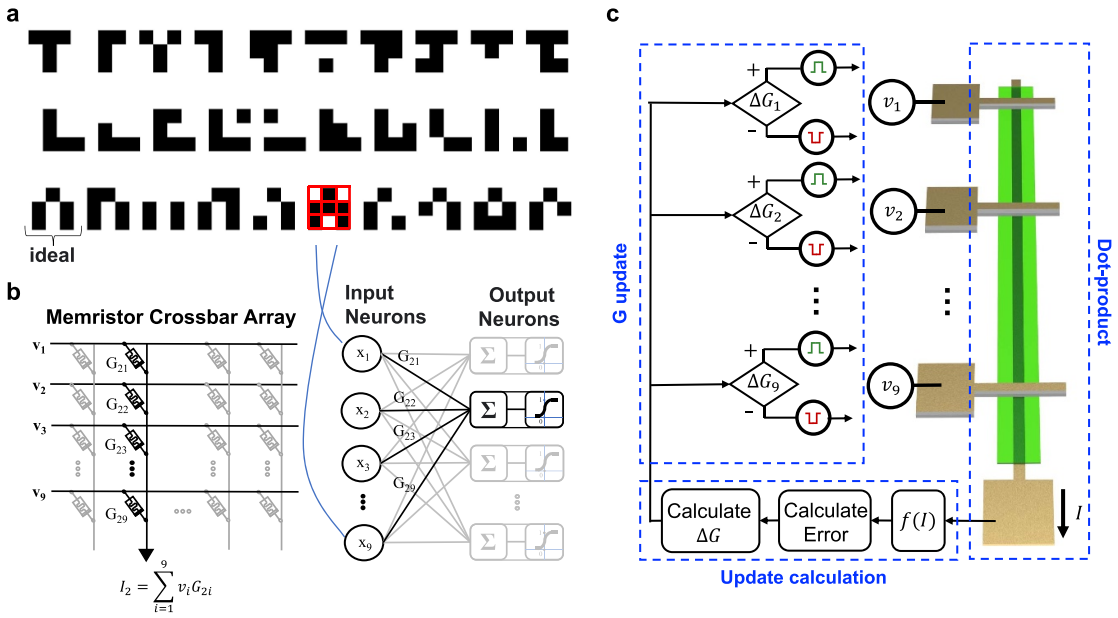

Figure 5. (a) Training images (1st image is the ideal case, without noise) including noisy images (one pixel flipped). (b) Graph illustration of logistic regression on h-BN memristor arrays. (c) A flowchart representing one iteration step in the training process for stochastic logistic regression: each pixel from the training image is translated to an input voltage and applied to the top electrodes in the memristor array. The output current is measured at the bottom electrode shared by all memristor devices in the array. A logistic function is applied to the normalized current, and the classification error is calculated using the training image labels to obtain the required conductance update ΔG (see text). The conductance of each h-BN memristor in the array is then updated through the application of positive or negative programming pulses.

array hardware. Resistive-switching I–V and pulsed characteristics of individual devices from the same h-BN memristor array are provided in supplementary figure 4. As presented below, the algorithm implementation reveals good immunity to reasonable levels of device-to-device experimental variability. Nonetheless, variability should be improved by optimized h-BN transfer methods (or by transfer-free deposition) and array design.

Figure 6 summarizes the results of the classification algorithm implemented on the arrays of h-BN memristors. At predetermined training intervals, the classification accuracy is assessed using the test images. Figure 6(a) plots the output of the logistic function (f_j) as a function of training step (iteration). This is actually the average for all test images (100 test images for each character). The different lines with symbols correspond to the measured output for each different character (maroon for 'T', blue for 'n', and green for 'L'). We see that for images of character 'T' the value approaches 1, while for 'L' and 'n' it approaches 0, meaning an accurate classification as this array was trained to classify character 'T'. Also shown in figure 6(a) are simulation results for the hardware implementation of stochastic multivariable logistic regression. The shaded regions indicate the range of the simulation results (minimum to maximum) from 10 different runs using random initial conductance values, and the solid line is the average. A small learning rate is factored into the conductance updates obtained from gradient descent to ensure a gradual change in conductance and improve convergence. In our simulations, we bound conductance values to G_{min} and G_{max} values obtained experimentally from pulse testing of the h-BN memristors. Additional details on the simulations are provided in the supplementary information. The simulation represents an ideal situation where conductance updates are perfectly controlled (no variability) for all memristors in the array, and the dot product is linear and without cycle-to-cycle variability. The comparison between simulations and experiments indicates that our hardware implementation achieves similar performance and accuracy to the ideal case. We note more abrupt changes in the experimental data, likely due to abruptness in changes of memristor conductance, but this appears to have little impact on the final accuracy. The rest of the results in figures 6(b)–(e) are only for experimental results on the h-BN memristor arrays. Figure 6(b) shows the confusion matrix for the f_j values before and after 500 training steps. Clearly, the classification improves significantly with training, in accordance with figure 6(a). Figure 6(c) shows a conductance map of the h-BN memristor before and after the hardware-implemented training. It is observed that after 500 training steps the pattern 'T' becomes noticeable, while before training the conductance pattern was random. A reasonable explanation for the full brightness of pixel 3 is the maximum percentage of reinforcement applied to

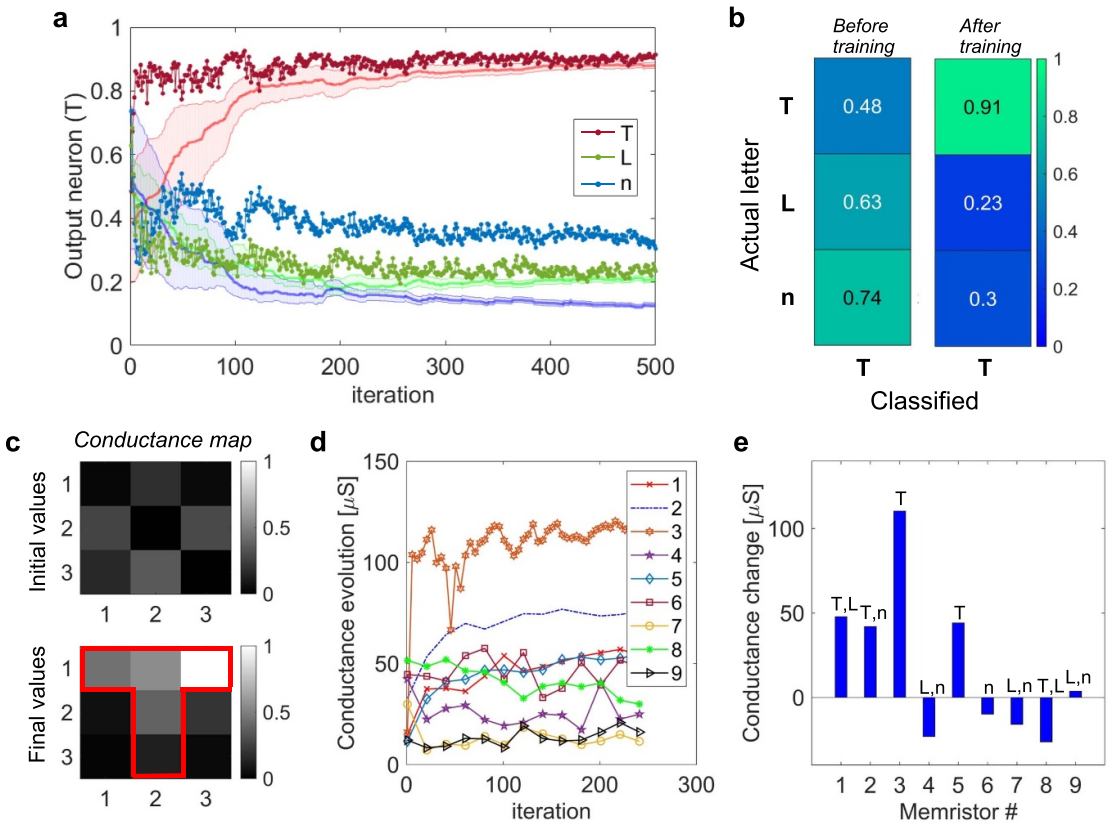

Figure 6. (a) Convergence of a logistic regression algorithm implemented on h-BN memristor arrays as described by the output of the logistic function indicating accurate classification of noisy pixel images. Lines with symbols correspond to experimental data on h-BN memristor array hardware, shaded regions with solid lines correspond to the range and average results from 10 MATLAB simulations with ideal memristor response. (b) Confusion matrix for hardware classification of character 'T' before and after training. (c) Conductance maps before and after training revealing the pattern 'T' after 500 iterations. (d) Evolution of experimental conductance values as a function of training step (iteration). (e) Change in conductance during training shows that memristors that correspond to pixels unique to the training pattern (character 'T') are strongly reinforced (large positive change in conductance) compared to those that
are not.

this pixel during training since it is only present in pattern 'T' (not in 'L' or 'n'). In fact, this is evident in the evolution of conductance for the full array over the course of 250 training steps plotted in figure 6(b). Another visualization of the learning process is the change in conductance during training for each h-BN memristor as plotted in figure 6(e). As shown, devices that correspond to pixels that are in the ideal 'T' pattern are more strongly reinforced (positive change in conductance) compared to the pixels that are not.

4. Conclusion

We report on the wafer-scale fabrication of h-BN memristor arrays to enable dot-product computations and the hardware implementation of machine learning algorithms. We show the resistive switching behavior of few-layer h-BN memristors having low set/reset voltages, >10× on/off ratio, good endurance, retention, and nonvolatile analog pulse programmability. We present the hardware computation of dot-products on an arrays of h-BN memristors. This work provides a quantitative analysis of dot-product revealing good linearity, reproducibility, and energy efficiency as determined by MAE, standard deviation, and program/read energy (e.g. attojoule range per read operation). Finally, we demonstrate a hardware-compatible implementation of stochastic logistic regression on h-BN memristor arrays for image classification. The experimental results show classification accuracy and algorithm performance comparable to arrays with ideal memristive behavior (from simulations). Exceptional resistive switching characteristics, dot-product performance, and implementation of logistic regression in h-BN memristor arrays indicate a significant step towards the integration of 2D materials for next-generation neuromorphic computing systems.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgments

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