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van der Waals ferroelectrics: Progress and an outlook for future research directions

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ABSTRACT

The recent discovery of van der Waals (vdW) ferroelectric materials has inspired their incorporation into numerous nonvolatile technologies and shown potential promise for various device applications. Here in this perspective, we evaluate the recent developments in the field of vdW ferroelectric devices, with discussions focusing on vdW heterostructure ferroelectric field-effect transistors and vdW ferroelectric memristor technologies. Additionally, we discuss some of the many open questions that persist in these technologies and possible pathways research can take to answer these questions and further advance the understanding of vdW ferroelectric materials.

I. INTRODUCTION AND BACKGROUND

In recent decades, two-dimensional van der Waals (vdW) materials have garnered much interest because of their unique properties, diverse applications, and promising potential to replace current silicon-based technologies.[1–3] These materials are generally characterized as atomically thin mono- and few-layers, with strong in-plane covalent bonds and weak out-of-plane vdW forces holding the atomic layers together. Importantly, vdW layers can be readily incorporated with disparate materials into vertically stacked heterostructures, as there is no requirement for lattice matching due to the absence of surface dangling bonds. This provides abundant opportunities for constructing vdW heterojunctions with desired properties and device functions.

Underpinning the technological potential is a fundamental knowledge of material properties. Compared to other optical and electrical characteristics of vdW materials that have been extensively investigated, ferroelectricity in these materials is still in the relatively early stage of exploration. Nonetheless, research in this direction has already yielded many interesting results that have the potential to enable novel device concepts. In this perspective, we will briefly review representative ferroelectric vdW materials and recent progress in demonstrating various device concepts; we will then discuss a few open questions that, in our opinion, should be addressed to further advance this promising field.

Ferroelectricity, in general, is characterized by spontaneous electric polarizations that arise from a non-centrosymmetric lattice. The in-plane and/or out-of-plane orientations of these polarizations can be manipulated, as desired, through the application of an external electric field. After the electric field has been removed, the lattice retains the defined polarization, leading to a stable polarization state that can persist for days[4] and even years.[5] The tunability of polarizations and retention is the basic operating mechanism for device applications, such as nonvolatile memory,[6–9] logic,[10–13] and transistors.[10,13–21] On the other hand, because of the depolarization field, ferroelectricity is suppressed when the material thickness is smaller than a critical value. As an example, this critical thickness is ∼1.2 nm (three unit cells) in BaTiO3 thin films.[22,23] More recent advancements have shown evidence of ferroelectricity in freestanding $BiFeO_3$ persisting down to ∼0.8 nm (two unit cells) in thickness.[24] On the other hand, the recent discovery of atomically thin vdW ferroelectric materials provides additional possibilities to overcome such a limit. In particular, vdW ferroelectrics, such as $CuInP_2S_6$ (CIPS), α-In_2Se_3, SnS, SnSe, SnTe, 1T′-$MoTe_2$, 1T′-MoS_2, and 1T′-WTe_2, have been demonstrated.[4,25–32] The ferroelectricity in many of these materials can persist down to the monolayer level at room temperature,[27,28,33] overcoming the thickness limit encountered in conventional oxides. While impressive progress has been made in all these materials, here we focus on CIPS and α-In_2Se_3 as representative examples to illustrate the potential of these materials in device applications.

Between these two ferroelectrics, there are fundamental differences in the origins and the characteristics of spontaneous

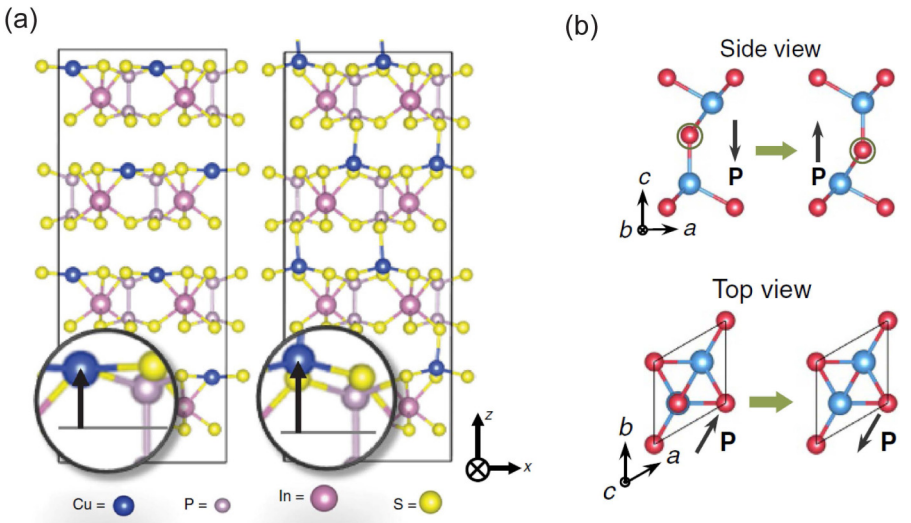

FIG. 1. Schematic of ferroelectric crystal structures. (a) Side view of CIPS demonstrating the displacements of Cu atoms along the *z* axis, defining the OOP polarization states. Reproduced with permission from Brehm *et al.*, Nat. Mater. **19**, 43 (2020). Copyright 2019 Springer Nature. (b) Side and top views of α-In_2Se_3 highlighting the displacement of the middle Se atoms, defining the interlinked OOP and IP polarizations. Reprinted with permission from Ding *et al.*, Nat. Commun. **8**, 14956 (2017). Copyright 2017 Author(s), licensed under a Creative Commons Attribution (CC BY) license.

polarizations. In CIPS, ferroelectric polarizations are controlled by Cu atoms, which can be displaced along the *c* axis when acted upon by an external electric field. In addition, a recent report has also shown that the ferroelectric properties of CIPS are dependent on the thickness of the sample, demonstrating that CIPS undergoes a structural phase transition from a monoclinic (*Cc*) crystal structure in bulk samples to a trigonal (*P*31*c*) crystal structure for thinner samples below a critical thickness of ~90 nm.[34] Interestingly, bulk samples above the critical thickness possess both out-of-plane (OOP) and in-plane (IP) ferroelectric polarizations as the displaced Cu atoms have both a vertical and a lateral component to the displacement. However, CIPS layers with thicknesses below ~90 nm only possess OOP ferroelectric polarizations. Furthermore, it has been reported that the displaced Cu atoms reach equilibrium in four distinct positions along the *c* axis,[35] allowing the lattice to possess two OOP polarization phases [Fig. 1(a); reproduced from Ref. 35]. In one pair of positions, Cu atoms are displaced upward and move into the vdW gaps between the monolayers, forming a bond with the nearest S atom in the adjacent monolayer layers. In the other pair of positions, Cu atoms are displaced downward out of the vdW gap and reside in the individual monolayers. Therefore, the equilibrium positions of Cu dictate the OOP polarizations in CIPS. In α-In_2Se_3, the position shift of the central Se atom layer leads to polarizations [Fig. 1(b); reproduced from Ref. 26]. Such a shift, in contrast to thin CIPS layers, breaks both OOP and IP symmetry, leading to simultaneous and interlinked OOP and IP polarizations even in monolayer α-In_2Se_3.[26,33] An advantage of this intercorrelation is the capability to control OOP (IP) polarization direction using the IP (OOP) electric field, providing great flexibility in device design and integrations.

II. RECENT DEVELOPMENTS IN VAN DER WAALS FERROELECTRIC DEVICE TECHNOLOGIES

Among the various devices being explored, ferroelectric field-effect transistors are one of the most common device structures with a wide range of applications. In addition, the ferroelectric memristors represent a relatively newer development that has been proposed as a critical component in solid-state neuromorphic computing. In the following, we provide a brief review of these two applications as examples.

A. van der Waals heterostructure ferroelectric field-effect transistors

Field-effect transistors have played a central role in the development of semiconductor devices and modern technologies. Conventionally, the geometric design of a field-effect transistor is a vertical stack of a metal (gate)/ oxide (dielectric)/ semiconductor (channel) structure. The basic function is to control the conductivity of the semiconductor channel between the source and drain electrodes. This is generally accomplished by applying and maintaining a bias to the gate electrode, which in turn, capacitively induces through the oxide, n-type, or p-type conduction in the semiconductor channel. In contrast, ferroelectric materials can offer nonvolatile control of the channel conductivity via the interaction between surface-bound charges and the channel, with the polarity of bound changes controlled by an external electric field.

With the recent advances in vdW material-based devices, a significant part of the current research has focused on integrating vdW ferroelectrics into field-effect transistors. One of the first reported all-vdW ferroelectric field-effect transistors used CIPS as the control medium and MoS_2 as the semiconductor channel material,[18] as shown in Fig. 2 (reproduced from Ref. 18). The fabricated device displayed a clockwise hysteresis loop in the MoS_2 channel drain-source measurements, indicating that CIPS was the source of the gating effect observed. The device exhibited an on/off ratio of the channel current of $\geq 10^2$, demonstrating the feasibility of the vdW ferroelectric gating mechanism. Since these initial findings, further developments have been realized in CIPS-based ferroelectric field-effect transistors as shown in Fig. 3 (reproduced from Ref. 21), with the most recent devices able to achieve on/off ratios of the channel current of $\sim 10^4$–10^7, endurance cycles of up to 10^4, retention times of up to an estimated ten years, and write/erase times in the μs range.[10,13,19–21] Along with the performance

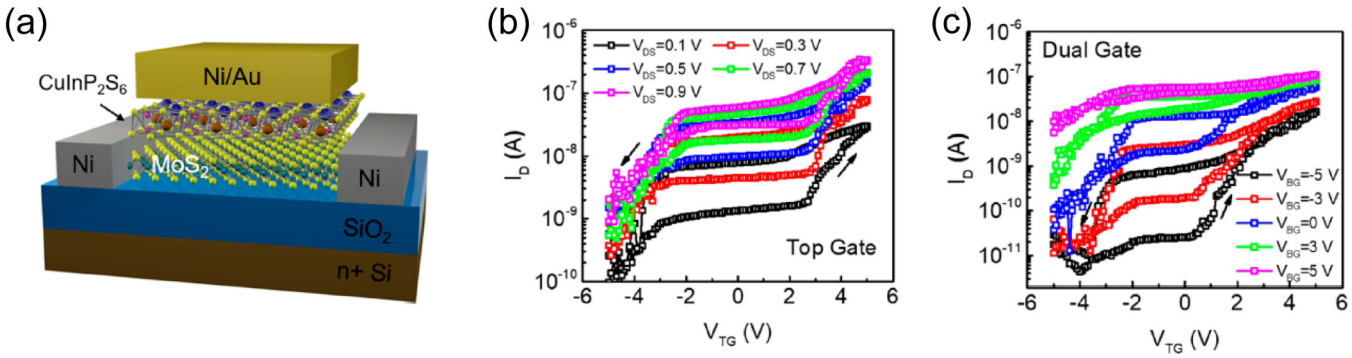

FIG. 2. Transport properties of MoS_2/CIPS vdW heterostructure ferroelectric field effect transistor with different gating controls. (a) Schematic of the device. (b) Top-gate I_D–V_{TG} and (c) dual-gate characteristics displaying counterclockwise hysteresis loops, demonstrating ferroelectric gating control of the current in MoS_2. Reproduced with permission from Si *et al.*, ACS Nano **12**, 6700 (2018). Copyright 2018 American Chemical Society.

advances, more complex circuit components have been fabricated and analyzed, such as an inverter circuit[10,13] as shown in Fig. 4 (reproduced from Ref. 10).

B. van der Waals ferroelectric memristors

Memristors, proposed to be the fourth fundamental circuit component, are circuit elements in which the resistance can be continuously tuned as a function of external voltage pulses. Memristive characteristics, which have been realized in numerous schemes with various mechanisms,[7,36–39] can be utilized to construct solid-state synapses as part of the neurocomputing network.[9,12,38,40] Much of the early research on ferroelectric memristors was based on oxide ferroelectrics.[41–46] The recent development of vdW ferroelectric memristors has focused mainly on α-In_2Se_3. Due to its unique OOP/IP polarization coupling, the

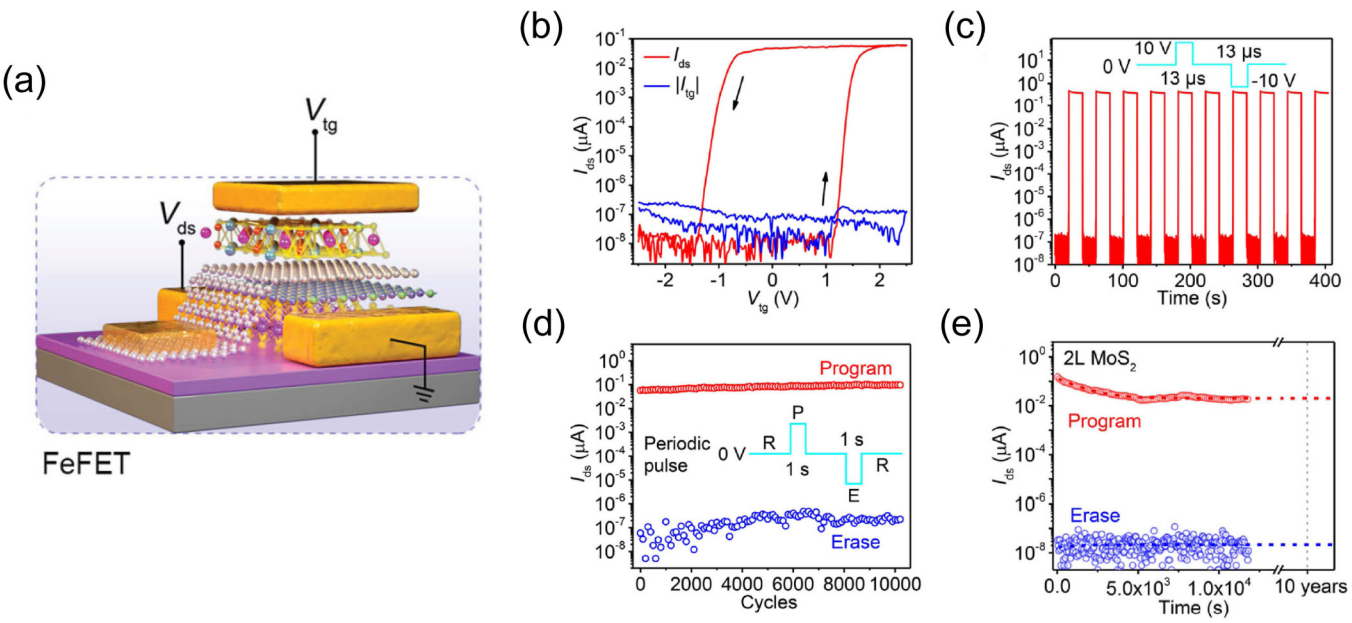

FIG. 3. Transport properties and performance characteristics of MoS_2/hBN/Gr/CIPS vdW heterostructure ferroelectric field effect transistor. (a) Schematic of the device and active terminals labeled. (b) Top-gate I_{DS}–V_{TG} transport characteristics (red) and minimal gate leakage current (blue). The I_{DS}–V_{TG} transport characteristics show counterclockwise hysteresis loops in the channel current, indicating the gating to be originating from the ferroelectric CIPS. (c) Large change in the channel current through ferroelectric gating achieved through μs-long write and erase pulses. (d) Endurance characteristics with over 10^4 cycles. (e) Retention characteristics stabilizing at over 10^4 s and demonstrating an estimated retention time up to ten years. Reproduced and adapted with permission from Wang *et al.*, Nat. Commun. **12**, 1109 (2021). Copyright 2021 Author(s), licensed under a Creative Commons Attribution (CC BY) license.

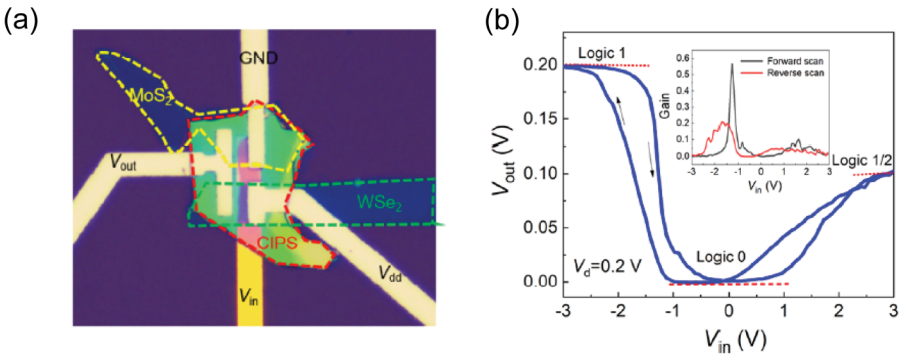

FIG. 4. Demonstration of a vdW ferroelectric field effect transistor ternary invertor circuit. (a) Optical image of a vdW Fe-FET ternary invertor circuit. (b) V_{out}–V_{in} characteristics of the circuit showing three logic states can be achieved. Reproduced and adapted with permission from Jiang *et al.*, ACS Appl. Electron. Mater. **3**, 4711 (2021). Copyright 2021 American Chemical Society.

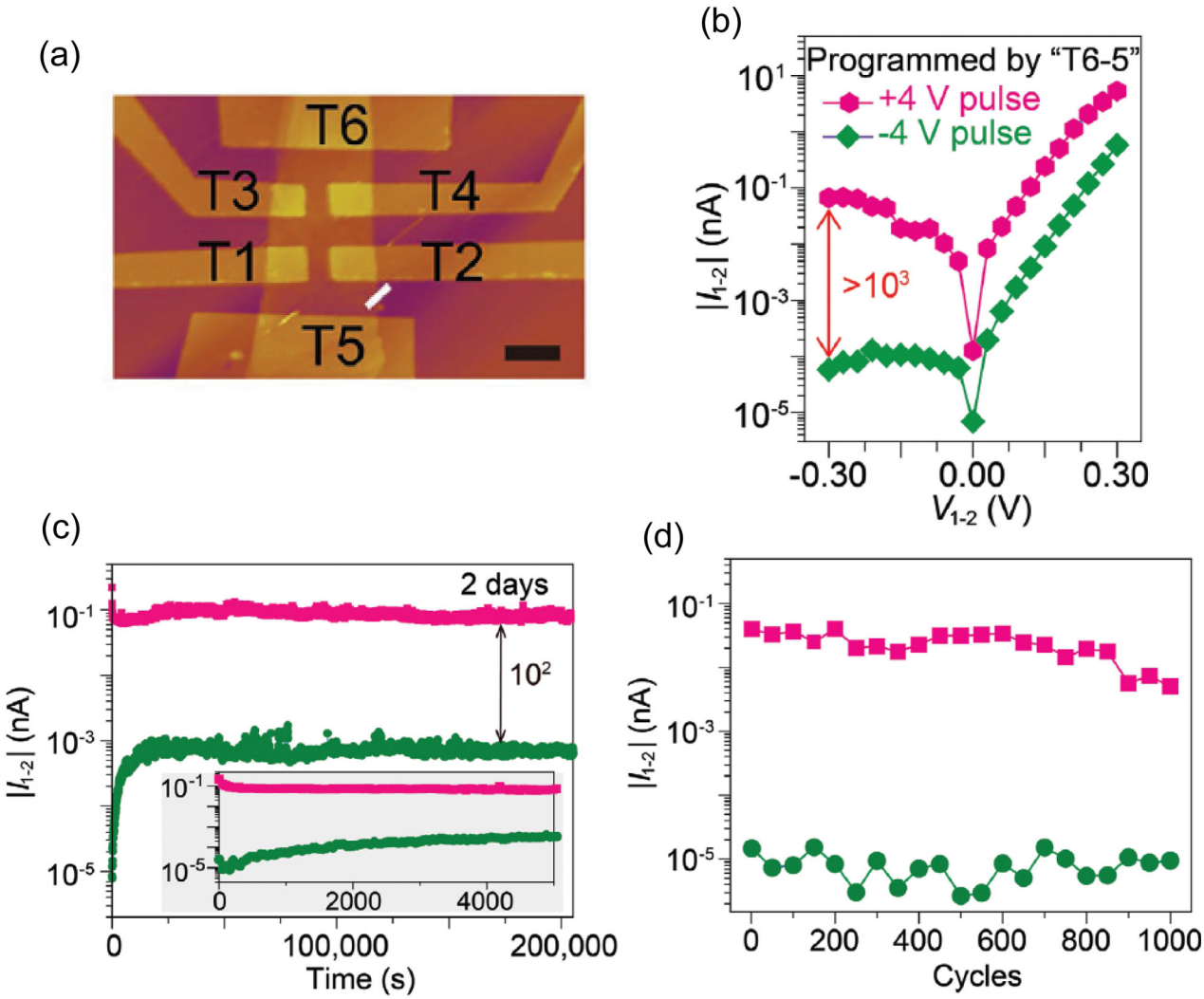

FIG. 5. α-In_2Se_3 memristor characterization and performance. (a) AFM topography image of the α-In_2Se_3 memristor. (b) Switching effect in the drain-source current of terminals 1–2 after applying 4 V programming pulse with 2 s duration to terminals 5–6. Terminals are denoted in (a) as T1–T6. This shows that a high-current (pink) and low-current (green) can be achieved through lateral poling at T5–T6. (c) and (d) Retention and cycle performance of the α-In_2Se_3 memristors high- and low-current states. Reproduced with permission from Xue *et al.*, Adv. Mater. **33**, 2008709 (2021). Copyright 2021 Author(s), licensed under a Creative Commons Attribution (CC BY) license.

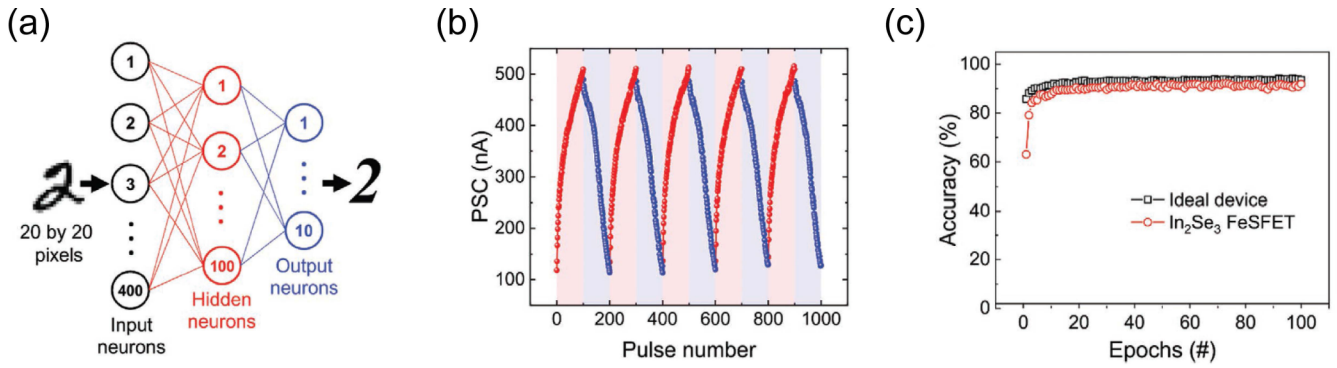

FIG. 6. Neuromorphic computation with α-In_2Se_3-based memristor devices. (a) Schematic representation of the neural network simulated, depicting three layers with 400 input neurons, 100 hidden neuron, and 10 output neurons, respectively. (b) Artificial-synapse operation of α-In_2Se_3 memristor devices showing both long-term potentiation (LTP) (red) and long-term depression (LTD) (blue) in the postsynaptic current output (PSC). In this operation, the back-gate acts as the presynaptic input and source electrode acts as the postsynaptic output. (c) Recognition accuracy of α-In_2Se_3 devices showing similar performance to an ideal neuromorphic computing device. Reproduced with permission from Wang *et al.,* Adv. Funct. Mater. **30**, 2004609 (2020). Copyright 2020 John Wiley & Sons.

multi-directional control of ferroelectric polarizations and channel conductivity through an OOP or IP electric field is possible, providing flexibility in device design and integration. A recent study (Fig. 5; reproduced from Ref. 12) demonstrated α-In_2Se_3-based memristors with a large on/off ratio of $>10^3$, two-second long write times, and retention time of days.[12] Another example[47] demonstrating neuromorphic computing is shown in Fig. 6 (reproduced from Ref. 47). In addition, a recent report (Fig. 7; reproduced from Ref. 48) implementing CIPS in a ferroelectric tunneling junction (FTJ) heterostructure device demonstrated impressive memristive properties with a large tunneling electroresistance (TER) of $>10^7$ and ~3 h long retention times,[48] thus superseding the TER that has been achieved with ABO_3-type perovskites and binary oxides. Besides the electric field control of memristor behaviors, recent studies reported that optical illuminations can also be used to set the device conductivity through light-ferroelectric interactions,[11,49,50] and the possibility of realizing photonic synapses was proposed.

III. OPEN QUESTIONS AND OPPORTUNITIES FOR FURTHER RESEARCH

While significant progress and milestones have been continuously accomplished for vdW ferroelectric device technologies, we believe that there are several aspects that warrant further investigations but have received less attention. Addressing these issues could provide a fundamental basis to guide the device development efforts and could also lead to new directions.

First of all, it remains an important open question as to the underlying mechanisms of memristive behaviors in α-In_2Se_3 devices. Our initial study[6] has suggested that energy barriers between ferroelectric domains play a significant role in controlling the device conductivity. On the other hand, the nature of ferroelectric-metal contacts (i.e., Schottky vs Ohmic), which depends on the ferroelectric polarization state, has been shown to be a significant factor as well.[51] Therefore, further studies are necessary to evaluate the relative

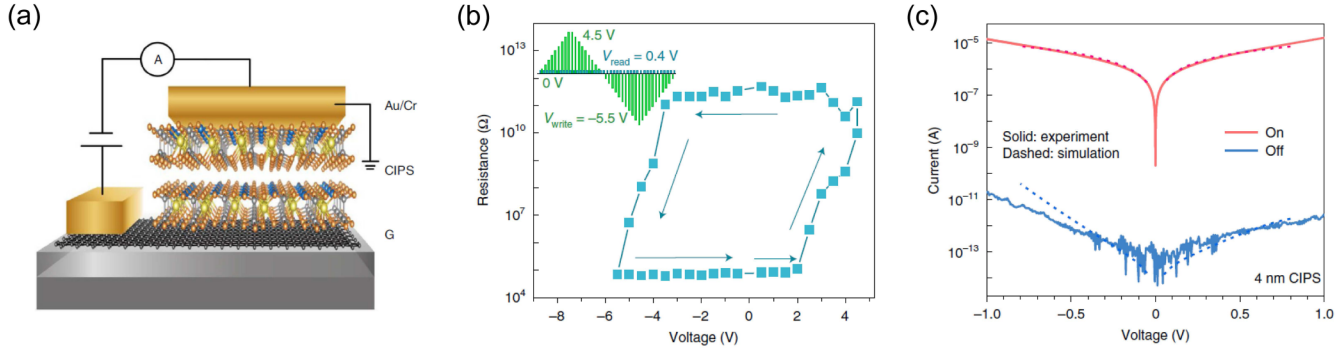

FIG. 7. Cr/CIPS/Gr FTJ heterostructure characterization and performance. (a) Schematic of the device. (b) Resistance tunability of FTJ as a function of the applied pulse voltages, with the inset showing the sequence of applied pulse voltages. (c) Current–voltage characteristics of FTJ after the device was programmed into the on and off states, demonstrating that a TER of $>10^7$ can be achieved. It should be noted that the on and off states were programmed by 4.5 and −5.5 V, respectively. Reproduced with permission from Wu *et al.*, Nat. Electron. **3**, 466 (2020). Copyright 2020 Springer Nature.

significance of these two effects, which will inform the current efforts to further optimize memristor performance.

The domain walls might also play an important role. In particular, memristive switching seems to be correlated with the evolution of domain configurations in the multi-domain state, which inherently involves changes to the domain wall patterns. With the existence of the in-plane component of ferroelectric polarizations, these domain walls can be positively or negatively charged, leading to electron accumulation or depletion. This in turn results in higher/lower electrical conductivity at the locations of the domain walls. Any changes in the domain wall configurations are, thus, likely to have a strong impact on the device properties. To the best of our knowledge, the domain wall properties in vdW ferroelectrics have not been explored and more studies in this direction are urgently needed. Understanding these properties can also help to realize the concept of "domain wall nanoelectronics,"[52,53] where the domain walls can function as the active elements in devices.

In addition, a fundamental knowledge of how light interacts with ferroelectric polarizations is central to advancing the concept of light-controlled ferroelectricity in vdW materials but is currently lacking in vdW ferroelectrics. Previous studies[11,49,50] have suggested that optical illumination can move the domain walls in α-In_2Se_3, leading to variations in device conductivity. Our study, on the other hand, indicates that optical illuminations may randomize polarization directions, resulting in the formation of disordered domains. As light-ferroelectric interaction can involve several different physical processes, such as coupling among photogenerated carriers, lattice phonons, surface-bound charges, and domain walls, careful and systematic studies are needed. Understanding these mechanisms can facilitate the development of optical writing of ferroelectric domains as a scalable approach to manufacture complex ferroelectric devices.

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AUTHOR DECLARATIONS

Conflict of Interest

Y.G. has an equity interest in Klar Scientific.

Author Contributions

Jacob Parker: Writing – original draft (lead). **Yi Gu:** Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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