An Integrated Quantum Spin Control System in 180nm CMOS

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Abstract— **Solid-state electron spins are key building blocks for emerging applications in quantum information science, including quantum computers, quantum communication links, and quantum sensors. However, solid-state spins are controlled using complex microwave pulse sequences, which are typically generated using benchtop electrical instruments. Integration of the required electronics will enable realization of a scalable low-power and compact optically addressable quantum system. Here, we report an integrated reconfigurable quantum control system, which is used to perform Rabi and Ramsey oscillation measurements for an NV center in diamond. The 180nm CMOS chip, fabricated within a footprint of 3.02mm², consumes 80 mW of power, and is capable of generating a tunable microwave signal from 1.6 GHz to 2.6 GHz modulated with a sequence of up to 4098 reconfigurable pulses with a pulse width adjustable from 10ns to 42ms and a pulse-to-pulse delay adjustable between 18 ns to 42m, at a resolution of 2.5 ns.**

Keywords—**CMOS integrated circuits, qubit, NV center, quantum computing, microwave.**

I. INTRODUCTION

To reach quantum supremacy, quantum computers need more than 50 logical qubits. For such quantum systems, rack-mounted microwave pulse generation and control systems with a high-power consumption are typically used for spin control and readout. To achieve scalability to a large number of qubits, such systems need to be integrated to significantly reduce the size and power consumption. There are different technologies to realize quantum computers [1]-[5]. One of the promising platforms to utilize the exponential power of qubits in room temperature is the nitrogen-vacancy (NV) center in diamond. Its high degree of stability, long coherence time, and unique magneto-optic properties among color centers make the NV center suitable for many quantum applications [6]. Current state-of-the-art architectures for NV center spin manipulation use rack-mounted systems [7]. This work presents a CMOS chip for microwave signal and pulse sequence generation and, as a proof of concept, demonstrates electron-spin resonance (ESR), Rabi oscillation, and Ramsey oscillation measurements at room temperature for a single NV center.

II. NV CENTER IN DIAMOND

The NV center in diamond is a fluorescent point defect, where one of the carbon atoms is replaced by a nitrogen atom, situated next to a vacancy [6] (Fig. 1(a)). Fig. 1(b) illustrates the NV energy level diagram. At room temperature, it can be described by three electronic levels, including the ground and excited states of the triplet manifold, and the metastable singlet state [6]. With no fields applied, the ground-state spin sublevel $m_s = 0$ and the degenerate $m_s = \pm1$ sublevels are separated by

resonance frequency near 2.87 GHz. Upon excitation to the excited state triplet, relaxation can either happen radiatively to the ground state triplet, or non-radiatively through the singlet. The $m_s = \pm1$ spin states are much more likely to go through this non-radiative decay, thus leading to spin-dependent photoluminescence.
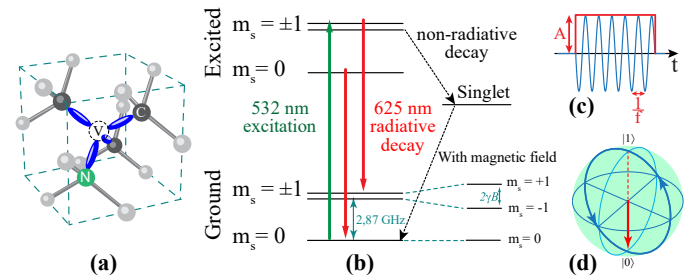

Fig. 1. (a) Molecular structure of the NV center and (b) its energy diagram. (c) A typical single truncated sinusoid (microwave pulse) for spin control. (d) The Bloch sphere representation of a two-level quantum mechanical system (qubit).

To access the spin sublevels for coherent quantum control, the $m_s = +1$ and -1 are isolated by applying an external DC magnetic field along the NV axis, which breaks the $m_s = \pm1$ degeneracy. The qubit can now be manipulated with microwave pulses to perform various operations or increase the coherence time. Here, a microwave pulse (shown in Fig. 1(c)) is defined as a truncated sinusoid with duration T, amplitude A, carrier frequency f, and the carrier phase, φ. Fig. 1(d) shows the Bloch sphere, which provides a visual picture of qubit operations. The south and north poles of the sphere indicate the pure $|0\rangle$ and $|1\rangle$ states, representing the $m_s = 0$ and $m_s = -1$ spin sublevels, respectively. The Bloch vector (red arrow) corresponds to the spin state of the system at a given time. Resonant microwave pulses rotate the vector along lines of longitude (blue curve), where the amount of rotation depends on the amplitude and duration of the microwave pulse. In this case, a rotation by 180^0 fully transfers the state from $|0\rangle$ to $|1\rangle$ and is referred to as a π-pulse. A rotation of 90^0, called a $\pi/2$-pulse, rotates the Bloch vector to the equator, resulting in a superposition state between $|0\rangle$ and $|1\rangle$. The phase of the microwave carrier, φ, alters the axis of rotation. Any experimental sequence can be constructed by sequential application of π and $\pi/2$ pulses with 4 different phases (*i.e.,* $\varphi = 0^o$, 90°, 180°, and 270°).

Fig. 2(a) shows an example microwave pulse sequence, where amplitude and duration of each pulse as well as the delay between the pulses is set to perform a certain spin control task. Fig. 2(b) shows a top-level block diagram of electro-optic spin control and read-out system for NV centers. Initialization and read-out are performed optically, and spin control is achieved

using microwave pulses. While the state-of-the-art NV center spin control typically employs rackmount equipment, in this work, the microwave pulse generation and control system is integrated.
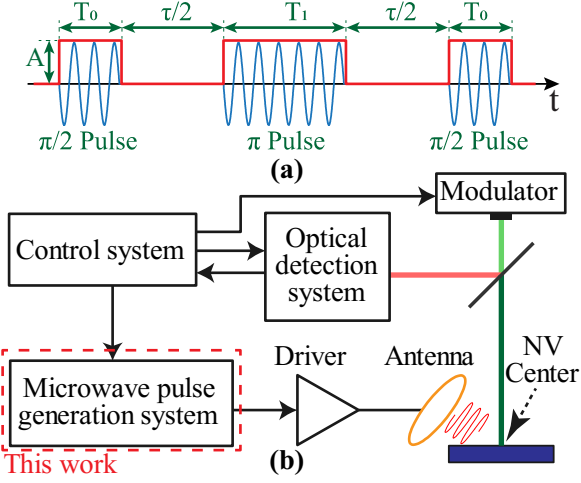

Fig. 2. (a) An example of microwave pulse sequence for spin control. (b) The top-level block diagram of typical electro-optic spin control and read-out system for NV centers.

III. SYSTEM ARCHITECTURE

Fig. 3 shows the block diagram of the integrated microwave pulse generation system, which consists of the RF generation system and the pulse sequence (envelope) generator. Within the RF generation system (Fig. 3), first, the phase and frequency of an LC-based VCO is locked to those of a stable off-chip frequency reference using a PLL. A poly-phase filter is used to generate differential in-phase and quadrature components from the PLL output (representing the $\varphi = 0º, 90º, 180º,$ and $270º$). A set of mixers within a switching network are placed after the poly-phase filter, which amplitude modulates the 4 outputs of the poly-phase filter with the generated digital pulse sequence and selects one of the outputs to realize truncated sinusoids (*i.e.* microwave pulses). The pulse sequence generator system, which produces the envelope for the train of truncated sinusoid pulses, consists of an LC-VCO (*i.e.* the clock generator), a state machine, a timer, and a memory unit that holds the features of each pulse and the delay between adjacent pulses, which are then used to generate the microwave pulse sequence.

Fig. 4(a) shows the diagram of the on-chip integer-N charge-pump PLL, where the VCO output is divided by a factor of 128 and is locked to the low frequency off-chip reference source. In this case, the synthesized microwave signal can be tuned from 1.6 GHz to 2.6 GHz (by tuning the off-chip low frequency reference) to cover the resonance frequency of the NV center upon various applied magnetic field bias levels. The schematic of the LC-VCO is shown in Fig. 4(b), where continuous tuning is realized using switchable capacitor bank together with varactor control. Fig. 4(c) shows the schematic of the differential cascode amplifiers placed after a 4-stage RC ploy-phase filter, which are used to compensate for the loss of the poly-phase filter. The amplifier input differential stage is biased through drain-gate feedback resistors. Fig. 4(d) shows the schematic of the balanced mixers shown in Fig. 3. Not that

the measured isolation of the on-chip switches, used to select the output phase, is about 60 dB.

Within the digital sequence generation system, a 400 MHz clock (generated using an LC-VCO oscillator) is distributed among 3 main blocks; the state machine, the timer, and the memory unit.
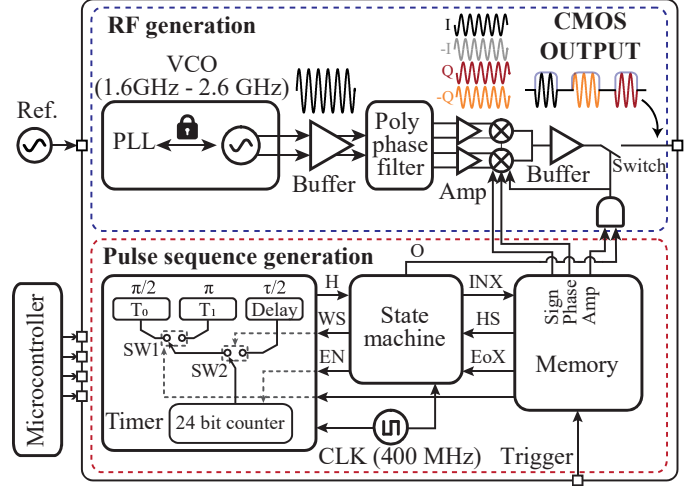

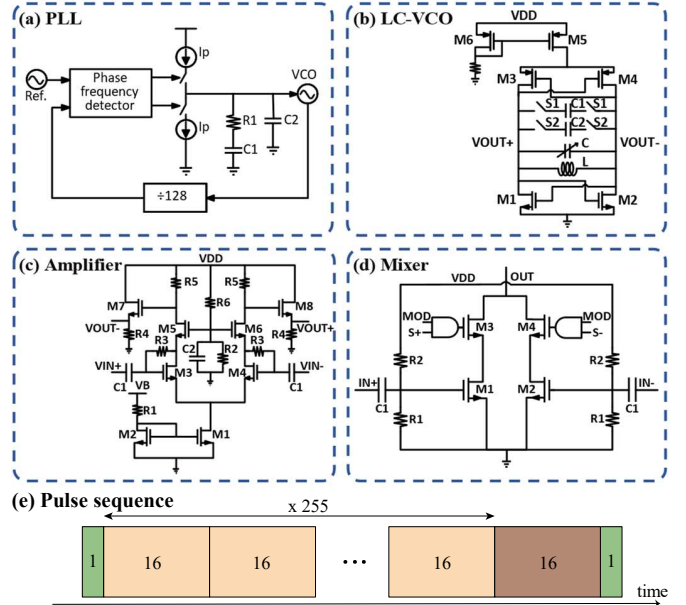Fig. 3. Detailed system architecture for the proposed CMOS chip.

Fig. 4. (a)-(d) Block diagram and detailed schematic of the main blocks of the proposed RF generation system. (e) The structure of the pulse sequence.

The timer cosists of a 24-bit counter and 3 registers holding the length of the π pulse, the length of the π/2 pulse, and the pulse-to-pulse delay. To generate the accurate legnth of each pulse or the delay differece between the pulses, the counter counts up to the value stored in the corresponding register. The minimum pulse width and delay are 10 ns and 18 ns, respectively, and the maximum for both is 42 ms. The pulse and delay length can be adjusted with a resolution of 2.5 ns. The state machine communicates with the timer and the memory unit and controls the state of the system. Each pulse is

represented with a 4-bit number stored in the memory unit, corresponding to the phase (2 bits for differential quadrature phases), amplitude, and pulse width.

(a)

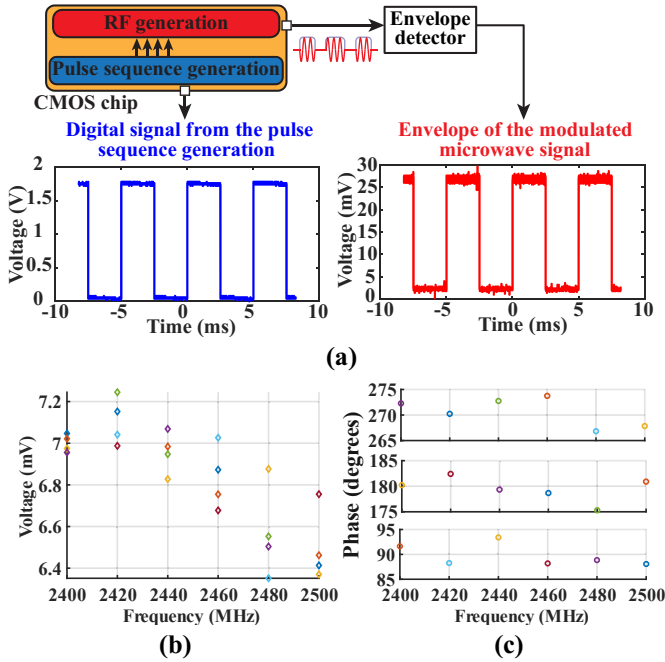

(b)   **(c)**

Fig. 5. (a) Measured digital signal from the pulse sequence and the detected envelope of the modulated microwave signal. (b) Measured amplitude variation and (c) quadrature phase variation of the microwave signal at different frequency points reference to the signal at $0°$.

For the digital sequence generation system in Fig. 3, initially, the system dwells at the idle state, where the timer is disabled and the output (O) is zero. In this case, the lengh of the π and $\pi/2$ and the pulse-to-pulse delay are written from the memory into the corresponding registers within the timer. When the state machine genrates the nth segment (*i.e.* pulse or delay) of the sequence, the memory index is set to the nth 4-bit data for which 3 bits (two bits for phase (φ), and a bit for amplitude) will directly control the RF generation system and the last bit sets the pulse width within the timer to T_o (for a $\pi/2$ pulse) or T_1 (for a π pulse) through switch SW1. At the end of this process, the HS signal is set to "1" and the state machine uses switch SW2 to select whether a pulse or a delay is generated (to be added to the sequence) and then enables the timer. This process starts with a single triger signal received from the control system of the quantum setup (in Fig. 2) and is repeated until the entire sequence is generated.

(a)   **(b)**

Fig. 6. (a) Die microphotograph. (b) The spin control measurement setup.

The state machine can generate sequences with up to 4098 pulses by generating the first pulse, 0 to 255 segments of reconfigurable 16 pulses, a segment of reconfigurable 0 to 16 pulses, and the end pulse (Fig. 4(e)).

Fig. 7. The Timing diagrams of the pulse sequence for ESR, Rabi, and Ramsey measurements.

IV. CMOS CHIP MEASUREMENTS

The CMOS chip is fabricated using TSMC's 180nm CMOS process technology. First, the microwave frequency synthesizer is measured. As the NV center is sensitive to the phase noise of the microwave signal, the LC-based VCO is locked to a clean off-chip reference. The phase noise of the locked VCO is below -63dBc/Hz at 10kHz offset, which is low enough for quantum measurements in this work.

Fig. 5(a) shows the measured digital signal from the pulse sequence generation and the envelope of the modulated microwave signal. The envelope of the RF signal was measured
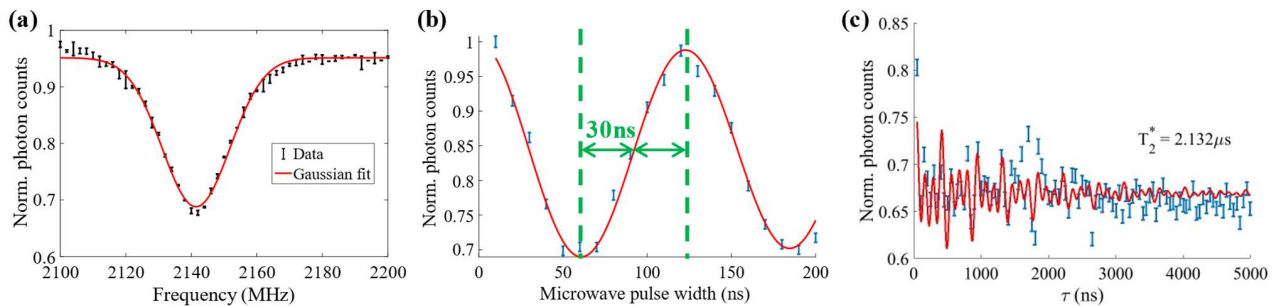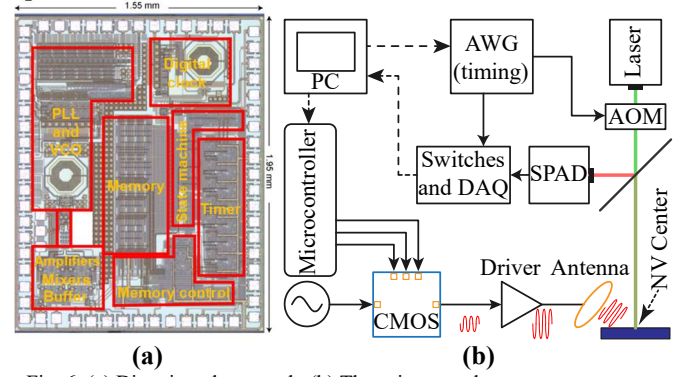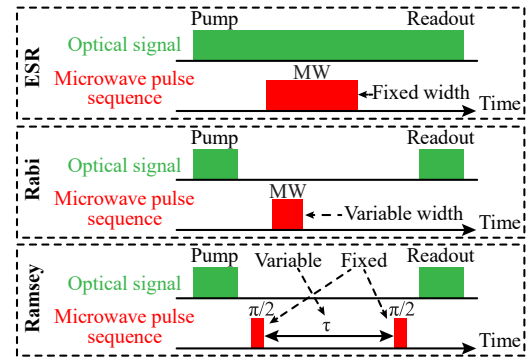

Fig. 8. (a) ESR measurement results. (b) Rabi oscillation results; the blue error bars are measured data, and the red line is a fit to that data to extract the width of a $\pi/2$ pulse. (c) Ramsey measurement results; the blue error bars represent measured data and the red curve represents a fit using the model presented in [5].

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with a Schottky diode at the chip output. The measured amplitude and phase variations of quadrature output signals are presented in Fig. 5(c) and Fig. 5(d), respectively, where a phase variation of under 5° is measured. Note that the amplitude variations can be compensated using amplifiers placed after the poly-phase filter. The microphotograph of the CMOS chip is shown in Fig. 6(a).

V. Measurements of Quantum System With CMOS Chip

The block diagram of the spin control measurement setup is shown in Fig. 6(b). The NV center is initialized and probed by a 532 nm continuous-wave laser, which is modulated by an acousto-optic modulator (AOM). The emitted photons are collected by a single-photon avalanche diode (SPAD) system and counted by a data-acquisition card (DAQ) through a switching network. The switching network and the AOM are modulated via an arbitrary waveform generator (AWG) to control the optical excitation and readout. The microwave pulses generated by the chip are used to coherently modulate the spin state of the NV center using an antenna fabricated near the NV center on the diamond chip. The CMOS chip is time-synchronized with the optical excitation and readout system. Fig. 7 shows the different pulse sequences used for electron spin resonance (ESR), Rabi oscillation, and Ramsey oscillation measurements, where green signals represent the optical excitation and readout signals and red signals represent the generated microwave pulse sequences. Fig. 8(a) shows the ESR measurement result of the NV center. In this experiment, the NV center is continuously pumped, and the microwave signal is periodically on for 10μs and off for 10μs. The frequency of the microwave signal is varied for each cycle. As the microwave frequency becomes in resonance with the spin state transition, a photoluminescence intensity reduction is observed. That is due to the non-radiative decay through the singlet state. The detected photoluminescence is shown in Fig. 8(a).

In the Rabi oscillation measurement results, the goal is to find the pulse width that rotates the Bloch vector to the equator (*i.e.* the $\pi/2$ pulse width). Here, a microwave signal tuned to 2140 MHz (ESR frequency) is applied. For each data point, the NV center was initialized into the $m_s = 0$ state before the microwave pulse is applied and was subsequently probed and projected onto the z-axis of the Bloch sphere. The microwave pulse width is changed after each measurement to observe Rabi oscillation. The optical readout results (the photon count) for different microwave pulse widths are shown in Fig. 8(b), from which the $\pi/2$-pulse width of about 30 ns can be calculated.

The CMOS chip was also used to perform the Ramsey measurements for the NV center. While the spin state of the NV center is initialized and measured the same way as in the Rabi experiment, in this experiment, the microwave frequency is detuned to about -5 MHz off the ESR frequency. The pulse sequence consists of two $\pi/2$-pulses (each 30 ns wide) separated by a delay of τ, which is varied from 10 ns to 5 μs. The first pulse rotates the spin from the ground state into the equatorial plane. During the free precession time τ, magnetic noise in the NV's local environment as well as the inhomogeneous broadening of the external magnetic field induces a phase

accumulation which translates the spin along a latitude line. After the delay τ, the spin is rotated with the second $\pi/2$ pulse. The photon count vs. delay is shown in Fig. 8(c). T_2^* is the time of exponential decay of the Bloch vector to 1/e of its initial amplitude. For measurements with the CMOS chip, T_2^* of 2.13 μs is measured, which is in close agreement with the results obtained using the benchtop system [7]. The performance of the implemented chip is compared with a few recently reported systems in Table 1.

Table 1. Comparison with the state-of-the-art spin control architectures.

	Nat Elect.[3]	Phys. Rev.[5]	This work
Operating temp.	300 K	300 K	300 K
Qubit platform	NV center	NV center	NV center
Qubit frequency	2.6-3.1 GHz	2-2.8 GHz	2-2.8 GHz
Technology node	65nm CMOS	Rack mount	180 nm CMOS
Waveform	Off-chip signal generation & modulation	AWG limited	Up to 4098 reconfigurable length pulses
Power	7.5mW*	>1W	Analog: 48 mW Digital: 32 mW
Chip area	0.04 mm²	-	3 mm²

*Does not include phase-locked loop and waveform control.

VI. Conclusion

A 180-nm CMOS integrated chip has been implemented and used at room temperature to demonstrate spin control of NV centers. The circuit generates reconfigurable microwave pulse sequences at 1.6 GHz–2.6 GHz. The minimum achievable pulse width and delay are 10 ns and 18 ns, respectively. Due to its reconfigurable memory structure, different pulse sequences were generated to perform ESR, Rabi, and Ramsey measurements on a single NV center. The T_2^* of 2.13 μs was measured. The CMOS chip was implemented within a footprint of 1.95x1.55 mm² and consumes 80 mW from a 1.8 V supply.

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