An Integrated Reconfigurable Spin Control System on 180 nm CMOS for Diamond NV Centers

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***Abstract*— Solid-state electron spins are key building blocks for emerging applications in quantum information science, including quantum computers, quantum communication links, and quantum sensors. These solid-state spins are mainly controlled using complex microwave pulse sequences, which are typically generated using benchtop electrical instruments. Integration of the required electronics will enable realization of a scalable low-power and compact optically addressable quantum system. Here, we report an integrated reconfigurable quantum control system, which is used to find electron-spin resonance (ESR) frequency and perform Rabi, Ramsey, and Hahn-echo measurements for a nitrogen-vacancy (NV) center spin qubit in diamond. The chip can be programmed to synthesize an RF signal tunable from 1.6 to 2.6 GHz, which is modulated with a sequence of up to 4098 reconfigurable pulses with a pulse width and pulse-to-pulse delay adjustable from 10 ns to 42 ms and 18 ns to 42 ms, respectively, at a resolution of 2.5 ns. The 180-nm CMOS chip is fabricated within a footprint of 3.02 mm^2 and has a power consumption of 80 mW.**

***Index Terms*— CMOS integrated circuits, microwave, nitrogen-vacancy (NV) center, quantum computing, qubit.**

I. Introduction

QUANTUM computers have the potential to solve specific sets of problems with significantly less computation cost than any other classical computer. The realization of this potential is being explored in a number of technologies [1] (see Fig. 1). These technologies include polarization encoding of photon [2], transmon qubits constructed from Josephson junctions [3], [4], electron spins in quantum dots [5], and others. Another promising technology to realize quantum bits (qubits) is utilizing electron and nuclear spins associated with nitrogen-vacancy (NV) centers in diamond [6], [7]. To reach quantum supremacy, quantum computers need more than 50 logical qubits [8]. For such quantum systems, rack-mounted equipment, and control systems with a high-power consumption are typically used for qubits control and readout.

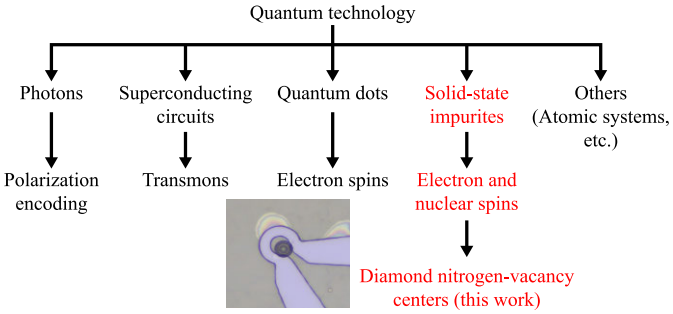

Fig. 1. Different physical implementations of quantum technology. Diamond NV centers are the quantum platform for the proposed work.

There are numerous works have been done toward the integration of qubits control and readout for different quantum platforms to realize quantum computers [9], [10], [11], [12]. Most of these platforms require cryogenic temperatures for proper operation. On the other hand, NV centers in diamonds can operate as qubit at room temperature. Its high degree of stability, long coherence time, and unique magneto-optic properties among color centers make the NV center suitable for many quantum applications [13]. Current state-of-the-art architectures for NV center spin manipulation use rack-mounted systems [14]. To achieve scalability to a large number of qubits, such systems should be integrated to significantly reduce the size and power consumption.

Here, we report the implementation of a CMOS chip that can be programmed to generate and amplify a train of synchronous tunable truncated sinusoid pulses (i.e., microwave pulses) with adjustable frequency, amplitude, phase, width, and pulse-to-pulse delay, which is then used for spin control. As a proof of concept, the implemented chip is used, at room temperature, to accurately measure the electron-spin resonance (ESR) frequency, Rabi oscillation, Ramsey oscillation, and Hahn-echo response for a single NV center in diamond. The frequency of the chip output signal is tunable from 1.6 to 2.6 GHz. This signal is modulated with a sequence of up to 4098 reconfigurable pulses generated on-chip. The minimum pulse width and pulse-to-pulse delay are 10 and 18 ns, respectively. The maximum pulse width and pulse-to-pulse delay are both 42 ms. Compared to the previous work [15], here we demonstrate new Ramsey oscillation measurements with an improved T_2^* of 2.16 μs and Hahn-echo response with revival periods of 6.92 μs with a CMOS chip. To the

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best of our knowledge, this is the first Hahn-echo refocusing of the NV center electron spin measured using a CMOS chip. Moreover, the chip-to-chip performance variation through the ESR contrast measurements is presented and analyzed. The mean ESR contrast, obtained with five different chips from the same design, equals 0.24. The pulse sequence generation is also discussed in detail.

This article is organized as follows. Section II summarizes the characteristics and unique properties of the NV center in diamonds. Section III describes the system architecture of the proposed CMOS chip for spin manipulation of the NV center. Section IV presents the chip characteristics. Section V demonstrates different quantum measurements with the CMOS chip. Section VI discusses the chip-to-chip performance variation through the ESR contrast (as a system-level SNR metric) measurements for different chips. Section VII concludes with an outlook on getting other advanced quantum measurements.

II. NV Center in Diamond

Crystal defects in diamonds are famously stable and have unique optical properties. One of these defects is the NV center, which is a fluorescent point defect. In this point defect in a diamond, one of the carbon atoms is replaced by a nitrogen atom, situated next to a vacancy [16] [see Fig. 2(a)]. The NV energy level diagram is shown in Fig. 2(b), which at room temperature, can be described by three electronic levels, including the ground and excited states of the triplet manifold, and the metastable singlet states [16]. With no fields applied, the ground-state spin sublevel $m_s = 0$ and the degenerate $m_s = \pm 1$ sublevels are separated by resonance frequency near 2.87 GHz. Upon excitation to the excited state triplet, relaxation can either happen radiatively to the ground state triplet, or non-radiatively through the singlet states. When $m_s = \pm 1$ spin states go through this non-radiative decay, the photoluminescence decreases. This highly probable non-radiative decay leads to spin-dependent photoluminescence. The statistical probability of decaying non-radiatively through a metastable state is 30% [17]. This defines the maximum contrast level that can be achieved for a continuous wave excitation. Achieving the maximum contrast level increases the signal to noise level of the system. To realize a qubit from an electron spin, two energy levels are required. By applying an external dc magnetic field along the NV axis, the $m_s = +1$ and -1 states can be isolated which breaks the $m_s = \pm 1$ degeneracy. This is known as Zeeman splitting effect [18]. Fig. 2(c) shows this effect, where the resonance response of the NV center splits when an external field is applied. This effect allows access to the spin sublevels for coherent quantum control. After separation of the resonances of the $m_s = +1$ and -1 spin sublevels, the qubit can now be manipulated with microwave pulses to perform different operations (e.g., to increase the coherence time of the qubit spin). Here, a microwave pulse [shown in Fig. 2(d)] is defined as a truncated sinusoid with duration T, amplitude A, carrier frequency f, and the carrier phase, φ. Fig. 2(e) shows the Bloch sphere, which provides a visual representation of qubit operations. The south and north poles of the sphere

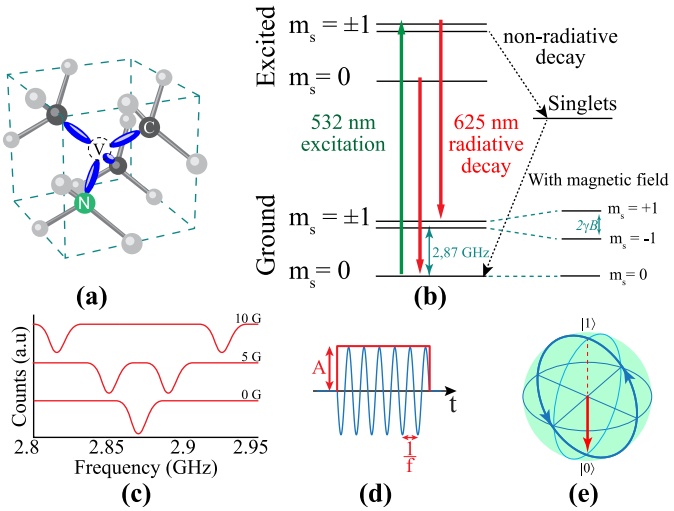

Fig. 2. (a) Molecular structure of the NV center and (b) its energy diagram. (c) Zeeman splitting demonstration [16] under an external magnetic field. (d) Typical single truncated sinusoid (microwave pulse) for spin control. (e) Bloch sphere representation of a two-level quantum mechanical system (qubit).

indicate the pure $|0\rangle$ and $|1\rangle$ states, representing the $m_s = 0$ and -1 spin sublevels, respectively. The Bloch vector (red arrow) corresponds to the spin state of the system at a given time. Resonant microwave pulses rotate the vector around a horizontal axis along lines of longitude (blue curve), where the amount of rotation depends on the amplitude and duration of the microwave pulse. Assuming the initial state to be in the north pole, here, a rotation of 90° transfers the spin vector to equator, where the spin takes a superposition between $|0\rangle$ and $|1\rangle$. A rotation of 180° fully transfers the spin vector from north pole to south pole. The rotations by 90° and 180° are referred to as $\pi/2$ and π-pulses, respectively. Fluctuations in the oscillator frequency or phase leads to fluctuations of the Bloch sphere axes [19]. Therefore, the horizontal axis of rotation depends on the phase of the microwave carrier, φ. The desired spin control sequence can be constructed by sequential application of π and $\pi/2$ pulses with four different phases (i.e., $\varphi = 0^o$, 90^o, 180^o, and 270^o) of the microwave signal.

Fig. 3(a) shows an example microwave pulse sequence, where the amplitude and duration of each pulse as well as the delay between the pulses is set to perform a certain spin control task. Assuming the initial state of the spin in the north pole of the Bloch sphere, the $\pi/2$-pulse rotates the Bloch vector to the equator along the y-axis. For a delay time of $\tau/2$, the spin de-phases by a certain amount. The second π-pulse rotates the Bloch vector to the opposite side of the equator along the y-axis. In a second delay time of $\tau/2$, the spin de-phases by the same amount and in the same direction. The last $\pi/2$-pulse rotates the Bloch vector to the north pole (i.e., the initial state). Here, any uncertainty in the pulses or delays will decohere the spin of the electron.

Fig. 3(b) shows a top-level block diagram of the electro-optic spin control and read-out system for NV centers. Initialization and read-out are performed optically, and spin control is achieved using microwave pulses. While the state-of-the-art NV center spin control typically employs rackmount

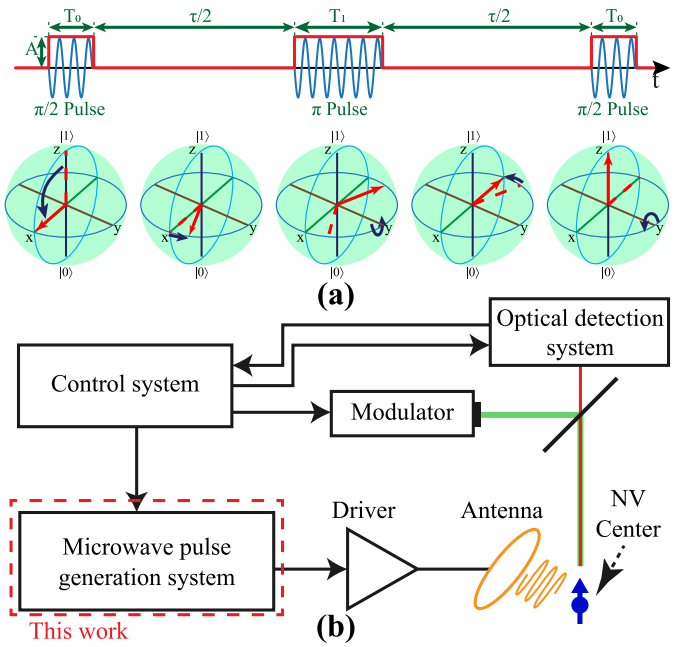

Fig. 3. (a) Example of microwave pulse sequence for spin control. (b) Top-level block diagram of typical electro-optic spin control and read-out system for NV centers.

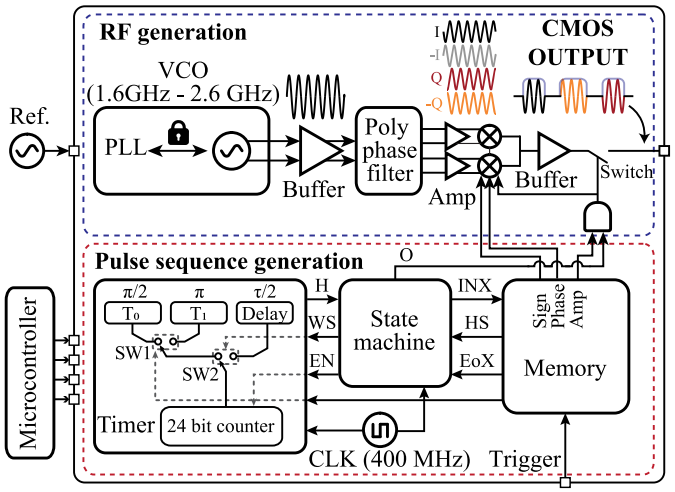

Fig. 4. Detailed system architecture for the proposed CMOS chip.

equipment, in this work, as a step toward the implementation of large-scale qubit systems, the microwave pulse generation, and control system is integrated.

III. System Architecture

Fig. 4 shows the block diagram of the implemented CMOS chip. The chip consists of two main parts; the RF generation system and the pulse sequence (envelope) generator, where the synthesized RF signal is multiplied by the digital pulse sequence to generate the spin control signal. In the first part, the RF generation system (see Fig. 4), a carrier signal is synthesized by phase and frequency locking of an *LC*-based VCO to those of a stable off-chip frequency reference using a PLL. The VCO output is followed by a buffer and a poly-phase filter. The poly-phase filter is used to generate differential in-phase and quadrature components from the PLL output (representing the $\varphi = 0^o$, 90^o, 180^o, and 270^o). The poly-phase filter is followed by variable gain amplifiers and two frequency mixers. These mixers amplitude modulate the four outputs of the poly-phase filter with the generated digital pulse sequence and select one of the outputs to realize the output truncated sinusoids (i.e., microwave pulses). In the second part, the pulse sequence generator system, the envelope for the train of truncated sinusoid pulses is generated. The envelope is controlled by a state machine, which works on the falling edge of the clock generated using a separate integrated 400 MHz *LC*-VCO. A timer and a memory unit hold the features of each pulse and the delay between adjacent pulses, which are then used to generate the microwave pulse sequence.

The 400 MHz clock, within the digital sequence generation system, is distributed to the state machine and the timer. To fine control the lengths of the pulses and delays between them, the timer uses a 24-bit counter and three registers. Registers hold the length of the π pulse, the length of the $\pi/2$ pulse, and the pulse-to-pulse delay. These registers are used to compare their stored values with the value from the counter. Everytime counter counts up and reaches a threshold, state machine gets triggered. This process is repeated to generate the accurate length of each pulse or the delay difference between the pulses. The minimum pulse width and delay are 10 and 18 ns, respectively, and the maximum for both is 42 ms. The pulse and delay lengths can be adjusted with a resolution of 2.5 ns. Besides the state machine, the memory unit also controls the state of the system. The memory unit stores a 4-bit information for individual pulses. The stored information corresponds to the phase (2 bits for differential quadrature phases), amplitude (0 and 1), and pulse width select (π- or $\pi/2$-pulse length) for each pulse. The detailed description of RF generation system and pulse sequence generation system are discussed next.

A. RF Generation

To efficiently drive the NV center and maximize its photoluminescence contrast, it is required to have a clean and stable microwave source, which is realized by phase and frequency locking of an *LC*-VCO to an off-chip reference. Since, in general, the phase noise of the oscillator affects the coherence of the NV center [19], it is desired to minimize the phase noise of the CMOS oscillator in order to increase the coherence time of the NV center. The diagram of the on-chip microwave source is shown in Fig. 5(a), wherein an integer-N charge-pump PLL the VCO output is divided by a factor of 128 and is locked to the low-frequency off-chip reference source. In this case, the synthesized microwave signal can be tuned from 1.6 to 2.6 GHz (by tuning the off-chip low frequency reference) to cover the resonance frequency of the NV center upon various applied dc magnetic field strengths. The schematic of the *LC*-VCO is shown in Fig. 5(b), where continuous tuning is realized using switchable capacitor bank together with continuous varactor control. The phase frequency detector is implemented using two edge-triggered, resettable *D* flipflops with their *D* inputs tied to a logical ONE

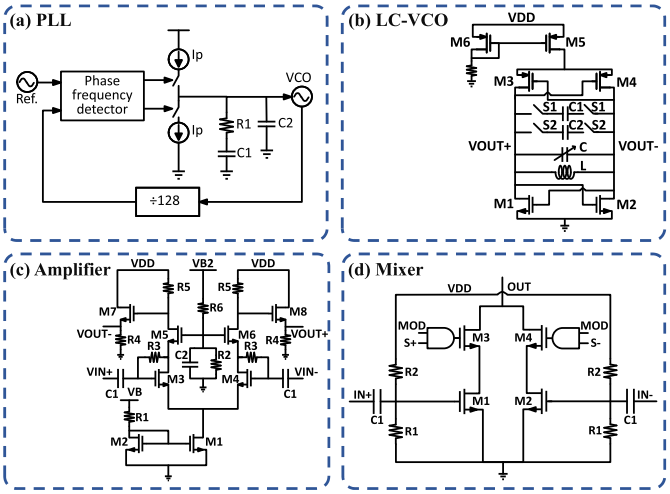

Fig. 5. (a)–(d) Block diagram and detailed schematic of the main blocks of the proposed RF generation system.

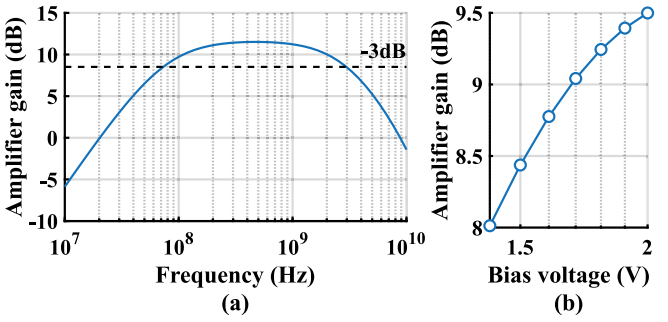

Fig. 6. (a) Simulated frequency response of the variable gain amplifier and (b) amplifier gain versus current mirror's bias voltage (VB) at 2.5 GHz.

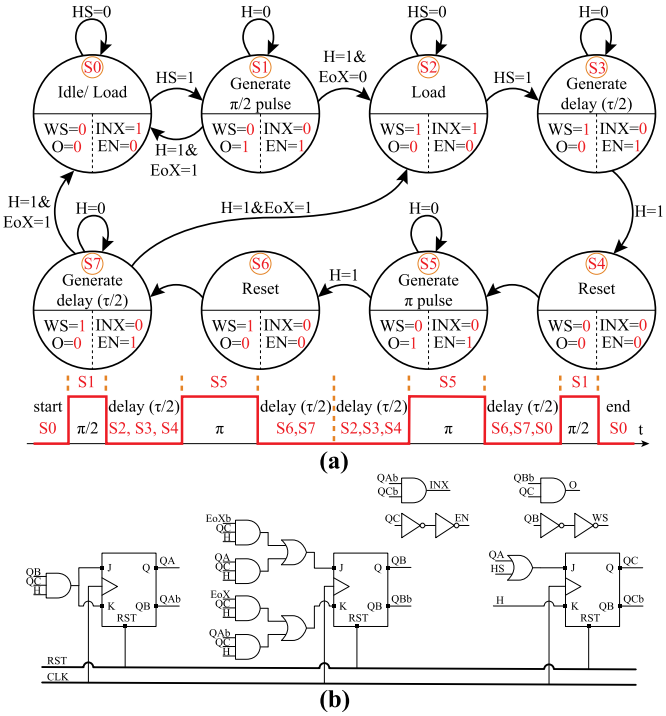

Fig. 7. (a) State diagram for a Moore machine to generate train of pulses with a delay between them. (b) Circuit implementation of the proposed state machine.

and follows the design in [20]. Fig. 5(c) shows the schematic of the differential cascode amplifiers placed after a four-stage *RC* ploy-phase filter, which are used to compensate for the loss of the poly-phase filter. The amplifier input differential stage is biased through drain-gate feedback resistors. A bias point, VB, changes the biasing of a current mirror, which subsequently affects the gain of the amplifier. Fig. 5(d) shows the schematic of the balanced mixers shown in Fig. 4. The amplitude and phase imbalance of the carrier signal of the I/Q signals contribute to the pulse errors which affect the qubit coherence. The benchtop system uses calibrated signals with minimum mismatches. For the proposed design the amplitude imbalance can be adjusted with the variable gain amplifiers, whereas the phase mismatch is inevitable and indirectly affects the SNR and can be calculated from the Bloch sphere representation (for example, 5° of phase mismatch between I/Q signals is equivalent to less than 3% of the phase accumulation error in case of a π spin precession). This effect should be accounted for at a data acquisition stage. Symmetrical layout improves the mismatch and decreases the pulse errors. Simulated frequency response of the variable gain amplifier is presented in Fig. 6(a). The maximum gain of the amplifier is 12 dB and the bandwidth is about 2.9 GHz. Fig. 6(b) shows that amplifier gain can be adjusted more than 1.5 dB by changing the bias voltage of the current mirror device from 1.4 to 2 V at 2.5 GHz, which can be used to partially compensate for the I/Q amplitude mismatch.

B. Pulse Sequence Generation

The pulse sequence generation is designed based on a Moore machine [21], where the output values are determined by the present state and the next state is defined based on the present state and the current inputs. The state of the digital pulse sequence generation system is set by the state machine, which communicates with the timer and memory unit (see Fig. 4). The state machine receives and processes the Hit (H) signal from the timer and Handshake (HS) and End of Experiment (EoX) signals from the memory and generates and sends Word Select (WS) and Enable (EN) signals to the timer, Index (INX) to the memory, and Output (O) modulation control signal to the switch in the RF generation system.

Fig. 7(a) depicts the state sequence within the state machine used to generate the shown digital pulse sequence ($\pi/2$, $\tau/2$, π, τ, π, $\tau/2$, $\pi/2$). In this case, the state machine uses eight different states (S0–S7) with three inputs (HS, H, EoX) and four outputs (WS, EN, INX, O). State S0 is the idle state where the state machine waits for the first HS signal in order to start the sequence. The first HS signal is generated by the trigger signal provided from the off-chip microcontroller (while the subsequent HS signals are generated by the memory unit according to the pattern of the desired pulse sequence). The trigger signal is required to synchronize the pulse sequences with optical excitation. With the first HS signal, the state machine goes to state S1 and enables the 24-bit counter (within the timer) to generate a $\pi/2$-pulse. Once this timer hits the pre-set value of T_0, H signal becomes active and the state

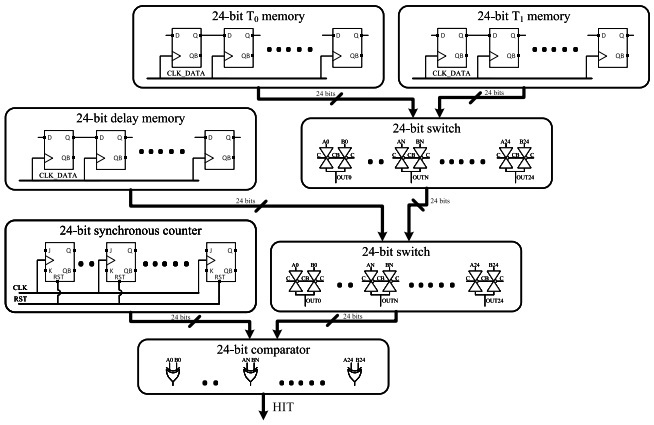

Fig. 8. Circuit implementation of the timer system for digital pulse sequence generation.

machine goes to the next state, S2. In this state, the state machine resets the timer, switches to the different WS and waits for the next HS signal. The HS signal transits the state machine to the next state, S3. Here, the modulation signal O becomes low to generate the delay between the pulses. Once the timer reaches the delay pre-set value (in this case $\tau/2$), H signal is set to high, and the state machine goes to state S4. In this state, the state machine resets the timer and advances to the next state, S5. At state S5, the state machine generates π-pulse by setting the signal O to high and enabling the 24-bit timer within the counter. After the counter within the timer reaches the pre-set value of T_1, H signal becomes active and the state machine advances to the next state, S6. In this state, the state machine resets the timer and advances to state S7. Similar to state S3, here the state machine generates the delay between the pulses. Depending on the input value of EoX, the state machine can either go to state S2, entering the finite loop (creating a series of π pulse - τ delay segments), or transit to state S0. From state S0, the state machine transits to state S1 to generate the last $\pi/2$-pulse and returns to state S0, waiting for the next hardware trigger to arrive.

Fig. 7(b) shows the circuit implementation of the proposed state machine. The designed state machine consists of three pulse-triggered JK flip-flops synchronized with the rising edge of the CLK signal. Each JK flip-flop receives matching inputs from other states and three inputs from the timer and memory units. The state machine outputs four signals, some of the signals are buffered to decrease loading to maintain the synchronized transitions of output signals.

The timer unit consists of a counter, register, switch, and comparator blocks (see Fig. 8). There are three 24-bit memory blocks for setting the pulse widths (T_0 and T_1) and the pulse-to-pulse delay. These blocks are using a cascade of *D* flip-flops serving as on-chip memory. All the registers are operating with a shared clock signal. A 24-bit switch array is used to select between the two memory units containing the duration of different pulses (i.e., T_0 and T_1). Similarly, a 24-bit switch array is used to switch between the 24-bit pulse duration and 24-bit delay according to the pattern of the digital pulse sequence. The switch arrays are based on transmission gate configuration for instantaneous data transmission. A 24-bit synchronous counter is utilized, where the count is compared to the selected memory unit using a 24-bit comparator to generate the digital Hit (H) signal, advancing the state of the state-machine. The comparator is based on XOR logic.

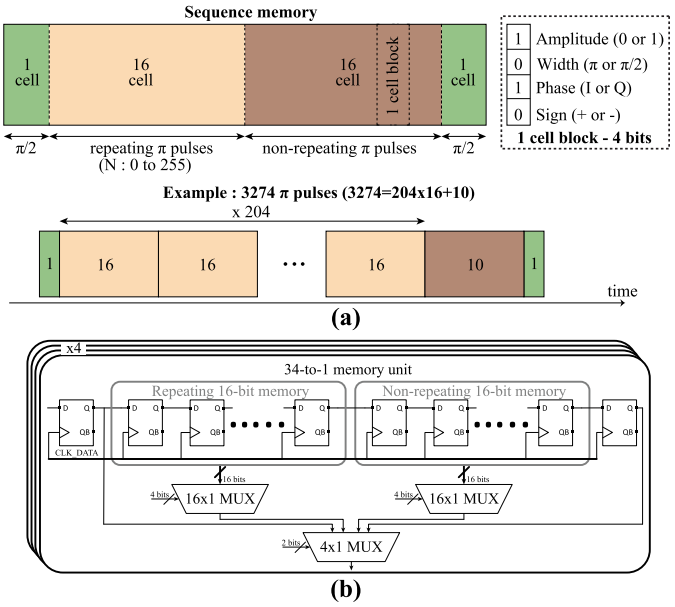

Fig. 9. (a) Block diagram of the memory unit. (b) Circuit implementation of the one-bit pulse information.

The digital pulse sequence generation system has a memory block that sets the amplitude, phase, and sign of each pulse, as well as the pulse width. This memory block can reconfigure 34 independent pulses. To efficiently use these reconfigurable pulses in quantum experiments, the memory block is divided into four segments [green and brown parts in Fig. 9(a)]. The first and the last segments [green cells in Fig. 9(a)] set the features of the first and last pulses, respectively. The second segment of the memory block [light brown in Fig. 9(a)], with 16 cells, can be repeated up to 255×. The third segment of the memory block [dark brown in Fig. 9(a)] consists of 16 cells. This segment is non-repeating. For example, as shown in the Fig. 9(a), in order to synthesize 3274 π-pulses, the repeating segment is played 204× followed by the last part of the sequence which is realized using ten cells of the non-repeating segment. Based on this architecture, the chip plays up to 4098 reconfigurable pulses for quantum spin control and manipulation.

The pulse sequence at any time is set by four control bits of amplitude (0, 1), width (π, $\pi/2$), phase (0, 90°), and sign ($+1$, -1). A 4×34 bit memory block is used to store these control bits. At each clock cycle, the memory block outputs four control bits. The memory block is implemented using cascaded *D* flip-flops with two 16-to-1 multiplexers and a 4-to-1 multiplexer [Fig. 9(b)]. The combination of two 16-to-1 and one 4-to-1 multiplexers is used to select one of the 34 bits from the memory unit for sequential pulse synthesis.

IV. CMOS Chip Measurements

The measurement setup for the CMOS chip characterization is shown in Fig. 10(a), which consists of a frequency

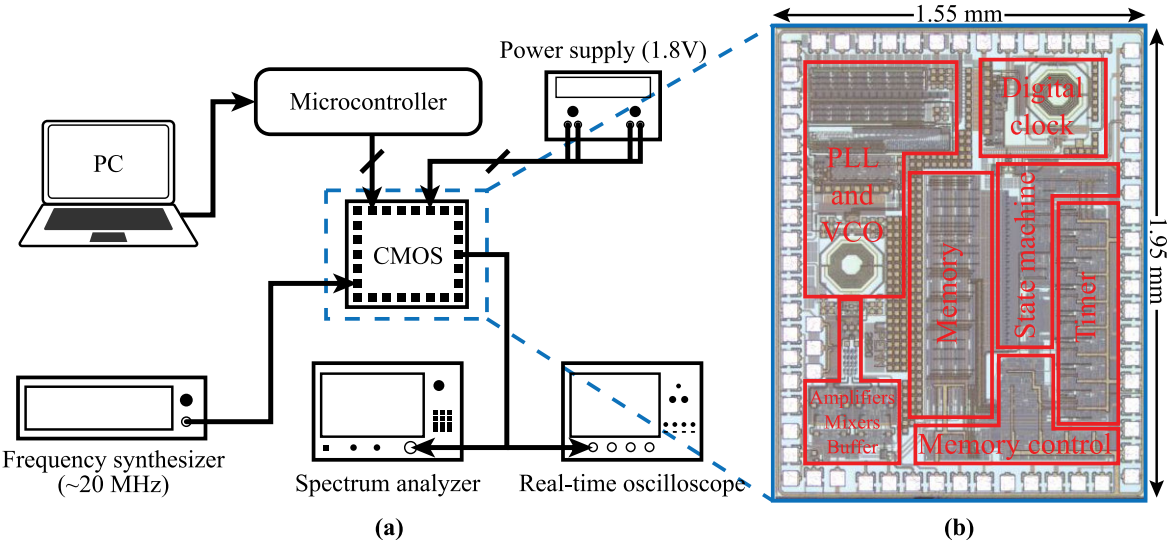

Fig. 10. (a) Block diagram of the CMOS chip measurement setup. (b) Die microphotograph of the implemented CMOS chip.

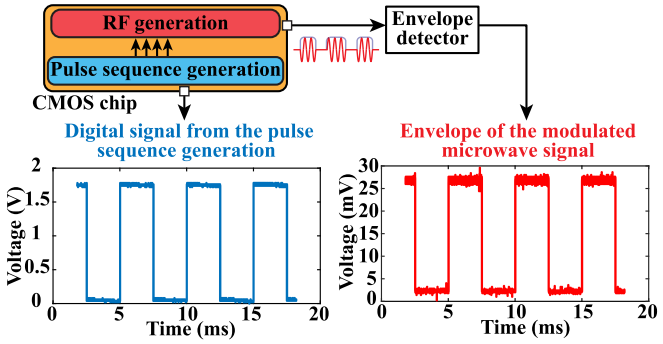

Fig. 11. Measured output of the digital pulse sequence generator and the detected envelope of the modulated RF signal (the microwave pulse sequence).

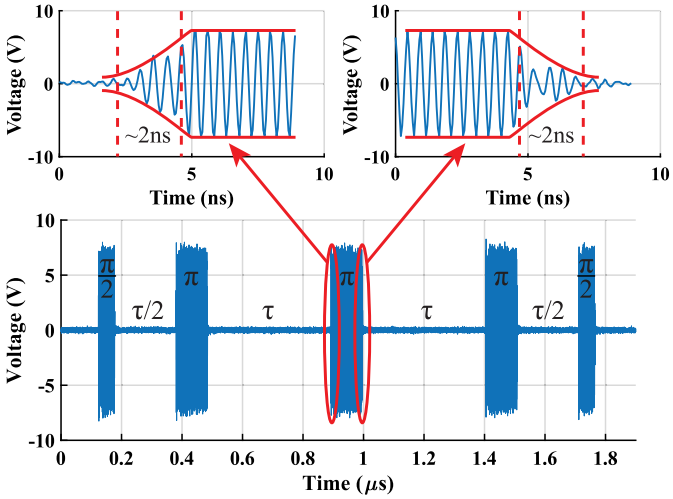

Fig. 12. Measured modulated signal at the output of the chip for a specific sequence with rise and fall time derivation.

synthesizer, serving as a reference for the on-chip PLL, a microcontroller for programming the chip, a power supply, and measurement instruments, including spectrum analyzer and real-time oscilloscope. The microphotograph of the implemented chip fabricated on the TSMC 180 nm CMOS process is shown in Fig. 10(b).

The phase noise of the microwave pulse sequence causes the dephasing of the coherent states of spins [19]. Therefore, in this design, the *LC*-based VCO is phase locked to a clean off-chip reference. The phase noise of the locked VCO is below −63 dBc/Hz at a 10 kHz offset, which proves to be sufficient for coherent control of the NV spin.

The measured output of the digital pulse sequence generator and the envelope of the modulated RF signal (the microwave pulse sequence) are shown in Fig. 11. The envelope of the modulated RF signal was detected using a Schottky diode placed at the chip output. The two signals have the same time length characteristics, which is in agreement with the pre-programmed values confirming the functionality of the digital sequence generator.

The induced phase of the electron spin is directly proportional to the external magnetic field component and surrounding magnetic noise [18]. It is important to keep the external magnetic field to a minimum to decrease its effect during the free precession time. The measured ratio of on and off microwave signals at the chip output is more than 60 dB. This provides a high enough extinction ratio for modulated signals.

Fig. 12 shows the measured modulated signal at the output of the chip for a specific pre-programmed sequence, which consists of two $\pi/2$-pulses at the beginning and end of the sequence, and three π-pulses between the two $\pi/2$-pulses. The delay between the first and second pulses, as well as, between the pre-last and last pulses is $\tau/2$. The delay between other pulses is τ. In this pre-programmed sequence, the widths of the $\pi/2$ and π pulses correspond to 100 and 200 ns, respectively. The delay of $\tau/2$ is equal to 200 ns. Fig. 12 shows the measured chip output waveform when the chip is programmed for this specific sequence. Here, the rise and fall time of about 2 ns is measured. The rise and fall time can change the amount of spin rotation and if unaccounted for, contribute to pulse errors.

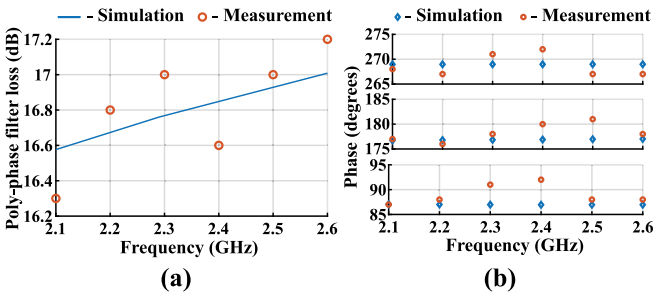

Fig. 13. Simulated and measured poly-phase filter (a) loss and (b) phase variations at different frequencies, referred to the signal at 0°.

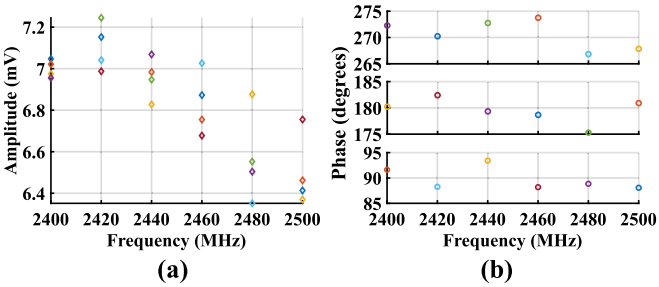

Fig. 14. (a) Measured amplitude variation and (b) quadrature phase variation of the microwave signal at different frequencies, referenced to the signal at 0°.

The resonance frequency of the NV center depends on the magnetic dc field; thus the chip was designed to operate for a wide frequency range to accommodate different magnetic field levels. In order to have quadrature signals with enough bandwidth at the output (from 1.6 to 2.6 GHz) a four-stage poly-phase filter was used. Fig. 13 shows the simulated and measured loss and phase variations of the proposed poly-phase filter. The average loss is about 17 dB and the phase variation is less than 3° around the desired value. Using less number of stages for the poly-phase filter decreases the total loss and narrows the bandwidth of quadrature signals.

The measured amplitude and phase variations of quadrature output signals are presented in Fig. 14(a) and (b), respectively, where a phase variation of under 5° is measured. Note that the amplitude variations can be compensated using tunable amplifiers placed after the poly-phase filter.

Another important parameter for the spin control of an NV center is the spurious free dynamic range (SFDR) of the microwave control signal around the spin resonance frequency of the NV center. Since the phase noise is related to the power density spectrum, any spurious tone negatively affects the spin coherence. Fig. 15 shows the measured power spectrum of the chip output signal used to excite and control the NV center, where an SFDR of more than 40 dB is achieved. The minimum SFDR depends on the shape of the spurious tone and its offset frequency. For our case, SFDR of 40 dB gives a coherence time of more than 25 μs, which is adequate to achieve the desired system performance in this work.

V. Quantum Measurements Using the CMOS Chip

The block diagram and photographs of the spin control measurement setup are shown in Fig. 16. The NV center is initialized and probed by a 532 nm continuous-wave laser, which

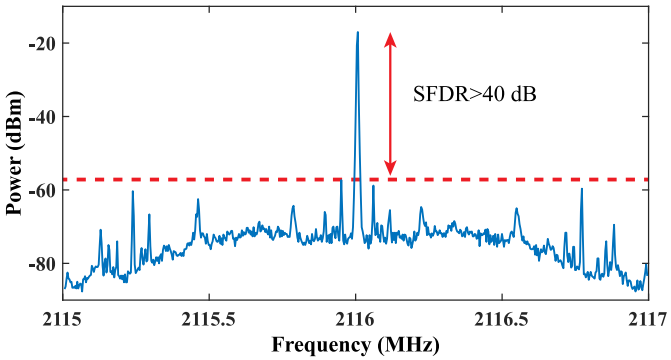

Fig. 15. Measured power spectrum of the chip output signal, where SFDR of more than 40 dB is achieved.

is modulated using an acousto-optic modulator (AOM). The emitted photons are collected by a single-photon avalanche diode (SPAD) system and counted using a data-acquisition card (DAQ) through a switching network. An arbitrary waveform generator (AWG) is used to control a switching network and modulate the 532 nm source using an AOM to control the optical excitation and readout. The resonances of the spin sublevels of the NV center are split by the magnetic field of a nearby permanent magnet. The microwave pulses generated by the chip are used to coherently modulate the spin state of the NV center using an antenna fabricated near the NV center on the diamond chip. The CMOS chip is time-synchronized with the optical excitation and readout system. This setup is used to perform ESR, Rabi oscillation, Ramsey oscillation, and Hahn-echo measurements.

A. ESR Measurements

Fig. 17(a) shows the pulse sequence used for ESR measurements, where the green signal represents the optical excitation and readout signals, and the red signal represents the microwave pulse sequence generated for spin control. In this case, the NV center is continuously pumped, and the microwave signal is periodically on for 10 μs and off for 10 μs. The frequency of the microwave signal is varied for each cycle. As the microwave frequency becomes in resonance with the spin state transition, a photoluminescence intensity reduction is observed. That is due to the non-radiative decay through the singlet state. The ESR measurements are performed for two chips of the same design. The detected photoluminescence is shown in Fig. 17(b) and (c) for chip 1 and chip 2, respectively. The measured resonance frequencies are different for two cases, due to a variation of the dc magnetic field strength around the NV center, which were successfully measured using the implemented chip.

B. Rabi Measurements

In the Rabi oscillation measurements, the goal is to find the pulse width that rotates the Bloch vector to the equator (i.e., the $\pi/2$ pulse width). Here, a microwave signal tuned to the ESR frequency (2140 MHz for chip 1 and 2116 MHz for chip 2) is applied. Fig. 18(a) shows the pulse sequence used for Rabi measurement, where green signals represent the

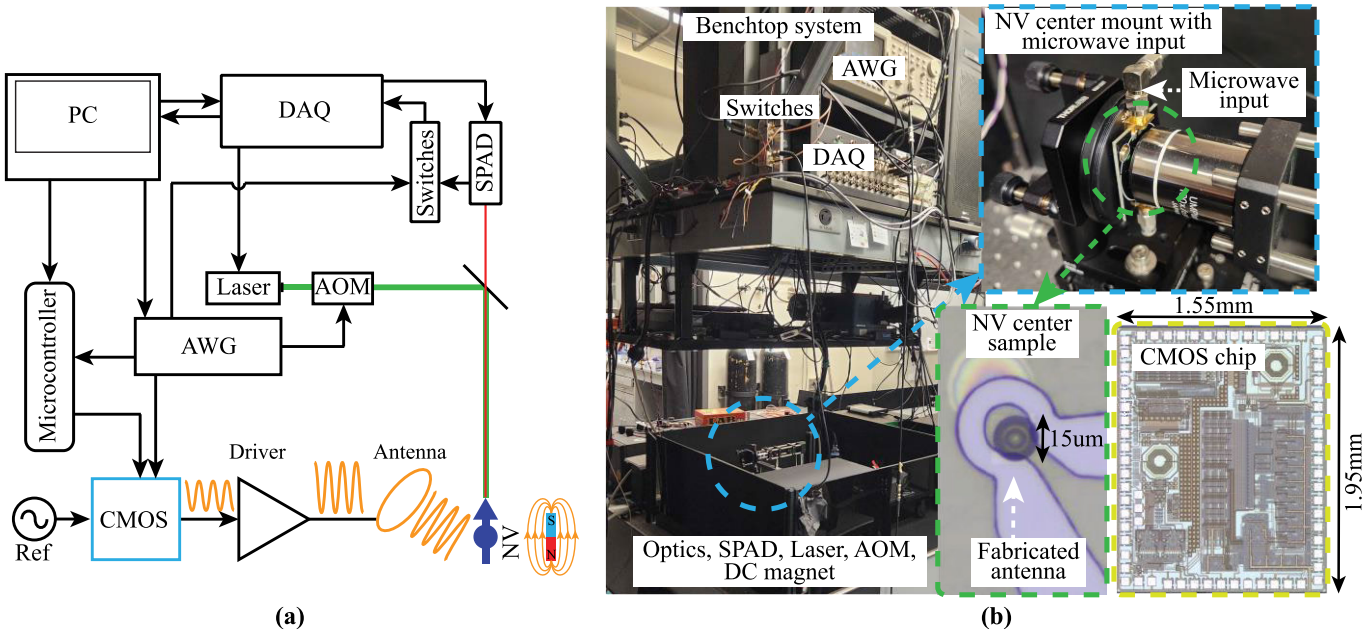

Fig. 16. (a) Block diagram of the spin control measurement setup and (b) photographs of the quantum measurement system including an NV center mount with a microwave input, a microphotograph of the NV center with a fabricated antenna, and a microphotograph of the CMOS chip.

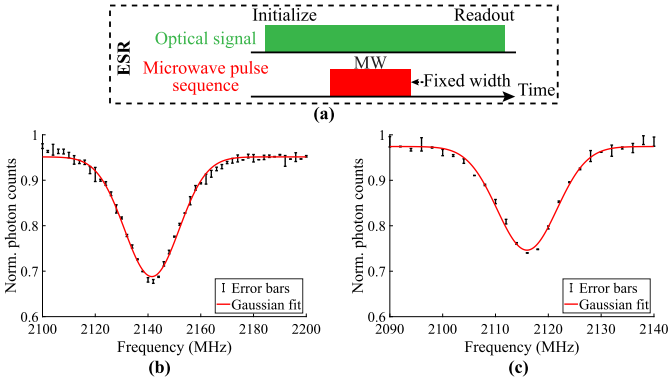

Fig. 17. (a) Timing diagram of the spin control pulse sequence for ESR measurements. ESR measurement results for (b) chip 1 and (c) chip 2.

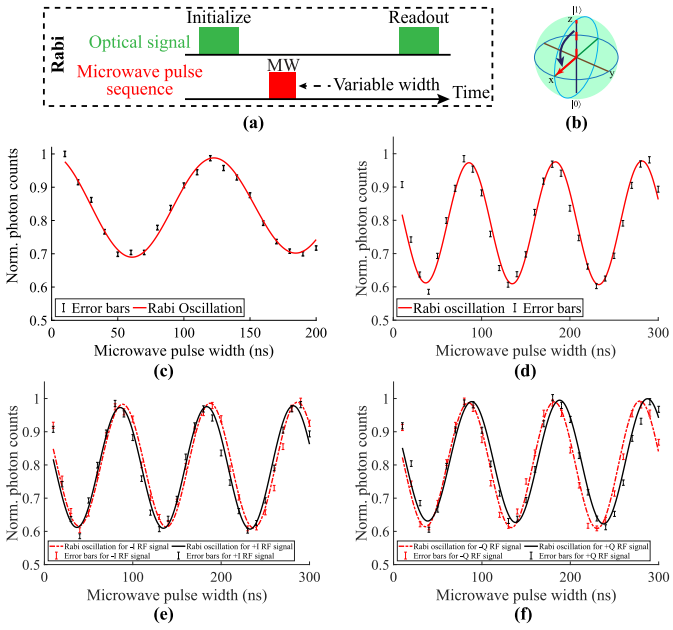

Fig. 18. (a) Timing diagram of the microwave pulse sequence used for Rabi measurements. (b) Bloch sphere representation of a spin transition during a microwave control for Rabi sequence. Rabi measurement results for (c) chip 1 and (d) chip 2: the black error bars represent measured data and the red curve represent sinusoidal fits. (e) Rabi measurements for $\pm I$ control signals for chip 2, and (f) Rabi measurements for $\pm Q$ control signals for chip 2.

optical excitation and readout signals, and red signals represent the generated microwave pulse sequence. The first optical signal initializes the NV center into the $m_s = 0$ state before the microwave pulse is applied and the second optical signal subsequently probes and projects the NV center onto the z-axis of the Bloch sphere. The microwave pulse width is changed after each measurement to observe Rabi oscillation. Fig. 18(b) shows a spin transition in the Bloch sphere as microwave control pulses with different durations are applied, causing the spin to proportionately rotate along a fixed axis. The amount of rotation depends on the microwave pulse widths for a constant signal amplitude. The optical readout results (the photon count) for different microwave pulse widths for chip 1 and chip 2 are shown in Fig. 18(c) and (d), respectively. The measured photon counts are normalized, and a sinusoidal fit is used to estimate the Rabi periods. In both cases, full sinusoidal signals are observed, which correspond to Rabi oscillations. The period of these oscillations depends on the applied microwave power. Based on the experiments, there is no apparent difference between chip 1 and chip 2 on Rabi oscillations measurements.

To study the effect of the I/Q mismatch of the generated pulse sequence at the chip output, four back-to-back Rabi measurements were performed. Fig. 18(e) and (f) demonstrate the measured photon counts for Rabi experiments for four different phases ($\pm I$ and $\pm Q$) of the applied microwave pulse

sequence generated using chip 2. The measured photon counts are normalized and used in order to extract the Rabi periods and confidence intervals (i.e., range of values with a 95% confidence level). The amplitude and phase mismatches in the generated quadrature signals result in variations in the Rabi oscillation period. In this case, Rabi oscillation periods of 99.5, 97.1, 97.9, and 98.9 ns for $\pm I$ and $\pm Q$ signals, were measured, respectively, corresponding to the confidence interval is in the range of 1.6, 1.4, 1.5, and 1.4 ns from the mean values for $\pm I$ and $\pm Q$ signals, respectively. During the calibration phase, the Rabi periods for $\pm I$ and $\pm Q$ signals can be matched by using slightly different gains for the amplifiers after the poly-phase filter. From these measurements, the average width of the $\pi/2$-pulse is estimated to be around 25 ns for chip 2.

C. Ramsey Measurements

The CMOS chip was also used to perform the Ramsey measurements for the NV center. In this case, the spin state of the NV center is initialized and optically excited in the same way as in the Rabi experiment. Then, the microwave frequency is detuned to about -5 MHz off the ESR frequency and the microwave pulse sequence shown in Fig. 19(a) is applied to the NV center. This pulse sequence consists of two $\pi/2$-pulses (each 25 ns wide) separated by a delay of τ, which is varied from 10 ns to 5 μs. The first pulse rotates the spin from the ground state into the equatorial plane [see Fig. 19(b)]. During the free precession time τ, magnetic noise in the NV's local environment as well as the inhomogeneous broadening of the external magnetic field induces a phase accumulation which translates the spin along a latitude line. After the delay τ, the spin is rotated with the second $\pi/2$ pulse. The photon count versus delay measurements for chip 1 and chip 2 is shown in Fig. 19(c) and (d), respectively. For measurements with the CMOS chip, T_2^* of 2.12±0.5 and 2.16±0.34 μs are measured for chip 1 and chip 2, respectively, where T_2^* represents the time of exponential decay of the Bloch vector to 1/e of its initial amplitude. This is in close agreement with the results obtained using the benchtop system [14].

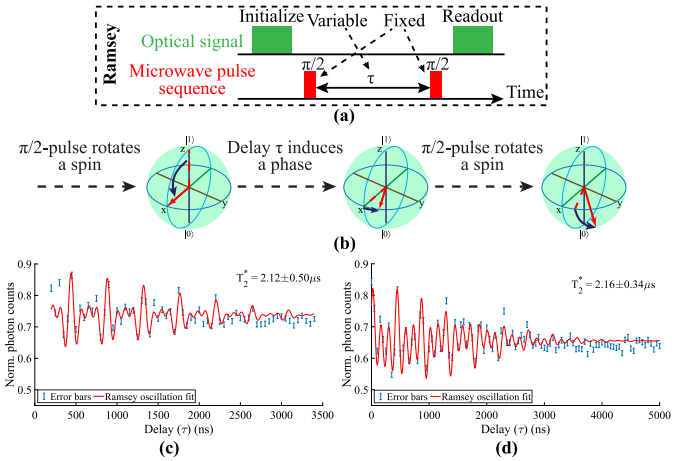

Fig. 19. (a) Timing diagram of the pulse sequence for Ramsey measurements. (b) Bloch sphere representation of the spin transition during a microwave control for Ramsey sequence. Ramsey measurement results for (c) chip 1 and (d) chip 2. The blue error bars represent measured data and the red curve represents a fit using the model presented in [14].

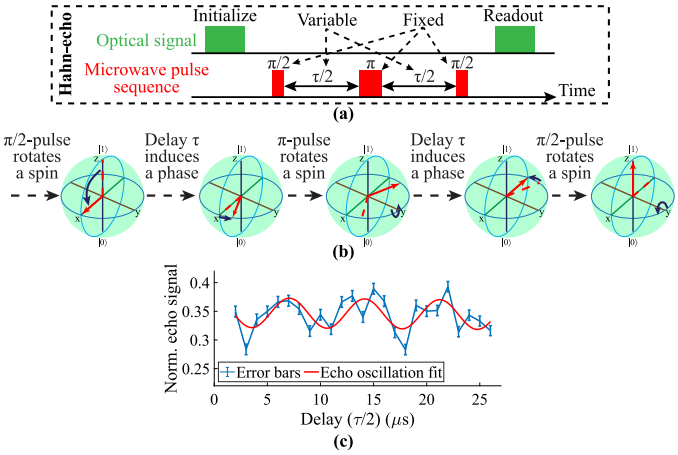

Fig. 20. (a) Timing diagram of the pulse sequence for Hahn-echo measurements. (b) Bloch sphere representation of a spin transition during a microwave control sequence applied for Hahn-echo measurements. (c) Hahn-echo measurement results for chip 2: the blue error bars represent measured data and the red curve represents the fit (using a train of Gaussians [23]).

D. Hahn-Echo Measurements

The Hahn-echo (i.e., spin-echo) protocol with a single refocusing π-pulse in the middle of two $\pi/2$-pulses is the building block for several advanced quantum measurements [22]. In Hahn-echo measurements, the spin state of the NV center is initialized and optically excited in the same way as in the previous experiments. Fig. 20(a) shows the timing diagram of the pulse sequence used for Hahn-echo measurements. As shown in Fig. 20(b), the first $\pi/2$ pulse rotates the spin by 90° to the equator. During free precession time of $\tau/2$, magnetic noise, around the spin of the electron, induces a phase. Next π-pulse flips the spin along a horizontal axis, leading to a change of the precession direction. Then, phase accumulates over a period of $\tau/2$. Last $\pi/2$ pulse rotates the spin by 90°. This measurement is repeated a number of times for different $\tau/2$ values (while keeping the π and $\pi/2$ pulses the same) and the state of the NV center for each measurement is recorded. The distribution of these states gives the projection along the z-axis of the Bloch sphere (i.e., the quantization axis). Hahn-echo protocol helps study the response of the NV center due to the inhomogeneous effects and perform relevant calibration. Fig. 20(c) shows the Hahn-echo measurements of the NV center using chip 2. In this experiment, the pulse widths are kept constant at 25 and 50 ns for $\pi/2$ and π pulses, respectively. The total evolution time, τ, is changed from 1 to 27 μs. The echo signal is constructed by subtracting two normalized photonic readouts for different phases of the last $\pi/2$ pulse. A train of Gaussians is fit to the normalized echo signal [23]. From this fit, revival periods, which are related to delays between pulses when the system is decoupled from slowly varying fields, can be observed. The revival period is equal to 6.92±0.18 μs, which arise from coupling energy to the ^{13}C spin bath [24]. This result is in good agreement with the measurement obtained with the benchtop setup, where the revival period was measured to be 7.07±0.29 μs. To the

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART SPIN CONTROL ARCHITECTURES

	This work	JSSC'21 [25]	JSSC'20 [10]	JSSC'19 [9]	JSSC'21 [11]
Operating temperature	300 K	300 K	3 K	3 K	4 K
Qubit platform	NV center	NV center	Transmons + spin qubits	Transmons	Spin qubits
Frequency	1.6-2.6 GHz[a]	2.87 GHz	2-20 GHz	4-8 GHz	11-17 GHz
Channels	1	1	32	1	16
SFDR	>40 dB	N/A	>42 dB	N/A	> 40 dB
SNR	>50 dB	N/A	>48 dB	N/A	> 50 dB
Technology node	180 nm bulk CMOS	65 nm CMOS	22 nm FinFET CMOS	28 nm bulk CMOS	22 nm FinFET CMOS
Waveform	Up to 2^{12} pulses	Off-chip modulation	Up to 2^{3} pulses	2^{4} symmetric waveforms	Up to 2^{19} pulses
Reconfigurable pulses	Yes	Off-chip	Yes	No	Yes
Quantum	External	External	External	External	External
Power	Analog: 48 mW Digital: 32 mW	40 mW	Analog: 54 mW Digital: 300 mW	Analog: <2 mW/qubit	Analog: 5.2 mW/qubit Digital:140 mW
Chip area	3 mm^2	1.5 mm^2[b]	4 mm^2	1.6 mm^2	16 mm^2

[a] Depends on the magnetic strength. [b] Includes sensing part

best of our knowledge, this is the first demonstration of such experiments with NV center using a CMOS chip. The performance of the implemented chip is compared with a few recently reported systems in Table I.

VI. SNR AND ESR CONTRAST

There are two possible mechanisms for an excited NV center to relax to a ground state. The first mechanism is to emit a photon and directly relax to a lower state. The second mechanism is to first relax to a metastable state and non-radiatively decay to a ground state, which makes the NV center's fluorescence intensity state dependent. The statistical probability of decaying non-radiatively through a metastable state is 30% [17]. This defines the maximum contrast level that can be achieved for a continuous wave excitation. The experimental contrast level sets the signal-to-noise ratio (SNR) of the received optical signal. Defining the SNR as [26]

$$\text{SNR} = \frac{I_{\max} - I_{\min}}{\sqrt{I_{\max} + I_{\min}}} \tag{1}$$

where $I_{\max}$ and $I_{\min}$ are the mean number of detected photons for a single measurement of $|0\rangle$ and $|1\rangle$ spin states, respectively, and can be calculated from the ESR measurements (i.e., ESR contrast). The contrast level can be defined as

$$C = \frac{I_{\max} - I_{\min}}{I_{\max}}. \tag{2}$$

Using (1) and (2), the SNR can be written in terms of the contrast level as

$$\text{SNR} = \sqrt{I_{\max}} \times \frac{C}{\sqrt{2 - C}}. \tag{3}$$

Equation (3) suggests that the SNR depends on photon collection efficiency and spin contrast.

Note that for the case that $C = 1$, corresponding to the full contrast, the SNR is limited only by shot noise. Equation (3) indicates that is directly related to the readout fidelity [21]. The higher the fidelity, the higher the confidence in each quantum measurement outcome.

In the benchtop system, an ultrahigh resolution frequency synthesizer (SG384 with 1 μHz resolution) and high precision AWG (AWG520 Tektronix, with 1 ns precision) provide consistent contrast in ESR measurements approaching 30%. The proposed design was tested for the same experiment with multiple chips. Fig. 21 shows the achieved contrast in ESR measurements for different chips at respective ESR frequencies.

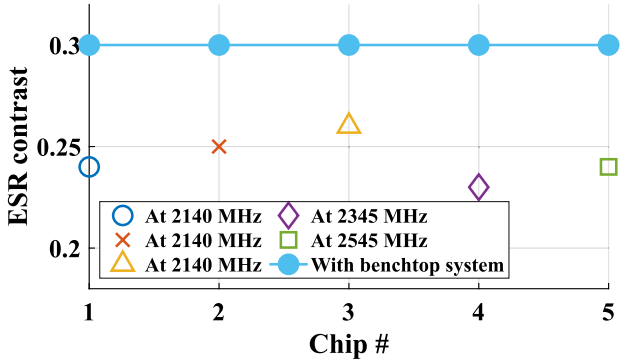

Fig. 21. Variation of ESR contrasts with different chips and respective resonance frequencies.

The measurements using different chips achieve consistent results with the ESR contrast between 0.23 and 0.26 with a mean value of 0.24. To improve the ESR contrast, the power of the microwave signal and the delay-to-pulse width ratio can be adjusted.

VII. CONCLUSION

A 180-nm CMOS integrated chip has been implemented and used at room temperature to demonstrate spin control of NV centers. The circuit generates reconfigurable microwave pulse sequences at 1.6–2.6 GHz. The minimum achievable pulse width and pulse-to-pulse delay are 10 and 18 ns, respectively. Due to its reconfigurable memory structure, different pulse sequences were generated to perform ESR, Rabi, Ramsey, and Hahn-echo measurements on a single NV center. The T_2^* of 2.16 μs was measured, and revival periods were observed. The CMOS chip was implemented within a footprint of 1.95 × 1.55 mm^2 and consumes 80 mW from a 1.8 V supply. The analog circuitry consumes 48 mW of which 19 mW is

consumed by the PLL, 16 mW is consumed by the VCO, and about 13 mW is consumed by the variable gain amplifiers.

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