

Shared Redundancy Strategy to Improve the Reliability and Fault-Tolerant Capability of Modular Multilevel Converter

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Abstract—Utilizing redundant submodules is a well-known strategy to improve the reliability and fault-tolerant capability of the modular multilevel converter (MMC). Redundancy-based fault-tolerant strategy makes it possible to restore the full performance of the converter in the postfault condition. The main drawback of this strategy is the high cost. In this configuration, each redundant submodule (RSM) can only be utilized in a specific arm and it cannot be used in other arms. This limitation leads to inefficient utilization of the RSMs in conventional MMC. This article proposes a shared redundancy strategy which allows RSMs to be used either in upper or lower arms. The derived reliability models in various case studies illustrate that the proposed strategy significantly improves the reliability and useful lifetime of MMC. To investigate the effectiveness of the proposed strategy, simulation and experimental results are provided.

Index Terms—Fault-tolerant, modular multilevel converter (MMC), reliability, shared redundancy strategy.

I. INTRODUCTION

DISTINCTIVE features of modular multilevel converter (MMC) have made it the main candidate for medium and high power applications [1]. Modularity and scalability of this converter have removed the obstacles to achieve higher voltages. Bulk-power transmission by HVDC link, back-to-back connection between various ac grids, and offshore wind farm integration are from several applications of the MMC [2]. In the MMC-based motor drive applications, the phase shifting transformer with multiple secondary windings is removed which reduces the cost, size, and weight of the whole system. In spite of these remarkable features, MMC consists of huge

number of capacitors and semiconductor devices, which affects the reliability and availability of the converter [3]. Although reliability is a common issue of all multilevel converters, the problem is worse in MMC because it is mainly used in very high voltage applications. Even at a similar voltage level, the MMC needs more capacitors and semiconductor devices compared to other multilevel topologies such as cascaded H-bridge converter (CHB), neutral-point clamped converter, or flying capacitor converter [4]. In a nutshell, boosting reliability and fault-tolerant capability of MMC is essential to prevent unplanned interruptions.

Among various fault-tolerant scheme, utilizing redundant submodules (RSMs) is more compatible with MMC. In this scheme, some RSMs are embedded in each arm of the converter that could be employed instead of faulty SMs [1]. Two main strategies, also, are presented. In the first strategy, which is called passive-RSM strategy or cold-RSM strategy, the RSMs do not participate in the modulation during normal operation. Once the fault occurs, the faulty SMs are bypassed and equal number of RSMs are inserted into the circuit [5]–[10]. The RSMs in this strategy have no initial charge. Replacing faulty SMs by cold-RSMs leads to imbalance of arm energies and severe circulating current that should be controlled during the charging period [1], [5], [6]. In the second strategy, which is called active-RSM strategy or hot-RSM strategy, all RSMs are utilized in both normal and fault conditions [10]. Some of these methods utilize the SMs and RSMs at their nominal voltage [10]. Some others, however, share the load among all available submodules to have less voltage stress on components and more voltage levels in the output [10]. These methods, also, have a transient charging period to share the missed voltage again between the surviving submodules [10]. In the hot-RSM strategy, there is more semiconductor devices in the current path which leads to larger power loss. Because of that, the hot-RSM strategy is more suitable for medium and low voltage applications while the cold-RSM strategy is more interesting in high-power applications like HVDC [1], [10]. Even though utilizing RSMs is costly, it guarantees the full performance of the MMC in postfault conditions without mentioned problems from previous groups [1].

Several studies are conducted to evaluate the reliability and lifetime of MMC considering RSM-based strategies. In [11], the Markov model is used to evaluate the reliability of MMC.

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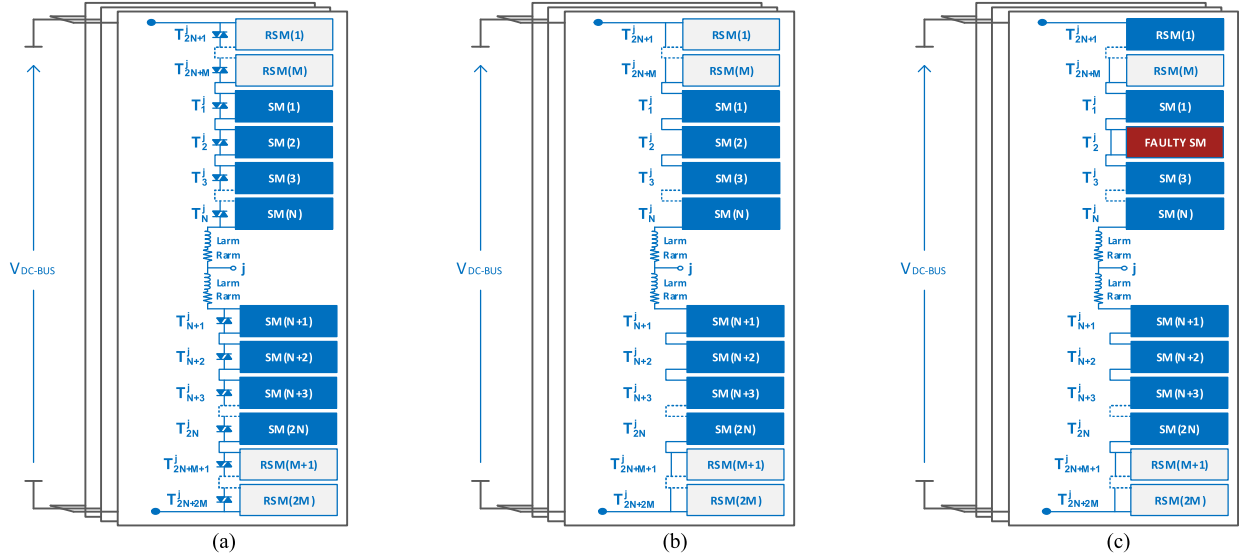


Fig. 1. (a) Conventional configuration of three-phase MMC with N SMs and M cold-RSMs in each arm. (b) T_1^j to T_{2N}^j are OFF and T_{2N+1}^j to T_{2N+2M}^j are ON during normal operation. (c) Faulty SM is bypassed and one RSM is replaced.

In this article, each arm is equipped by only one RSM and the reliability model extracted for single-fault in each arm. Tu *et al.* [12] have proposed a hierarchical model for the reliability assessment of MMC. In this article, k -out-of- n : G system [13] is used for hot redundancy, and homogeneous Poisson process (HPP) is utilized for cold redundancy strategies. The missed point in [12] is that power loss dissipation inside the SMs is not homogenous. According to [14]–[16], the power loss and junction temperature of lower insulated-gate bipolar transistor (IGBT) is significantly higher than the upper ones in half-bridge SMs. Since the junction temperature is from the main factors in IGBT faults, the failure rates of these switches should not be considered equal [17]. Indeed, in the hot-RSM strategy with load sharing, the SM voltages and switching frequency increase after each fault. Farzankia *et al.* [4] and Guo *et al.* [17] also have compared the reliability of MMC with various strategies. The obtained result in these studies show that cold-RSM strategy is more reliable compared with the hot-RSM strategies.

According to [1], the reliability of MMC is still a major concern and strategies that can improve the reliability and lifetime of MMC with lower cost is demanded by industry. The main limitation of RSM-based methods is that the embedded RSMs can only be utilized in one specific arm and it is not possible to use them to tolerate the faults in other arms. Farias *et al.* [1] and Guo *et al.* [17] have mentioned the potential benefits of sharing redundancy among the converter arms. However, the need for practical structures that can share the RSMs among arms still is sensed. This article proposes a modified configuration of the MMC that shares the RSMs among the converter arms. The proposed configuration is applicable for various number of RSMs. Obtained results demonstrate a considerable improvement in the reliability and useful lifetime of the converter.

II. OPERATION PRINCIPLE OF CONVENTIONAL MMC USING COLD-RSM STRATEGY

Fig. 1(a) shows a three-phase MMC with N SMs and M cold-RSMs in each arm. Various structures are proposed for submodules, where the half-bridge structure is more common because of its higher efficiency and simplicity [2]. The reference voltage of upper and lower arms of phase j in ideal condition is as follows:

$$v_U^j = \frac{V_{DC-Bus}}{2} - \frac{V_{DC-Bus}}{2} m \sin(\omega t + \varphi_0^j) \quad (1)$$

$$v_L^j = \frac{V_{DC-Bus}}{2} + \frac{V_{DC-Bus}}{2} m \sin(\omega t + \varphi_0^j) \quad (2)$$

where V_{DC-Bus} is the overall dc bus voltage and m is the modulation index. The output phase-to-neutral voltage of MMC is as follows:

$$v_j = \frac{V_{DC-Bus}}{2} m \sin(\omega t + \varphi_0). \quad (3)$$

As it can be seen in Fig. 1(a), each submodule (SM or RSM) is equipped by a bidirectional switch which is usually a thyristor valve. These switches are utilized to insert the submodules into the circuit or bypass them. Sometimes, a vacuum contactor, also, is connected in parallel with the thyristor valve to reduce their conduction loss [1]. In the cold-RSM strategies, all SMs are in the current path and all RSMs are bypassed during normal operation. For this purpose, according to Fig. 1(b), T_1^j to T_{2N}^j are OFF and T_{2N+1}^j to T_{2N+2M}^j are ON. Once a fault occurs in one SM, according to Fig. 1(c), corresponding T should be turned ON and one of the RSMs at the faulty arm should be inserted into the circuit.

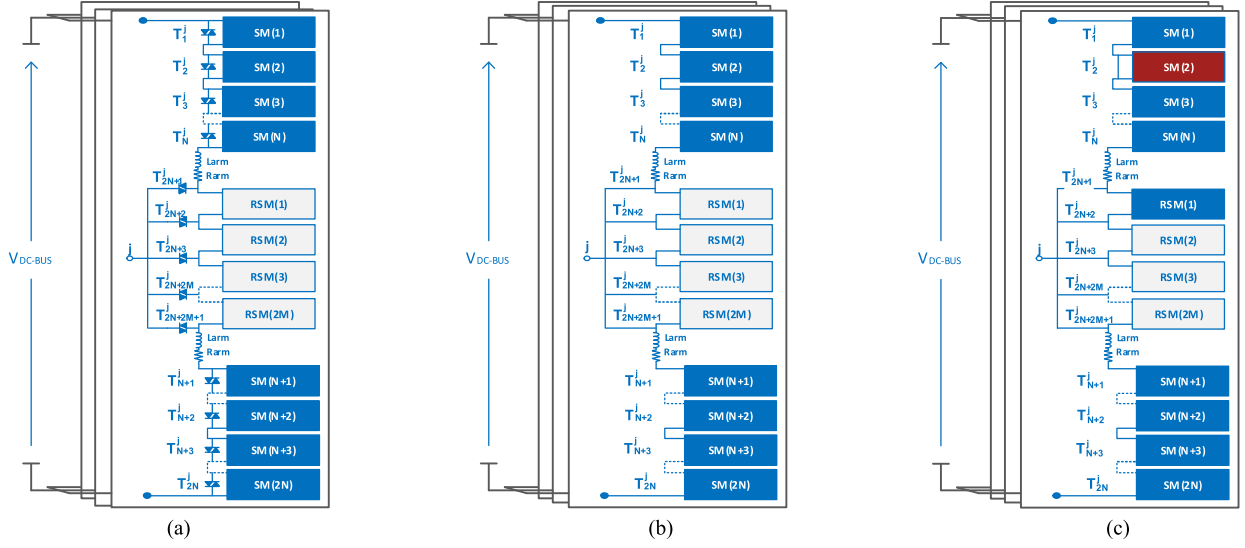


Fig. 2. (a) Proposed configuration with N SMs in each arm and $2M$ shared cold-RSMs in each phase. (b) T_1^j to T_{2N}^j are OFF and T_{2N+1}^j to $T_{2N+2M+1}^j$ are ON during normal operation. (c) Faulty SM is bypassed and one cold-RSM is replaced.

III. PROPOSED CONFIGURATION FOR SHARED REDUNDANCY STRATEGY

The main drawback of redundancy-based strategies is the high implementation cost. The utilized RSMs in the conventional MMC can operate at a specific arm and cannot be utilized in other arms. For instance, assume an MMC with four SMs and one RSM in each arm. If one of the SMs is defected in the upper arm of phase A, it can be replaced by the embedded RSM in this arm. However, if another SM at the same arm becomes faulty, there is no other RSM available. Hence, the converter cannot handle the new fault condition. In the described situation, the converter has five remaining unused RSMs in other healthy arms. However, those five unused RSMs cannot be used because of structural constraints.

This article proposes a modified configuration of the MMC which makes it possible to share RSMs between upper and lower arms of each phase. In other words, all RSMs in each phase can replace the faulty SMs regardless of their location, either in upper or lower arms. Fig. 2(a) illustrates the proposed configuration. Analogous to the conventional configuration in Fig. 1(a), each arm of the proposed configuration has N operating SMs with $2M$ RSMs in each phase. Each SM has a bidirectional thyristor valve (T_1^j to T_{2N}^j), which are connected in parallel. The RSMs, however, do not have the parallel thyristor valves. Instead, T_{2N+1}^j to $T_{2N+2M+1}^j$ are embedded according to Fig. 2(a) to control the RSMs' operation. In the normal condition, according to Fig. 2(b), T_1^j to T_{2N}^j are OFF and T_{2N+1}^j to $T_{2N+2M+1}^j$ are ON. Therefore, all SMs are in the circuit and all RSMs are bypassed. Once a fault occurs in one SM at the upper arm, the corresponding T should be turned ON to bypass the faulty SM. At the same time, T_{2N+1}^j is turned OFF. Fig. 2(c) illustrates the proposed configuration when one SM in upper arm is faulty. As it can be seen, the RSM(1) is inserted into the upper arm after the fault occurrence. For the next fault in the upper arm, the faulty

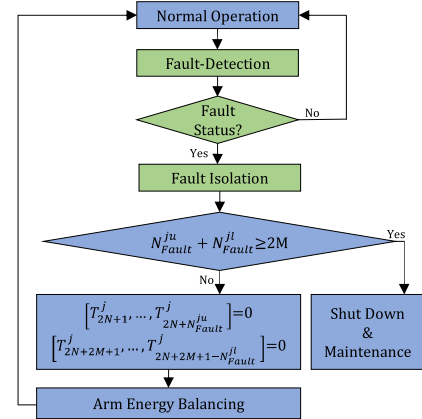


Fig. 3. Flowchart of the control system.

SM should be bypassed and T_{2N+2}^j should be turned OFF. This process can be replicated for up to $2M$ faulty SMs in the upper arm. In the case of having fault in the lower arm, also, the faulty SM should be bypassed and one RSM should be inserted in the lower arm by opening $T_{2N+2M+1}^j$.

The operation principle of protection system is illustrated in Fig. 3. After the fault occurrence, the fault detection unit activates the fault-tolerant strategy. In the next step, the number of faulty SMs in each phase is compared with the available RSMs ($2M$). If the number of faulty SMs in each phase is lower than the embedded RSMs, the required RSMs are inserted to the faulty arms and system returns to the normal operation after a transient charging period [1]. Otherwise, the system should be turned OFF. The fault conditions can be classified into three sections. The first section consists of the fault conditions with utmost M faulty SMs in each arm. Both conventional and proposed configurations can handle these fault states. The second section contains the fault

states with more than $2M$ faulty SMs in one phase. Both of the configurations cannot handle these faults. In the third section, the number of faulty SMs in one arm is from $(M + 1)$ to $2M$. These faults cannot be handled by the conventional MMC while the proposed configuration is able to handle them.

IV. RELIABILITY MODELING

According to [12], reliability is a probability which shows a system will perform correctly during specific period of time and under a certain operating or environmental condition. The useful lifetime of system, also, is defined as the time period which the reliability of system is larger than an expected value. For example, B1 factor shows the time period which the reliability of system is larger than 0.99. In other words, B1 is the time period that 1% of components are failed. Accordingly, B10 factor shows the time period that the reliability of system is larger than 0.9. These parameters usually are considered to select the guarantee period by producers [12]. Each system, also, has a failure rate which can be defined as follows:

$$\lambda(t) = -\frac{1}{R(t)} \frac{dR(t)}{dt} \quad (4)$$

where $R(t)$ is the reliability function. This article aims to provide reliability models based on constant failure rates and compare them in various case studies. Consequently, the reliability function of system could be written as follows [12], [18]:

$$R(t) = e^{-\lambda t}. \quad (5)$$

A. Reliability Model of Components

In order to obtain the reliability model of MMC, it is required to model the reliability of all components in the converter.

1) Reliability Model of Diode: According to [18], the failure rate of diode can be written as follows:

$$\lambda_{\text{diode}} = \lambda_{\text{base}}^{\text{diode}} \cdot \pi_T^{\text{diode}} \cdot \pi_S^{\text{diode}} \cdot \pi_C^{\text{diode}} \cdot \pi_Q^{\text{diode}} \cdot \pi_E^{\text{diode}} \text{ FIT}. \quad (6)$$

In this model, $\lambda_{\text{base}}^{\text{diode}}$ is the base failure rate of diode, and 1FIT is equal to 10^{-9} failure in hour. The π_T^{diode} is the temperature factor that can be obtained from the following equation:

$$\pi_T^{\text{diode}} = e^{-3091 \left(\frac{1}{T_J^{\text{diode}} + 273} - \frac{1}{298} \right)} \quad (7)$$

where T_J^{diode} is the junction temperature of diode that can be calculated as follows:

$$T_J^{\text{diode}} = P_{\text{Loss_Total}}^{\text{diode}} \times \left(\frac{R_{thJC}^{\text{diode}}}{k} + \frac{R_{thCH}^{\text{diode}}}{k} \right) + T_{\text{heat-sink}}. \quad (8)$$

In this equation, R_{thJC}^{diode} is the junction to the case thermal resistance, R_{thCH}^{diode} is the case to heat-sink thermal resistance, k is the current factor, $T_{\text{heat-sink}}$ is the heat-sink temperature, and $P_{\text{Loss_Total}}^{\text{diode}}$ is the total power loss of the diode that can be calculated as follows:

$$P_{\text{Loss_Total}}^{\text{diode}} = P_{\text{conduction}}^{\text{diode}} + P_{\text{off}}^{\text{diode}} \quad (9)$$

where $P_{\text{conduction}}^{\text{diode}}$ is the conduction loss, and $P_{\text{off}}^{\text{diode}}$ is the turn-OFF loss of diode that can be calculated as follows:

$$P_{\text{conduction}}^{\text{diode}} = \frac{k}{T} \int_{t_0}^{t_0+T} \frac{i_F(\tau)}{k} \times V_F \left(\frac{i_F(\tau)}{k} \right) d\tau \quad (10)$$

$$P_{\text{off}}^{\text{diode}} = \frac{k}{T} \sum_{n=1}^N \frac{V_{F,\text{off}}(n)}{V_{CE,\text{ref}}} E_{\text{rec}} \left(\frac{i_F(n)}{k} \right). \quad (11)$$

In these equations, T is the calculating period to obtain the average value, i_F is the forward current of diode during conduction, $V_{F,\text{off}}$ is the blocking voltage in the n th switching action, $V_{CE,\text{ref}}$ is the reference blocking voltage, and E_{rec} is the energy loss in the turn-OFF process of diode. Up to here, the temperature factor of diode can be calculated. The next factors are π_S^{diode} , π_C^{diode} , π_Q^{diode} , and π_E^{diode} that are electrical stress factor, contact construction factor, quality factor, and environmental factor, respectively. The stress factor can be obtained from (12) and other factors can be selected from [18] based on the specific application

$$\pi_S^{\text{diode}} = \begin{cases} 0.054 & V_{\text{operating}} < 0.3V_{\text{rated}} \\ \left(\frac{V_{\text{operating}}}{V_{\text{rated}}} \right)^{2.43} & V_{\text{operating}} \geq 0.3V_{\text{rated}} \end{cases}. \quad (12)$$

Considering mentioned factors in (6), the reliability model of diode would be as follows:

$$R(t) = e^{-\lambda_{\text{diode}} t}. \quad (13)$$

2) Reliability Model of IGBT: The failure rate of IGBT is as follows [18]:

$$\lambda_{\text{IGBT}} = \lambda_{\text{base}}^{\text{IGBT}} \cdot \pi_T^{\text{IGBT}} \cdot \pi_A^{\text{IGBT}} \cdot \pi_R^{\text{IGBT}} \cdot \pi_S^{\text{IGBT}} \cdot \pi_Q^{\text{IGBT}} \cdot \pi_E^{\text{IGBT}} \text{ (FIT)}. \quad (14)$$

Similar to the diode, the temperature factor of IGBT can be calculated as follows:

$$\pi_T^{\text{IGBT}} = e^{-2114 \left(\frac{1}{T_J^{\text{IGBT}} + 273} - \frac{1}{298} \right)}. \quad (15)$$

The junction temperature of IGBT, also, can be calculated as follows:

$$T_J^{\text{IGBT}} = P_{\text{Loss_Total}}^{\text{IGBT}} \times \left(\frac{R_{thJC}^{\text{IGBT}}}{k} + \frac{R_{thCH}^{\text{IGBT}}}{k} \right) + T_{\text{heat-sink}} \quad (16)$$

where R_{thJC}^{IGBT} is the junction to the case thermal resistance, R_{thCH}^{IGBT} is the case to heat-sink thermal resistance, and $P_{\text{Loss_Total}}^{\text{IGBT}}$ is the total power loss of the IGBT that can be calculated as follows:

$$P_{\text{Loss_Total}}^{\text{IGBT}} = P_{\text{conduction}}^{\text{IGBT}} + P_{\text{on}}^{\text{IGBT}} + P_{\text{off}}^{\text{IGBT}}. \quad (17)$$

The conduction loss of IGBT is as follows:

$$P_{\text{conduction}}^{\text{IGBT}} = \frac{k}{T} \int_{t_0}^{t_0+T} \frac{i_C(\tau)}{k} \times V_{CE} \left(\frac{i_C(\tau)}{k} \right) d\tau \quad (18)$$

where i_C is the switch current and V_{CE} is the switch voltage in ON state. The turn-ON and turn-OFF loss of IGBT, also, are as follows:

$$P_{\text{on}}^{\text{IGBT}} = \frac{k}{T} \sum_{n=1}^N \frac{V_{CE,\text{off}}(n)}{V_{CE,\text{ref}}} E_{\text{on}} \left(\frac{i_C(n)}{k} \right) \quad (19)$$

$$P_{\text{off}}^{\text{IGBT}} = \frac{k}{T} \sum_{n=1}^N \frac{V_{CE,\text{off}}(n)}{V_{CE,\text{ref}}} E_{\text{off}} \left(\frac{i_C(n)}{k} \right) \quad (20)$$

where, $V_{CE,\text{off}}(n)$, $i_C(n)$, E_{on} , and E_{off} are the blocking voltage of IGBT, switch current, energy loss in turning ON, and energy loss in turning OFF process at the n th switching action. The next factor is the power rating factor of IGBT that can be obtained as follows [18]:

$$\pi_R^{\text{IGBT}} = (P_{\text{rated}})^{0.37}. \quad (21)$$

And the voltage stress factor is as follows [18]:

$$\pi_S^{\text{IGBT}} = 0.045 e^{3.1 \left(\frac{V_{CE}}{V_{\text{rated}}} \right)} \quad (22)$$

where V_{CE} is the applied voltage and V_{rated} is the rated voltage of switch. Other factors, also, are reported in [18] based on the target application. Considering these factors in (14), the reliability model of IGBT is as follows:

$$R(t) = e^{-\lambda_{\text{IGBT}} t}. \quad (23)$$

3) Reliability Model of Capacitor: The failure rate and reliability of the capacitor depends on its technology considering required voltage, current, and power rating. The application of MMC is in medium and high powers that current rating is from tens to hundreds of amperes. The capacitor voltage, also, is a few kilovolts. For these applications, AVX film capacitor is a suitable choice. In these capacitors, the failure rate is as follows [19]:

$$\lambda_{\text{Cap}} = \lambda_{\text{base}}^{\text{Cap}} \cdot \pi_Q^{\text{Cap}} \cdot \pi_E^{\text{Cap}} \cdot \pi_B^{\text{Cap}} \quad (\text{FIT}) \quad (24)$$

where π_Q^{Cap} , π_E^{Cap} , and π_B^{Cap} are qualification and environmental factors and their values are reported in [19] for various conditions. The base failure rate, also, can be calculated as follows:

$$\lambda_{\text{base}}^{\text{Cap}} = 3 \times 10^{5.738 \left(\frac{V_{\text{operating}}}{V_{\text{rated}}} - 1 \right)} \times e^{3.933 \left(\frac{\theta_{\text{HS}} + 273}{368} \right)^{27.75}} \quad (\text{FIT}) \quad (25)$$

where θ_{HS} is the hot spot point temperature that can be obtained as follows:

$$\theta_{\text{HS}} = \theta_{\text{amb}} + (P_j + P_d) \times (R_{\text{th1}} + R_{\text{th2}}). \quad (26)$$

In this equation, R_{th1} is the thermal resistance between hot spot and case, and R_{th2} is the thermal resistance between the case and ambient air. The P_j and P_d , also, are Joule losses and dielectric losses, respectively. The absolute maximum hot spot temperature of AVX film capacitor is 95 °C [19]. Indeed, these capacitors are available in a vast rating and dimensions. Therefore, according to the method presented in [19], dimensions and thermal resistances of capacitor can be selected in a way to limit the hot spot temperature. Considering safety margin, 85 °C is a reasonable target for hot spot temperature [19]. Hence, the reliability model of the capacitor is as follows:

$$R(t) = e^{-\lambda_{\text{Cap}} t}. \quad (27)$$

4) Reliability Model of Thyristor: According to [18], the failure rate of thyristor can be written as follows:

$$\lambda_{\text{Thyristor}} = \lambda_{\text{base}}^{\text{Thyristor}} \times \pi_T^{\text{Thyristor}} \times \pi_R^{\text{Thyristor}} \times \pi_S^{\text{Thyristor}} \times \pi_Q^{\text{Thyristor}} \times \pi_E^{\text{Thyristor}} \quad (\text{FIT}). \quad (28)$$

The temperature factor for thyristor, $\pi_T^{\text{Thyristor}}$, can be calculated as follows:

$$\pi_T^{\text{Thyristor}} = e^{-3082 \left(\frac{1}{T_J^{\text{Thyristor}} + 273} - \frac{1}{298} \right)} \quad (29)$$

where $T_J^{\text{Thyristor}}$ is the junction temperature of thyristor, which can be calculated as follows:

$$T_J^{\text{Thyristor}} = P_{\text{Loss_Total}}^{\text{Thyristor}} \times \left(\frac{R_{\text{thJC}}^{\text{Thyristor}}}{k} + \frac{R_{\text{thCH}}^{\text{Thyristor}}}{k} \right) T_{\text{heat-sink}}. \quad (30)$$

In this equation, $P_{\text{Loss_Total}}^{\text{Thyristor}}$ is the total power loss in thyristor, $R_{\text{thJC}}^{\text{Thyristor}}$ is the thermal resistance between junction and case, $R_{\text{thCH}}^{\text{Thyristor}}$ is the thermal resistance between the case and heat sink, and k is the current factor. The power loss in thyristor consists of turn-OFF loss, turn-ON loss, and conduction loss. In this application, however, the thyristors do not have repetitive switching actions. Therefore, the dominant power loss in here is the conduction loss that can be calculated as follows:

$$P_{\text{conduction}}^{\text{Thyristor}} = \frac{k}{T} \int_{t_0}^{t_0+T} \frac{i_F(\tau)}{k} \times V_F \left(\frac{i_F(\tau)}{k} \right) d\tau. \quad (31)$$

In this equation, i_F is the forward current and V_F is the forward voltage of thyristor in the ON state. The thermal resistances in (30), also, can be extracted from the thyristor's datasheet. The next factor is $\pi_R^{\text{Thyristor}}$ that is current rating factor. According to [18], this factor can be calculated using the following equation:

$$\pi_R^{\text{Thyristor}} = (I_{\text{rms}})^{0.4} \quad (32)$$

where I_{rms} is the rms current of thyristor. The voltage stress factor, also, can be calculated as follows:

$$\pi_S^{\text{Thyristor}} = \left(\frac{V_{\text{Applied}}^{\text{Thyristor}}}{V_{\text{Thyristor rated}}^{\text{Thyristor}}} \right)^{1.9}. \quad (33)$$

In this factor, $V_{\text{Applied}}^{\text{Thyristor}}$ is the applied blocking voltage, and $V_{\text{Thyristor rated}}^{\text{Thyristor}}$ is the rated blocking voltage of the thyristor. The quality factor ($\pi_Q^{\text{Thyristor}}$) and environmental factor ($\pi_E^{\text{Thyristor}}$), also, are reported for various conditions in [18] that can be selected based on the target application.

B. Reliability Model of SM

The distribution of power loss between SMs is homogeneous. However, the IGBTs and diodes of SM have different loading and power loss. Obtained results in [15]–[17] demonstrate that the power loss of lower IGBT is significantly larger than the upper one in a vast range of power factors. Conversely, the power loss in upper diode is much larger than the lower diode. According to (15) and (16), higher power loss leads to higher junction temperature and higher failure rate. Therefore, the

failure rate of each IGBT and diode in SM should be calculated separately. Considering these differences, the overall failure rate of SM can be written as follows:

$$\lambda^{SM} = \lambda_{IGBT}^{upper} + \lambda_{IGBT}^{lower} + \lambda_{diode}^{upper} + \lambda_{diode}^{lower} + \lambda_{Capacitor}. \quad (34)$$

The reliability function of each submodule, also, could be written as follows:

$$R(t) = e^{-\lambda^{SM}t}. \quad (35)$$

Since the conventional MMC and proposed configuration utilize same SMs, reliability model of SM in (29) is valid to use at both structures.

C. Reliability Model of MMC and Proposed Configuration

According to definition in [12], each arm of the MMC with cold-RSMs is a repairable system meaning that it returns to the prefault condition after replacing the faulty SM by an RMS. Number of faults in repairable systems is distributed by HPP [12]. Following equation shows the probability of having Q faults in HPP:

$$P_Q(t) = \frac{(\lambda_{SYS}t)^Q}{Q!} e^{-\lambda_{SYS}t} \quad (36)$$

where λ_{SYS} is the failure rate of the repairable system. In the conventional MMC, each arm could be repaired up to M times. Therefore, each arm can operate properly as far as the number of faulty SMs is between zero to M . Hence, the reliability function of each arm at conventional MMC is as follows:

$$R_{MMC}^{arm}(t) = \sum_{i=0}^M \frac{(\lambda_{MMC}^{arm}t)^i}{i!} e^{-\lambda_{MMC}^{arm}t} \quad (37)$$

where λ_{MMC}^{arm} is the failure rate of the arm which always consists of N operating submodules, M conducting thyristor valves, N thyristor valves that are OFF, and one inductor. Hence, the failure rate of each arm of MMC can be written as follows:

$$\lambda_{MMC}^{arm} = N\lambda^{SM} + M\lambda_{TV}(ON) + N\lambda_{TV}(OFF) + \lambda_{Inductor} \quad (38)$$

where λ_{TV} is the failure of thyristor valves that is two reverse parallel thyristors. Conventional MMC consists of six arms where all of them should perform properly to have a healthy system. Therefore, the reliability function of conventional MMC can be obtained by multiplying reliability function of six arms (that are the same) as follows:

$$R_{MMC}(t) = (R_{MMC}^{arm}(t))^6 = \left[\sum_{i=0}^M \frac{(\lambda_{MMC}^{arm}t)^i}{i!} e^{-\lambda_{MMC}^{arm}t} \right]^6 \quad (39)$$

In the conventional MMC, repairability is in the arm level, while in the proposed configuration, the repairability is in the phase level. In other words, each phase of the proposed configuration can be repaired up to $2M$ times. Therefore, each phase can operate properly as far as the number of faulty SMs would be between zero to $2M$. Consequently, the reliability function

TABLE I
CASE STUDY PARAMETERS

Parameter	Value
DC bus voltage	33 kV
Rated power	15 MVA
Rated line-to-line voltage (rms)	20 kV
Number of SMs per arm	20
Number of RSMs per phase	4 ($M=2$)
Nominal voltage of SMs and RSMs	1.65 kV
Capacitance of SMs and RSMs	3.85 mF
Capacitor voltage ripple	10%
Load impedance	$21.78 + 16.33j \Omega$ (1 pu)
Arm inductance	10.6 mH (0.15 pu)
Arm resistance	1.067Ω (0.04 pu)
Switching frequency	300 Hz (5 pu)
System frequency	60 Hz (1 pu)
Modulation index	0.96

of each phase can be written as follows:

$$R_{New}^{Phase}(t) = \sum_{i=0}^{2M} \frac{(\lambda_{New}^{Phase}t)^i}{i!} e^{-\lambda_{New}^{Phase}t} \quad (40)$$

where

$$\begin{aligned} \lambda_{New}^{Phase} = & 2N\lambda^{SM} + (2M+1)\lambda_{Thyristor}(ON) \\ & + 2N\lambda_{Thyristor}(OFF) + 2\lambda_{Inductor}. \end{aligned} \quad (41)$$

In order to have a healthy system, three phases of the converter should perform properly. Therefore, the reliability function of the proposed configuration is as follows:

$$R_{New}(t) = (R_{New}^{Phase}(t))^3 = \left[\sum_{i=0}^{2M} \frac{(\lambda_{New}^{Phase}t)^i}{i!} e^{-\lambda_{New}^{Phase}t} \right]^3 \quad (42)$$

D. Case Study

The reliability models of MMC and proposed configuration consist of several factors and parameters. Some of these factors are related to installation and environment. Some other, however, are related to the operational conditions such as voltage stress on devices, current amplitude, power loss, and junction temperature. In order to compare the reliability of MMC and proposed configuration, it is required to conduct the study on specific cases. For this purpose, a system with 20 SMs and detailed parameters listed in Table I is considered. The operating voltage of SMs is 1.65 kV. Considering the rated power and current, Infineon FF450R33T3E3 IGBT module is selected. Using the reported data in datasheet of the selected module, the failure rates of IGBTs and diodes can be calculated according to Table II. Obtained results in this table illustrate that power loss of lower IGBT is significantly larger than the upper ones which resulted in larger failure rate. The power loss of the upper diode, also, is larger than the lower one. However, the failure rate of diodes is much lower than the failure rate of IGBTs. For SM capacitors, also, the AVX film capacitor produced by Kyocera company with the voltage rating of 1950 V is chosen [19]. According to (24) and considering 85 °C as the temperature of hot spot point, the base failure rate of capacitor will be 2.45

TABLE II
FAILURE RATE CALCULATION PARAMETERS FOR IGBT AND DIODE

	IGBT	Diode
λ_{base} (FIT)	0.74	1
π_s	0.212	0.185
π_R	192.1	-
π_Q	1	1
π_E	6	6
π_C	-	1
π_A	0.7	-
R_{thJC}, R_{thCH} (K/kW)	28.4, 17.4	45.5, 19.3
$T_{heat-sink}$ (°C)	80	80
$P_{conduction}^{upper}, P_{conduction}^{lower}$ (W)	112, 297.1	76.4, 10.8
$P_{OFF}^{upper}, P_{OFF}^{lower}$ (W)	54.6, 192	198.3, 78
$P_{ON}^{upper}, P_{ON}^{lower}$ (W)	58.9, 216.8	-
$P_{Loss-Total}^{upper}, P_{Loss-Total}^{lower}$ (W)	225.5, 705.9	274.7, 88.8
T_J^{upper}, T_J^{lower} (°C)	90.31, 112.33	97.8, 85.7
$\pi_T^{upper}, \pi_T^{lower}$	3.58, 5.01	7.7, 5.8
$\lambda^{upper}, \lambda^{lower}$	453.3, 631.9	8.5, 6.4

TABLE III
FAILURE RATE CALCULATION PARAMETERS FOR THYRISTOR

	TV(OFF)	TV(ON)
λ_{base} (FIT)	2.2, 2.2	2.2, 2.2
π_s	0.284, 0.284	0.284, 0.284
π_R	0.3, 0.3	8.67, 5.62
π_Q	1, 1	1, 1
π_E	6, 6	6, 6
R_{thJC} (°C / W)	0.078, 0.078	0.078, 0.078
R_{thCH} (°C / W)	0.02, 0.02	0.02, 0.02
$T_{heat-sink}$ (°C)	70, 70	70, 70
$P_{conduction}^{Thyristor}$ (W)	0, 0	511.4, 146.5
$T_J^{Thyristor}$	70, 70	120.1, 84.4
$\pi_T^{Thyristor}$	3.9, 3.9	12, 5.7
$\lambda^{Thyristor}$	4.4, 4.4	391.4, 120.5

FIT. Applying $\pi_Q^{Cap} = 1$, $\pi_E^{Cap} = 4$, and $\pi_B^{Cap} = 5$, the failure rate of capacitor will be 49.1 FIT. Substituting calculated failure rates into (28), the failure rate of SM is equal to 1149.2 FIT.

The Infineon TZ240N thyristor module, also, is selected to be used in this application. As it is mentioned earlier, 2N thyristor valves always are OFF at the both configurations. According to the characteristics of the selected thyristor and the considered case study, the failure rate of these thyristors is 4.4 FIT. Therefore, the failure rate of OFF thyristor valve is 8.8 FIT. The ON thyristor valves, however, are conducting the arm currents. The important point here is that arm current has a dc content. Therefore, the positive cycle is larger than the negative cycle. Since the positive cycle is passing through one thyristor, and the negative cycle is passing through the reverse parallel thyristor at the same thyristor valve, the conduction loss and current factors of them would be different. As it can be seen in Table III, two current factors are reported for the ON thyristor valve, which the larger one is related to the thyristor that conducts the positive cycle. The conduction losses, junction temperatures, temperature factors, and accordingly, their failure rates are different according to Table III. It is worth to note that only $2M$ thyristor valves in conventional MMC, and $(2M + 1)$ thyristor valves in

the proposed configuration are ON, and remaining $2N$ thyristor valves are OFF in each phase. On the other hand, almost 10% of submodules are RSMs in high-power MMCs. Therefore, the IGBTs have the dominant influence on the system reliability.

Fig. 4 illustrates the reliability behaviors of MMC and proposed configuration with 5% ($M = 1$), 10% ($M = 2$), and 15% ($M = 3$) RSMs. The red curves are related to the MMC configuration and the green curves are related to the proposed configuration. In Fig. 4(a), MMC with one RSM per arm is compared by the new configuration with $2M = 1$ and $2M = 2$. According to the obtained results, the reliability of conventional configuration at the end of the first, second, and third year of operation are 89.26%, 66.58%, and 43.59%, respectively. The corresponding values in the proposed configuration, however, are 97.40%, 85.26%, and 65.80%. The expected lifetime of the systems, also, can be represented by B1 and B10 factors. As it can be seen in Fig. 4(a), the B1 factor for MMC is 2.492×10^3 h and its B10 factor is 8.419×10^3 h. For the proposed configuration, however, B1 is 6.171×10^3 h and B10 is 1.485×10^4 h. Obtained results demonstrates a remarkable improvement on the expected lifetime by the proposed configuration. In the second case, the MMC with two RSMs per arm ($M = 2$) is compared by the proposed configuration with $2M = 2$, $2M = 3$, and $2M = 4$. As it can be seen in Fig. 4(b), the reliability of the proposed configuration with $2M = 3$ is higher than the reliability of MMC with $M = 2$ which means that more reliable system is achieved by lower number of RSMs. Comparing the MMC with $M = 2$ and proposed configuration with $2M = 4$, also, confirms the superior reliability and lifetime of the proposed configuration. This process is replicated for $M = 3$, and the results are shown in Fig. 4(c). Reliability of first three years of operation as well as expected lifetime of both configurations are listed in Table IV.

It is clear that the obtained results are depended on the system parameters and selected components (see Tables I and III). Even though changing these parameters can change the reported results in Table IV, the final conclusion that the proposed configuration improves the reliability and expected lifetime of MMC is still effective. In fact, changing the system parameters and components only changes the failure rate of SMs which is identical for both configurations. However, the difference among these configurations originates from their reparability, which is in the arm level (according to (39)) or in the phase level (according to (42)). In order to illustrate the effect of changing system parameters, the reliability models are drawn in Fig. 4(d) for 30% tolerance in λ^{SM} and $M = 2$. Obtained results from this simulation is summarized in Table V. As it can be seen, the proposed configuration has improved the reliability and lifetime of system in various failure rate. Indeed, obtained results shows that the improvement of B1 and B10 factors, and accordingly the lifetime of system, are almost independent of the failure rates.

V. SIMULATION RESULTS

In this section, the proposed configuration is simulated to analyze its electrical waveforms and validate its functionality.

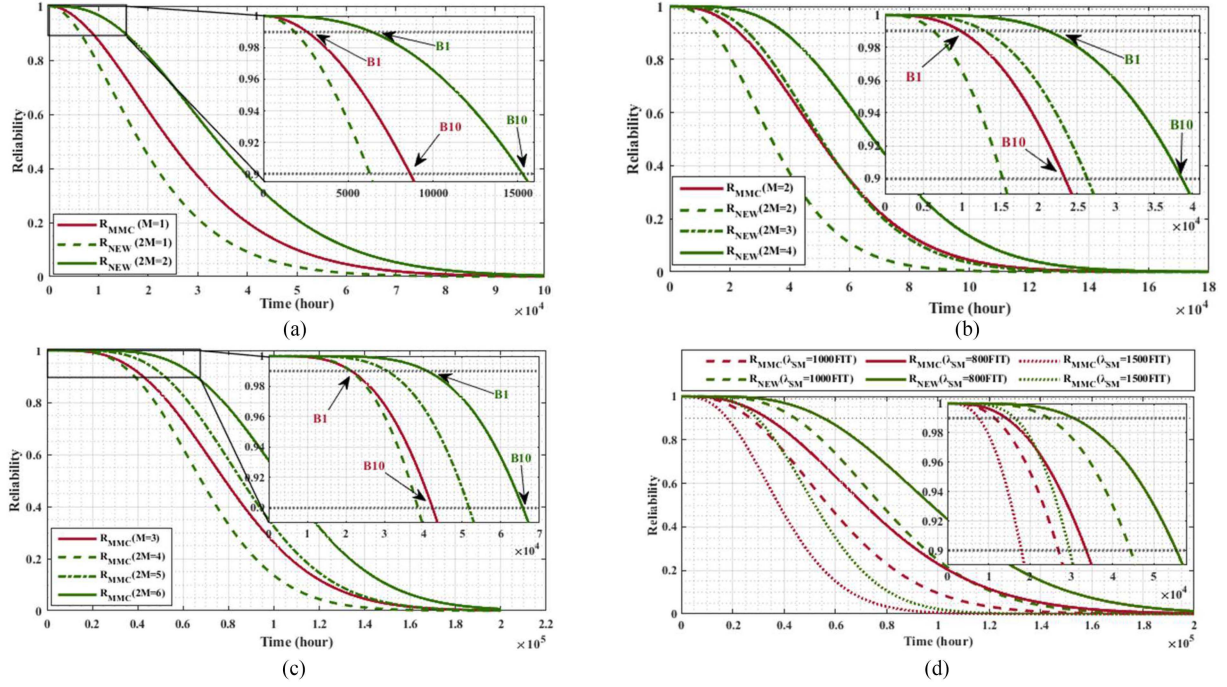


Fig. 4. Reliability behavior of the conventional MMC (red curve) and the proposed configuration (green curve). (a) $M = 1$; (b) $M = 2$; (c) $M = 3$; (d) various failure rates. B1 and B10 are the time-periods that the reliability of system drops from 1 to 0.99 and 0.9, respectively.

TABLE IV
RELIABILITY AND LIFETIME OF MMC AND PROPOSED CONFIGURATION FOR VARIOUS NUMBER OF REDUNDANCIES

	MMC			Proposed Configuration			Improvement (%)		
	$M = 1$	$M = 2$	$M = 3$	$M = 1$	$M = 2$	$M = 3$	$M = 1$	$M = 2$	$M = 3$
Reliability after one year	0.8926	0.9919	0.9999	0.9740	0.9997	0.9999	8.14	0.78	0
Reliability after two years	0.6658	0.9457	0.9938	0.8526	0.9945	0.9998	18.68	4.88	0.47
Reliability after three years	0.4359	0.8497	0.9737	0.6580	0.9710	0.9988	22.21	12.13	2.51
B1 ($\times 10^3$ hour)	2.492	9.445	20.000	6.171	20.235	38.280	59.61	53.32	47.75
B10 ($\times 10^3$ hour)	8.419	22.233	39.445	14.849	36.663	61.176	43.30	39.35	35.52

TABLE V
RELIABILITY AND LIFETIME OF MMC AND PROPOSED CONFIGURATION FOR VARIOUS FAILURE RATES

	MMC			Proposed Configuration			Improvement (%)		
	800	1000	1500	800	1000	1500	800	1000	1500
Failure rate of SM (FIT)	800	1000	1500	800	1000	1500	800	1000	1500
Reliability after one year	0.9972	0.9943	0.9822	0.9999	0.9998	0.9991	0.27	0.55	1.69
Reliability after two years	0.9801	0.9610	0.8891	0.9989	0.9968	0.9824	1.88	3.58	9.33
Reliability after three years	0.9407	0.8887	0.7190	0.9937	0.9824	0.9170	5.3	9.37	19.8
B1 ($\times 10^3$ hour)	13.695	10.692	7.281	29.339	22.911	15.606	53.32	53.33	53.34
B10 ($\times 10^3$ hour)	32.235	25.172	17.148	53.158	41.511	28.274	39.36	39.36	39.35

For this purpose, a three-phase system is considered with 20 operational SMs in each arm ($N = 20$), and 4 shared RSMs in each phase ($2M = 4$). The detailed parameters of the simulated system are listed in Table I. In the modulation unit, the phase shift pulse width modulation method is implemented. This unit determines the number of SMs that should be inserted into the circuit. Then, similar to [8]–[10], the sorting algorithm sorts the capacitor voltages in each arm and generate ON/OFF signals for the SMs based on their capacitor voltage level and arm current direction. After the fault occurrence, the faulty SM should be bypassed and a cold-RSM should be inserted to the faulty arm. Closed-loop control on capacitor voltages based on

sorting technique, and a circulating current controller based on proportional resonant (PR) controller [20] is utilized to control the system.

The proposed configuration with $2M = 4$ can handle four faults in each phase regardless of the fault location, while the conventional MMC can handle only two fault in each arm. To bold this feature, four faults are applied to the upper arm of phase A. Fig. 5 illustrates the simulation results. In the first section ($t < 0.4$ s), system is in the normal condition. Hence, T_1^j to T_{40}^j are OFF and T_{41}^j to T_{45}^j are ON. At $t = 0.4$ s, the first fault is applied to the upper arm of phase A. Once the fault is detected, the corresponding thyristor valve of faulty SM is

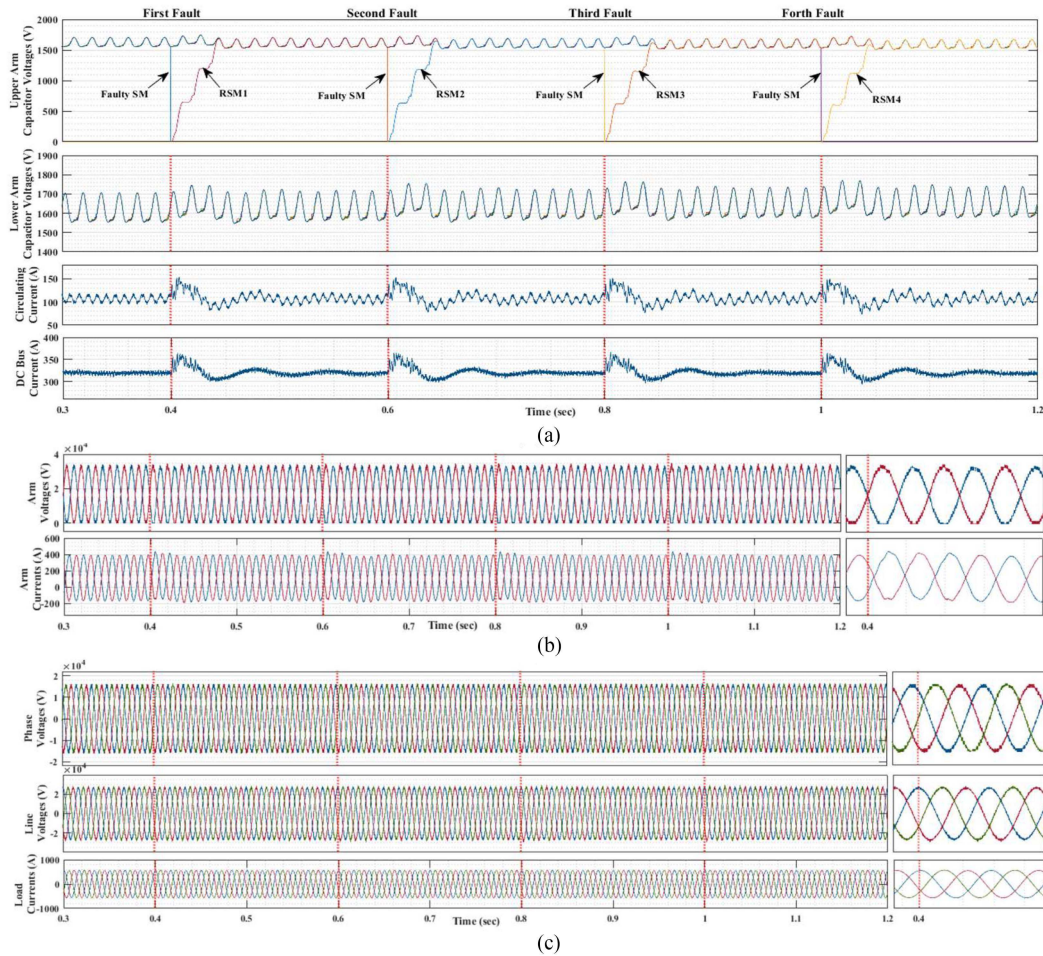


Fig. 5. Simulation results of the proposed configuration with ($N = 20, 2M = 4$). (a) Capacitor voltage of SMs and RSMs in upper arm of phase A, capacitor voltage in lower arm of phase A, circulating current of phase A, and dc bus current. (b) Upper and lower arm voltages and currents. (c) Phase-to-neutral voltages, line-to-line voltages, and load currents.

turned ON and T_{41}^a is turned OFF. By doing so, the faulty SM is bypassed and the first shared RSM is inserted into the upper arm of phase “a.” As it can be seen, the voltage of faulty SM is dropped to zero and first RSM has started to charge. For the other faults, a same process is implemented. Comparing the obtained results in this simulation with the reported results in [8]–[10] confirms that the performance of the proposed configuration is same as the conventional MMC with cold-RSM strategy regarding voltage and current waveforms using same modulation and control techniques. However, the proposed converter can handle up to four faults in each phase regardless of fault location while the conventional MMC can handle up to two faults in each arm.

VI. EXPERIMENTAL RESULTS

In this section, the experimental results are provided to verify the performance of the proposed configuration using a three-phase prototype with four operational SMs ($N = 4$), and two shared RSMs in each phase ($2M = 2$). The detailed parameters of the experimental setup are provided in Table VI. The PS-PWM technique, sorting technique for capacitor voltage

TABLE VI
EXPERIMENTAL SETUP PARAMETERS

Parameter	Value
DC bus voltage	400 V
Number of SMs per arm	4
Number of RSMs per phase	2 ($M = 1$)
Voltage of SMs and RSMs	100 V
Capacitance of SMs and RSMs	3.6 mF
Load impedance	$20 + 6.28j \, \Omega$
Arm inductance	5 mH
Switching frequency	1000 Hz
Modulation index	0.92

balancing, and a PR circulating current controller are implemented in this experiment.

In the normal condition, T_1^j to T_8^j are OFF and T_9^j to T_{11}^j are ON. In order to create fault condition, one SM from upper arm of phase “a” is bypassed and T_9 is turned OFF. As it can be seen in Fig. 6(a), the cold-RSM in this system is charged in almost four cycles. The second fault, also, is applied to the upper arm of phase “a.” After bypassing the faulty SM, T_{10} is turned OFF and second RSM is inserted to the faulty arm. As it can be seen, the converter restores its full performance after the two faults

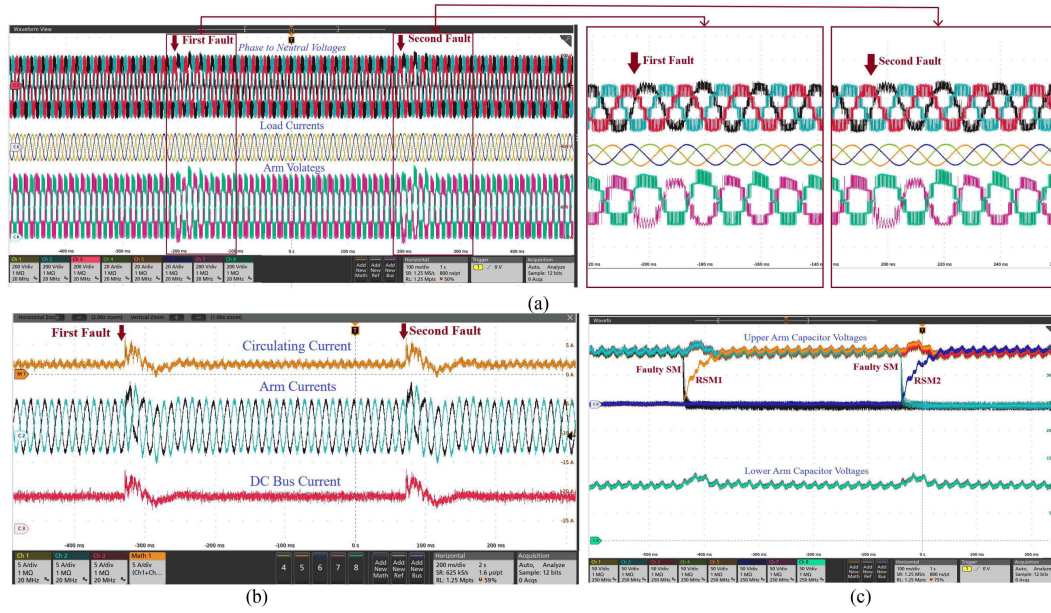


Fig. 6. Experimental result of the proposed configuration with ($N = 4, 2M = 2$). (a) Phase-to-neutral voltages, load currents, and the upper and lower arm voltages of phase A. (b) Circulating current of phase A, upper and lower arm currents of phase A, and dc bus current. (c) Capacitor voltage of SMs and RSMs of phase A.

in upper arm of phase “a.” It is worth to mention that each SM in this system has stored 25% of the overall stored energy in arm. In the larger systems, each SM includes a smaller portion of energy in the arm. In the simulated system, for instance, each SM contains only 5% of arm energy. It is needless to mention that the transient period for restoring 5% is lighter than the transients for replacing 25% of arm energy. The obtained experimental results, also, shows that arm currents are increased after the fault occurrence. The arm voltages and output waveforms, also, have experienced a short transient period to restore the system performance.

VII. CONCLUSION

In this article, a new configuration was proposed for MMC which allows to share the RSMs between upper and lower arms of each phase. Contrary to the conventional MMC, where RSMs in one arm cannot be used in another arm, the proposed configuration makes it possible to share RSMs between both the upper and lower arms of each phase. Regarding operation principle, the modulation and control of the proposed configuration is quite similar to the conventional MMC with cold-RSM strategy. The simulation and experimental results, also, validate the proposed configuration can handle more fault states in each arm using the shared RSMs.

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