GaAs MMIC Interferometer for Broadband Interference Suppression

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***Abstract*— This paper presents a GaAs interference suppression MMIC for integration in broadband receiver front ends. The circuit is an interferrometer, with a gain stage in one path, and a gain stage followed by a variable delay line in the other path. The voltage-tunable delay is implemented with discrete inductors and diode-connected transistors. The total time delay of the second path is adjusted by varying the voltage on the varactors to place a spectral notch at different frequencies across the band. The demonstrated prototype circuit is well matched across X-band and the notch can be tuned from 8.2 to 10.8 GHz. For a CW signal in this band, the circuit shows a 10 dB suppression of interference signals 2 GHz away, and over 11 dB suppression for 3 GHz separation. Broadband suppression at the front end can improve the useful dynamic range of digital cancellation.**

***Keywords*— Interference suppression, GaAs, MMIC.**

I. Introduction

Self and external interference in broadband analog receivers can overload the analog to digital converter (ADC) and is difficult to cancel digitally when the RF bandwidth is large [1]. An overview of self interference in full-duplex (simultaneous transmit and receive) front ends, and some possible solutions for mitigating self interference are given in [2]. Tapped feedback paths in both the analog and digital domains can be used, with a specific example in [3], where a part of the transmit signal is tapped off, adjusted in magnitude and phase, and then recombining with the received signal. This approach was also used in RFIDs [4]. Multiple taps or delay lines analogous to FIR filters are shown in [5], [1], [6] and use 2, 3, and 16 taps, respectively. Since directly tapping of the outgoing signal is required, this type of solution only applies to self-interference cancellation.

For out-of-band fixed-frequency interfering signal suppression, static filters are often used, while a possible solution for variable unwanted signals are electronically-tunable passive filters, with an overview in [7] and examples in e.g., [8], [9]. These filters, however, can be lossy at higher frequencies, and bulky at lower microwave frequencies. A circuit architecture that can be used for cancelling external interference is shown in [10] as it does not directly tap the outgoing signal. Rather, feed-forward auxiliary paths filter out the pre-determined desired signal and then amplify and time delay the interfering signal before combining it with the main path, thus suppressing the unwanted signal. This demonstration is tunable but only over a narrow range from 874.1 to 884.4 MHz with a 2-MHz wide

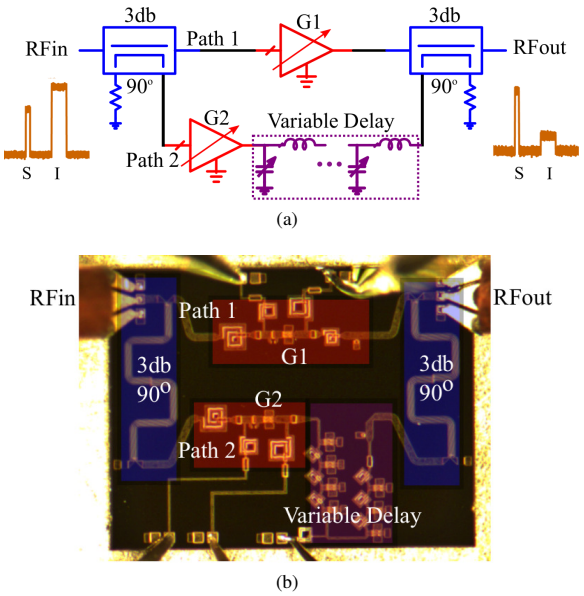


Fig. 1. (a) The block diagram of the interferometer designed to provide a tunable spectral notch. (b) Photograph of the final GaAs MMIC chip with corresponding areas to the block diagram colored. The total chip area is 3.8 mm × 2.9 mm.

20 dB deep notch. The need for adaptive circuits is an area of growing interest for full duplex systems, e.g. [1], [5]. An example of analog adaptation is shown in [11].

In this paper, we present an analog broadband interference suppression GaAs MMIC based on an active interferometer architecture. The block diagram and photograph of the MMIC are shown in Fig. 1. This architecture applies to a general signal, and covers a wide RF bandwidth, in this case 8–12 GHz, creating a spectral notch at the unwanted signal carrier frequency. The notch is tunable with a small range of control voltage. The circuit can be placed after an LNA in a receiver without degrading the noise figure while contributing gain. Suppression of an interfering signal can help optimize the useful dynamic range of the ADC, and therefore improve digital cancellation. If the interfering signal is too large, the ADC will saturate [6]. One the other hand, if it is too small, only a part of the dynamic range of the ADC will be used. Therefore, including variable gain in both paths of the circuit in Fig. 1 can assist digital signal cancellation over a wide RF bandwidth, providing improvements in dynamic range.

II. Tunable Active Notch Circuit Design

The tunable active notch is designed on WIN Semiconductors' GaAs enhancement (E) mode single-polarity supply PIH10 process with a final size of 3.8 mm by 2.9 mm. The circuit is an interferometer in which the input signal is split into two paths that are recombined after analog processing. Path 1 in Fig. 1 is a variable gain stage, while Path 2 consists of a variable gain stage followed by a variable delay line implemented with discrete inductors and diode-connected HEMTs with drain and source terminals grounded. When the signals in the two paths are 180° out of phase, destructive interference results in a transmission null. The final MMIC implementation is shown in Fig. 1a with each area is highlighted in the same color as in the block diagram of Fig. 1b. This front-end circuit is intended to be placed after the LNA and before downconversion.

Folded Lange couplers with isolated ports terminated in 50Ω are used as the splitter and combiner. For a small footprint and operation over the 6–12 GHz octave, the Lange couplers are folded as shown in the layout of Fig. 1b. When folding the coupled-line sections, a phase unbalance occurs, which is compensated by varying the length of the coupled lines close to the ports. Fig. 2 shows the simulated performance before and after compensation.

Both gain stages are conjugately matched in small-signal operation and use 4x75μm transistors which are chosen as their output impedance is well matched to the variable delay line over bandwidth and over control voltage. The drain supply voltage is 2 V. The gate bias voltages are set to obtain a gain value that compensates for the additional loss of the tunable variable delay line. In both simulation and measurements, the gate voltage of Path 1 is 0.8 V and that of Path 2 is 1 V. The variable delay line in Path 2 (purple in Fig.1), consists of seven 4x75 μm transistors, and 6 spiral 0.4-nH inductors. The transistors are chosen for their large variation in capacitance with a small footprint, while the inductor size is determined by the 50Ω desired line impedance. Additional lines and capacitors help match the output of the gain stage and achieve the desired phase difference between the two paths.

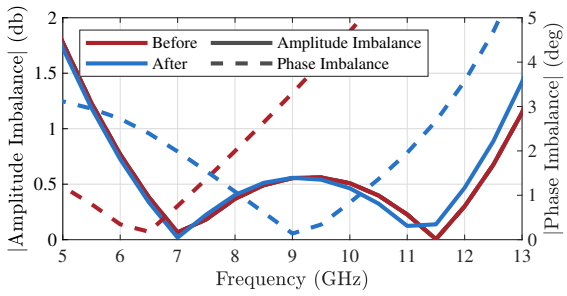
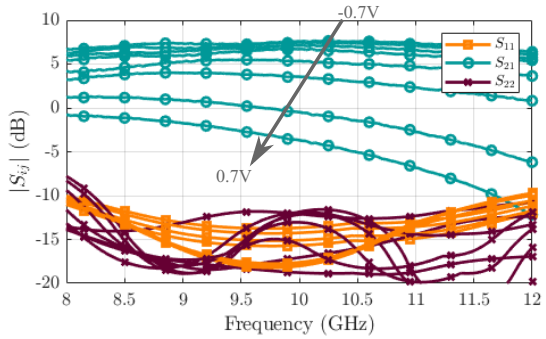
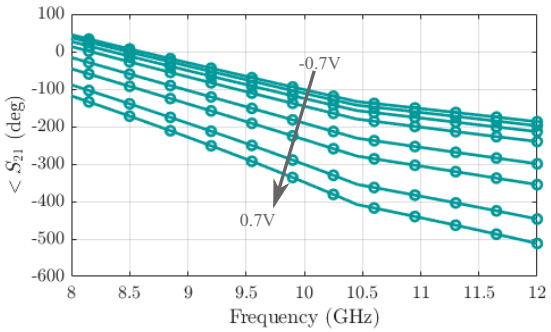


Fig. 2. Simulated folded Lange coupler amplitude (solid) and phase (dashed) imbalance before (red) and after compensation to account for folding (blue).



(a)



(b)

Fig. 3. (a) Measured magnitude of S parameters and (b) angle of S_{21} of Path 2. The control voltage V_c is increased from -0.7 to 0.7 V (in the direction shown by the arrow) with the gate voltage at 1 V and the drain voltage at 2 V.

III. Simulated and Measured Performance

A separate Path 2 circuit, which includes gain stage G2 and the variable delay line, is fabricated and characterized first to assess how the nonlinear model predicts diode-connected transistor behavior. With a gate voltage of 1 V and drain voltage of 2 V, the delay line control voltage is varied from $V_c = -0.7$ to $+0.7$ V. The measured S parameters are shown in Fig. 3, plotted with control voltage varied in $\Delta V_c = 0.2$ V steps. The input and output match of the line stays well matched with $|S_{11}| < -9.8$ dB and $|S_{22}| < -8.0$ dB across the entire 8–12 GHz range. The transmission gain is above 5 dB for most control voltages and drops above $V_c = 0.3$ V when the transistors approach turn-on, shunting a part of the RF signal to ground. The measured $\angle S_{21}$ is plotted in Fig. 3(b) and increases with control voltage, allowing for adjustment of phasing between Paths 1 and 2, thereby tuning the frequency of the notch.

It is interesting to compare the simulated performance, since the nonlinear transistor model is not extracted for varactor simulations. Fig. 4 shows the agreement between simulations and measurements of the transmission coefficient magnitude and phase for the two extreme control voltages. Note that the trend is well predicted, but the absolute values differ and show more phase variation in measurements, as well as increased gain variation. The simulated return loss remains below 8 dB and is slightly higher than in measurements in the center of the band.

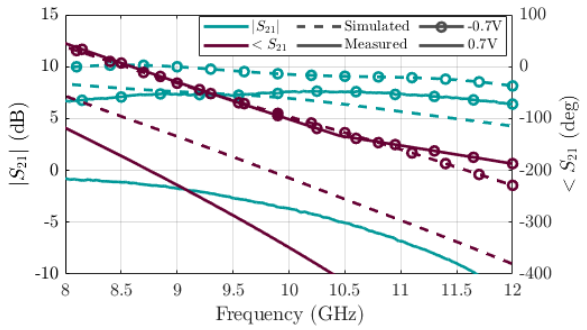


Fig. 4. Simulated (dashed) and measured (solid) transmission coefficient range for the extreme values of the control voltage.

The results of full interferometer circuit simulations and measurements are shown in Fig. 5(a) and (b). For both cases, the drain voltage is set to 2 V, and the Path 1 and Path 2 amplifier gate bias voltages are 0.8 V and 1 V, respectively. The input and output match closely agree between simulations and measurements and remain below -16 dB and -12 dB across the 6–12 GHz octave due to the Lange couplers, however the notch tuning is somewhat narrower and covers X band. The 6–8 GHz range is not plotted to better present the notch data over frequency. There is a shift of about -0.4 GHz in the measured vs. simulated notch tuning with control voltage, namely 10.8–8.2 GHz vs. 11.3–8.5 GHz. The depth of the notch is shallower in the measured case when the same control voltage is used as in the simulations. Simulations show that changing the gate bias voltage can improve the depth of notch in the lower part of the frequency band.

IV. Two-Signal Suppression Tests

Two CW tones at different frequencies and different spacings are used to demonstrate the performance of the interference suppression circuit. In the experiment, two generators with equal output powers are combined with a broadband coupler before the chip input, while the output of the MMIC is measured with a spectrum analyzer, Fig. 6(a). First, the output with two tones at a Δf=2 GHz spacing is measured as a function of control voltage on the variable delay line, with the results for 8.5 GHz and 10.5 GHz shown in Fig. 6(b) in blue and red. Next, tones at 6.5 and 9.5 GHz with a Δf=3 GHz spacing are applied and the output powers as a function of control voltage are shown in yellow and purple. The higher frequencies are more attenuated for negative control voltages, while lower-frequency signals undergo more attenuation at higher voltages. Fig. 7 displays the difference in power levels between the two sets of signals.

The behavior over frequency is shown in Fig.8 when measuring four cases of frequency spacing and control voltage comparing to the previously measured $|S_{21}|$. Four conditions are shown: (a) Δf=2 GHz, V_c=-0.4 V (red); (b), Δf=2 GHz, V_c=+0.4 V (blue); (c) Δf=3 GHz, V_c=0 V (yellow); and (d) Δf=3 GHz, V_c= 0.6 V (purple). The $|S_{21}|$ shows the expected

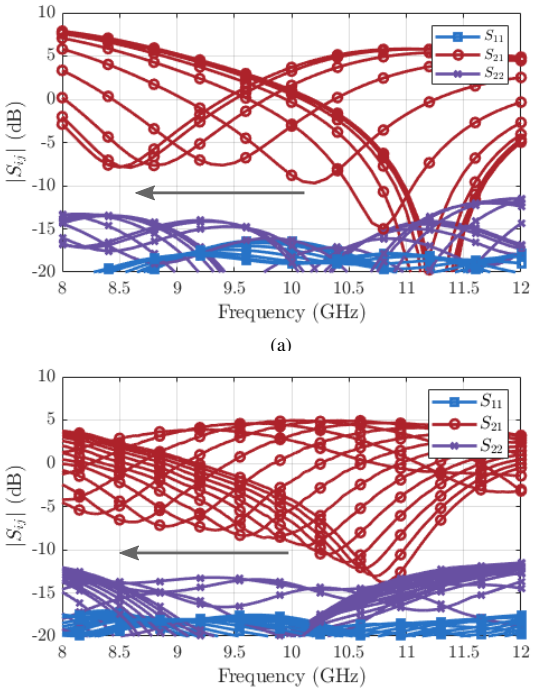


Fig. 5. (a) Simulated and (b) measured S parameters of the interferometer chip. The control voltage for the artificial line is varied from $V_c = -0.7$ V to 0.7 V. As the control voltage, increased, the notch placement goes down in frequency as shown by the arrow. The drain voltage is set at 2 V. The gate voltages on Paths 1 and 2 are 0.8 and 1.0 V, respectively.

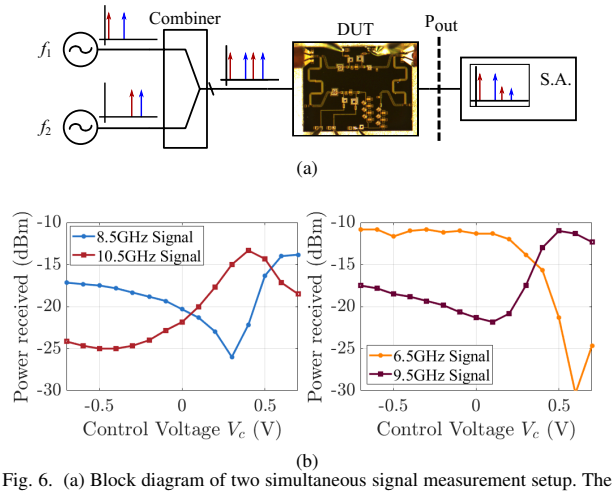


Fig. 6. (a) Block diagram of two simultaneous signal measurement setup. The power is calibrated to the reference plane labeled P_{out} using a "thru" and a power meter. (b) The measured output power for 8.5 and 10.5 GHz (left) and 6.5 and 9.5 GHz CW input signals (right), measured on a spectrum analyzer as the control voltage is varied. The input signal powers are -10 dBm.

trends. The difference in power level is normalized to a "thru" line transmission.

For condition (a), the 8.5 GHz signal has about 1 dB of gain while the 10.5 GHz is about 8 dB lower, while for condition (b), there is gain of nearly 5 dB for the 10.5 GHz signal while

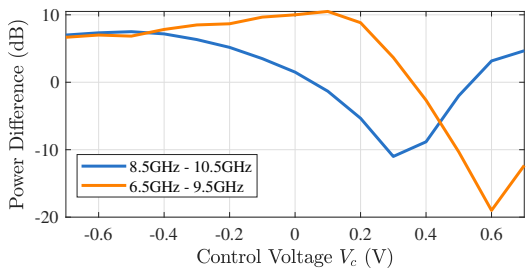


Fig. 7. The difference in output power between 8.5 and 10.5 GHz (blue) and 6.5 and 9.5 GHz CW input signals (yellow), measured on a spectrum analyzer as the control voltage is varied. The input signal powers are -10 dBm.

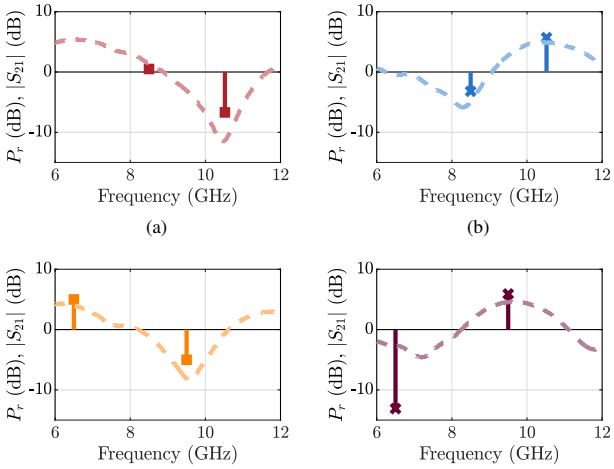


Fig. 8. Measured two-signal power normalized to a "thru" line transmission (vertical bars). Measured $|S_{21}|$ (dashed) plotted for comparison. For $\Delta f = 2$ GHz, two control settings are measured, (a) $V_c = -0.4$ V and (b) 0.4 V. For $\Delta f = 3$ GHz, the control voltages are (c) $V_c = 0$ V and (d) 0.6 V.

the 8.5 GHz signal is about 9 dB lower. For condition (c), the 6.5 GHz signal has 5 dB of gain and the 9.5 GHz signal is 10 dB lower, while for condition (d) the 9.5 GHz signal is at 6 dB of gain and the 6.5 GHz signal is attenuated 19 dB for a value of -13 dB. For a larger Δf, the suppression is larger, as expected. The signal suppression predicted from small-signal measurements differs from the one observed in large signal measurements, especially for condition (d) where the varactor diodes were forward biased close to conduction, although the spurs as measured on the spectrum analyzer are 30 dB lower.

V. Conclusions

An active tunable notch for suppressing interfering signal power is implemented in a single-polarity GaAs E-mode HEMT process for operation between 8 and 12 GHz. The circuit reduces the power of an interfering signal that is 2 or 3 GHz from the desired signal by 9 and 19 dB respectively, while amplifying the desired signal by as much as 6 dB. The circuit is easy to bias and is tunable with a small range of control voltage. The circuit can be placed after an LNA in a receiver without degrading the noise figure while contributing gain. The gain stages in Paths 1 and 2 can also be designed as LNAs, with a 3 dB increase in IP3 compared to a single LNA, and a small penalty in noise figure due to the splitter loss. The topology can be implemented in GaN for higher power handing and better linearity. Adding variable gain stages before the final combiner can help increase the signal suppression.

This architecture applies to a general signal, and covers a wide RF bandwidth. Suppression of an interfering signal can help optimize the useful dynamic range of the ADC, and therefore improve digital cancellation. If the interfering signal is too large, the ADC will saturate [6], while if it is too small, only a part of the dynamic range of the ADC will be used. Therefore, including variable gain in both paths of the circuit in Fig. 1 can assist digital signal cancellation over a wide RF bandwidth, providing improvements in dynamic range.

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