

# A Wireless Implantable Opto-Electro Neural Interface ASIC for Simultaneous Neural Recording and Stimulation

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Recent advances in optogenetics enable optical stimulation that uses light to reversibly control the activity of the genetically targeted specific neurons. Optical stimulation has distinct advantages of cell specificity, high temporal precision, and rapid reversibility, compared to electrical stimulation [1]–[4]. LEDs typically require high instantaneous current in the order of mA level to emit sufficient light for effective optical stimulation. Such a power-consuming function will challenge wireless power transmission. Wireless operation in terms of power delivery and data transmission is highly desired for eliminating tethers, batteries, and limitations during *in vivo* studies. Thus, energy-efficiency optical stimulation circuits are required. In addition, the stimulation-induced artifacts can corrupt neural recording and lead to saturation of sensing frontend (SFE) circuits. Neural interface ASIC for simultaneous neural recording and stimulation requires an SFE that can tolerate large artifacts. Hence, we present a novel wireless implantable opto-electro (WIOE) neural interface ASIC with features of artifact-tolerant SFE, energy-efficient optical stimulation, and wireless and battery-free operation.

Fig. 1. shows the ASIC block diagram and the conceptual view of the wireless WIOE neural interface system for *in vivo* studies on small freely behaving rodents (e.g., rats). The WIOE ASIC together with an Rx coil and passive capacitors are assembled in a headstage device carried by the subject while receiving wireless power through an inductive link operating at 135MHz. Power management circuits rectify received AC power and offer supply voltage & biasing to other circuits. The forward data telemetry recovers stimulation parameters from the OOK-modulated Rx coil voltage,  $V_{COIL}$ . The ASIC employs a novel voltage-boosting switched-capacitor-based stimulation (VB-SCS) structure to drive LED without the need for a supply voltage larger than the LED forward voltage ( $V_F$ ). The ASIC simultaneously records evoked neural activities using a novel  $\Delta\Sigma$ -modulation-based direct digitizing SFE that can tolerate large stimulation artifacts. The Tx backscatter packetizes the digitized recording data and transmits the data packet by OOK modulating the Rx coil. The backscattered data is then recovered by a commercial data Rx.

Constant current stimulation (CCS) and switched-capacitor-based stimulation (SCS) structures have been widely used (Fig. 2). CCS can drive LED with a precision constant current. The large LED current, however, heavily loads the inductive link. SCS can address this issue by charging a storage capacitor and controlling the capacitor dump charges without loading the inductive link. However, CCS and SCS require a supply voltage larger than the LED  $V_F$ . Blue LEDs used for evoking neural activities have  $\sim 3V$   $V_F$ . Thus, we propose a novel VB-SCS structure, which employs series-parallel switched-capacitor topology, to enable optical stimulation with a lower supply voltage. The VB-SCS consists of 6 switches and 2 flying off-chip capacitors. In the charging phase, the two capacitors,  $C_1$  and  $C_2$ , are charged in parallel to the supply voltage,  $V_{SUP}$ . During the stimulation phase, the VB-SCS stack  $C_1$  and  $C_2$ , boosting the LED driving voltage,  $V_{C2}$ , up to  $2 \times V_{SUP}$ . The current limiter sets the upper bound of LED current,  $I_{LED}$ . The stimulation control circuit generates stimulation pulses with adjustable frequency and pulse width. The VB-SCS reduces the required  $V_{SUP}$  by  $2\times$ . VB-SCS facilitates wireless power transmission, LED driving, and technology scaling.

In Fig. 3, a 2<sup>nd</sup>-order  $\Delta\Sigma$ -based direct digitizing SFE with continuous-time (CT)-discrete-time (DT) hybrid architecture is presented. The CT-DT hybrid architecture is implemented using a CT Gm-C integrator and a 6bit 1st-order DT passive noise shaping (NS) SAR [5]. The feedback signal, which is reconstructed by feedback CDAC, is subtracted from the input signal at the input of the Gm-C integrator. Gm-C employs an energy-efficient current-reuse OTA. The four NS capacitors,  $C_{NS}$ , are used to process the residue voltage on the SAR CDAC,  $C_{SAR}$ , and  $C_{NS} = \frac{1}{2}C_{SAR}$ . The NS operation includes two phases. In the residue processing phase ( $\phi_{RES}$ ), four parallel  $C_{NS}$ ,  $4C_{NS}$ , are connected between the top plates

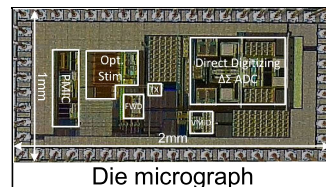
of the two  $C_{SAR}$ . Then the SAR residue voltage,  $V_{RES}$ , is sampled and integrated via charge sharing, resulting in  $V_{INT}$  on  $4C_{NS}$ . In the summation phase ( $\phi_{SUM}$ ), four  $C_{NS}$  and two  $C_{SAR}$  are in series. Then,  $V_{INT}$  is added with the SAR sampled signal,  $V_{SAMP}$ . This NS operation realizes a noise transfer function of  $1-0.8z^{-1}$ . The segment data weighted averaging (DWA) can improve the linearity of the feedback CDAC. The  $\Delta\Sigma$  SFE operation timing diagram shows that upon the sampling period ( $\phi_S$ ) finishes,  $\phi_{SUM}$  starts during which the SAR completes 6 comparison cycles ( $\phi_{COMP}$ ); after the LSB conversion,  $\phi_{RES}$  starts and DWA circuit updates the pointer ( $\phi_{DWA}$ ), followed by the feedback CDAC refreshment ( $\phi_{DAC}$ ).

In the optical stimulation measurements (Fig. 4), VB-SCS connects  $C_1$  and  $C_2$  in parallel to control the voltage doubler charge top places of  $C_1$  and  $C_2$ ,  $V_{C1}$  and  $V_{C2}$ , to  $V_{SUP}$  (i.e., 1.8V) and connects  $C_1$  and  $C_2$  in series when the stimulation starts, resulting in the peak of  $V_{C2}$  equal to 3.6V. VB-SCS delivers current pulses with 2ms pulse width at 2Hz to LED. The current limiter sets the peak  $I_{LED}$  to 8mA, resulting in 10.4mW/mm<sup>2</sup> light intensity. The transient normalized output light (NOL) follows  $I_{LED}$  curve with a small delay. After each stimulation,  $C_1$  and  $C_2$  are recharged back to 1.8V. Fig. 4 also shows the measurements of the  $\Delta\Sigma$ -based SFE. With a 300mVpp, 2.98kHz sinusoidal input, the power spectrum shows a peak SNDR of 70.1dB in a 10kHz bandwidth. The measured amplitude sweep shows a DR of 71.6dB with a full scale of 1.2Vp. These measurements reveal that the proposed  $\Delta\Sigma$ -based SFE can provide 11-bit ENOB and tolerate stimulation-induced artifacts up to 300mVpp.

The functionality of the WIOE neural interface ASIC in wireless power and data transmission setup was fully verified *in vivo* (Fig. 5) on adult Sprague Dawley rats with AAV-mCherry virus injected in their primary visual cortex (V1) to express neurons with light-sensitive ChR2. The headstage prototype consists of a 1.5×1.5cm<sup>2</sup> rigid PCB that carries the ASIC, Rx coil, and off-chip capacitors, as well as a 5×11mm<sup>2</sup> flexible polyimide substrate that carries one blue LED (Cree TR2227TM) and one pad for tungsten electrode assembly. Only the flexible substrate is implanted underneath the skin with the LED attached to the surface of one V1 lobe and the tungsten electrode penetrating into tissue. The rigid PCB is vertically connected to the flexible substrate through mating headers. The Rx coil attached to the backside of the PCB receives wireless power from the Tx coil driven by a class-E PA through the 135MHz inductive link and establishes bidirectional data transmission with the Tx coil via the same inductive link. Under anesthesia, the animal subject received unilateral optical stimulation. The ASIC delivered a current pulse train with 5mA LED current at 1Hz to the LED while recording local field potentials (LFP) from the penetrating tungsten electrode at 0.6mm tissue depth. Digitized LFP data was received wirelessly and recovered by a commercial data Rx for post processing. Compared to the baseline, stimulation evoked LFPs show larger amplitude and longer phase synchronization, indicating the effectiveness of optical stimulation. In transient LFPs, the stimulation artifact appears along with LFPs. The recovered LFP data shows the SFE with wide DR can digitize neural signals while tolerating large artifacts. The WIOE ASIC is fabricated in a standard CMOS 180nm process. Fig. 6 shows the ASIC power and area breakdown and a benchmarking table.

## References:

- [1] G. Gagnon-Turcotte *et al.*, "A 13 $\mu$ m CMOS SoC for Simultaneous Multichannel Optogenetics and Electrophysiological Brain Recording," ISSCC, Feb. 2018.
- [2] S. -Y. Lee *et al.*, "A Programmable Wireless EEG Monitoring SoC with Open/Closed-Loop Optogenetic and Electrical Stimulation for Epilepsy Control," ISSCC, Feb. 2019.
- [3] Y. Jia *et al.*, "A Trimodal Wireless Implantable Neural Interface System-on-Chip," ISSCC, Feb. 2020.
- [4] T. Yousefi *et al.*, "A 12.5mg mm-Scale Inductively-Powered Light-Directivity-Enhanced Highly-Linear Bidirectional Optogenetic Neuro-Stimulator," CICC, Apr. 2020.
- [5] J. Liu *et al.*, "A 40kHz-BW 90dB-SNDR Noise-Shaping SAR with 4 $\times$  Passive Gain and 2nd-Order Mismatch Error Shaping," ISSCC, Feb. 2020.



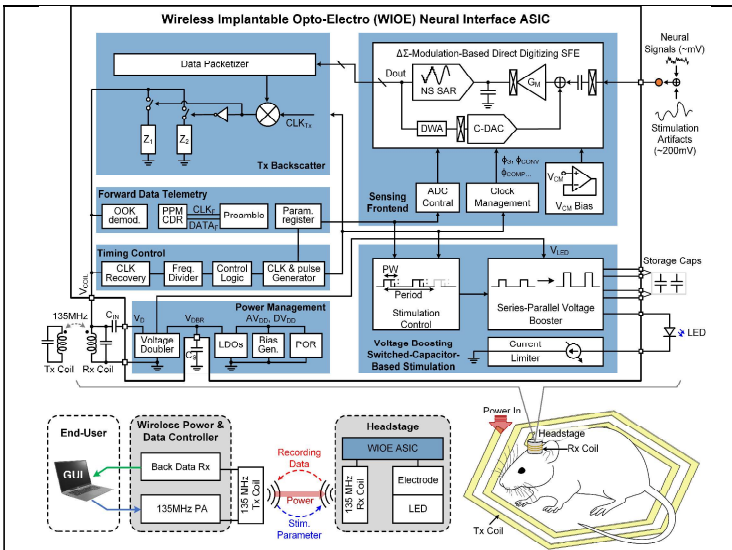


Fig. 1. Conceptual view of the wireless WIOE neural interface system and ASIC block diagram

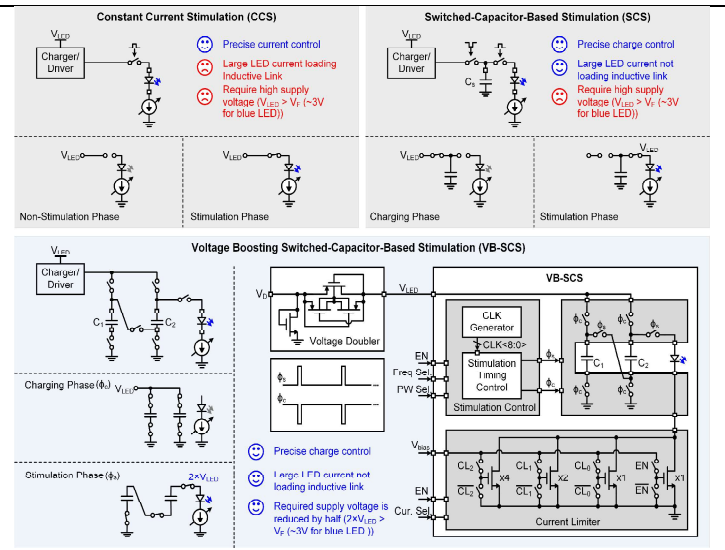


Fig. 2. Prior arts of optical stimulation circuit and proposed voltage-boosting switched-capacitor-based stimulation (VB-SCS)

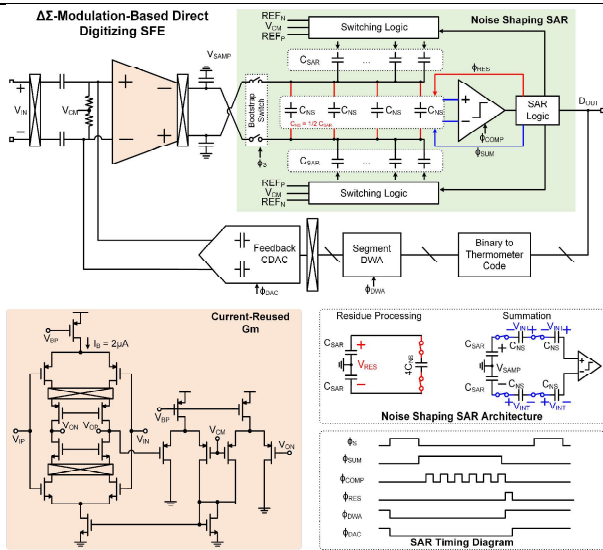


Fig. 3. Architecture and schematic of the proposed  $\Delta\Sigma$ -modulation-based direct digitizing SFE

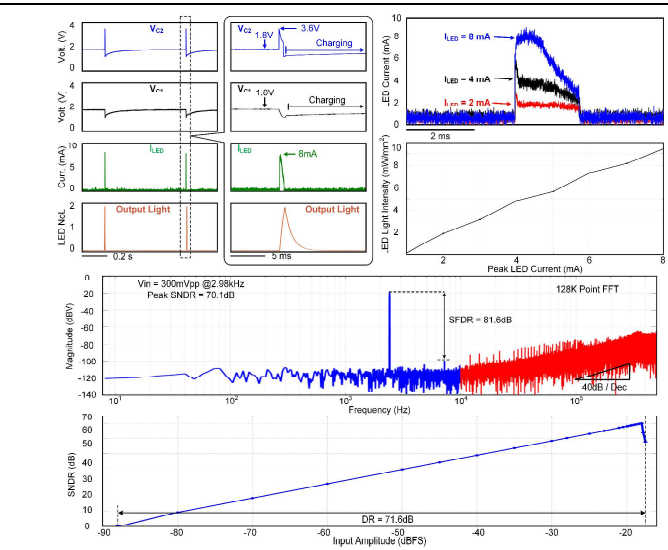


Fig. 4. Measured stimulation waveforms, LED light intensity, output PSD and SNDR versus input amplitude

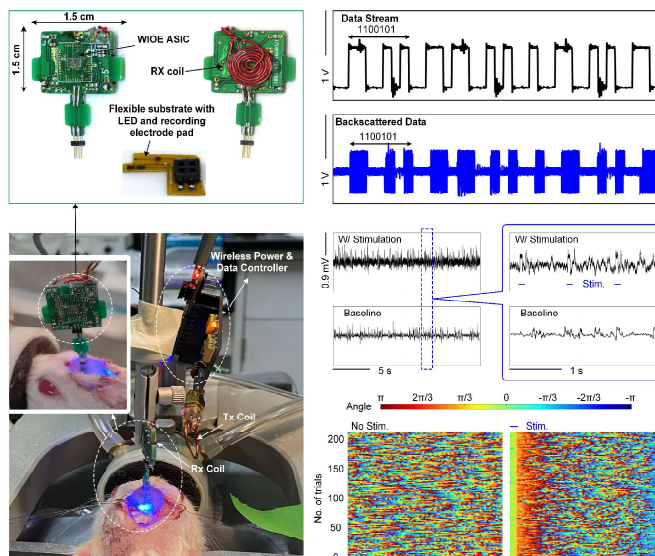
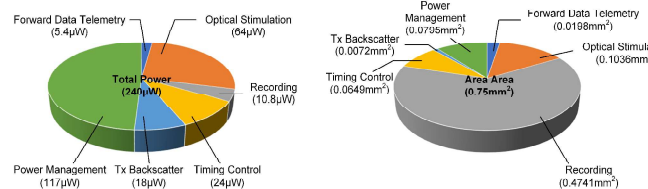


Fig. 5. Measured wireless data transmission waveform, *in vivo* experimental setup and measurement results



|            | References                                | This Work      | ISSCC'18 [1]<br>Gagnon-Turotte | ISSCC'19 [2]<br>Lee  | ISSCC'20 [3]<br>Jia  | CICC20 [4]<br>Youssef |
|------------|-------------------------------------------|----------------|--------------------------------|----------------------|----------------------|-----------------------|
| System     | Technology                                | 180nm          | 130nm CMOS                     | 180nm + CoTg         | 350nm CMOS           | 130nm CMOS            |
|            | Chip Area (mm <sup>2</sup> )              | 2              | 2                              | 13.67                | 25                   | 12                    |
|            | Supply Voltage (V)                        | 1.2 / 1.8      | 1.2                            | 1.2 / 1.8 / 3.3      | 1.8 / 3.3 / 4        | 1.2 / 3.3             |
|            | Power Source                              | Inductive Link | Battery                        | Battery              | Inductive Link       | Inductive Link        |
|            | Wireless Comm.                            | Yes            | Yes                            | Yes                  | Yes                  | No                    |
|            | Total Power (mW)                          | 0.24           | -                              | 0.992                | 21                   | 0.16 <sup>o</sup>     |
| Simulation | Optimization Modality                     | Optical        | Optical                        | Electrical / Optical | Electrical / Optical | Optical               |
|            | Opt. Stim. Topology                       | VBSGS          | CCS                            | Laser Driver         | SCS                  | CCS                   |
|            | Stim. Supply (V) /<br>LED Drive Volt. (V) | 1.8 / 3.6      | 3.7 / 3.7                      | 3.3 / -              | 3.3 / 3.3            | 3.3 / 3.3             |
|            | Max Stim. Current<br>(mA)                 | 8              | 35                             | 0.51 / 120           | 0.75 / 24.8          | 15                    |
|            | Topology                                  | CT-DT ΔFM      | MASH ΔFM                       | Amp / 1 AM           | Amp / SAR ADC        | Amp / SAR ADC         |
|            | Artifact Tolerant                         | Yes            | No                             | No                   | No                   | No                    |
| Recording  | Peak Input (mV <sub>pp</sub> )            | 300            | 5                              | -                    | -                    | -                     |
|            | Power (μW) /<br>Channel                   | 10.8           | 11                             | 20                   | 50                   | -                     |
|            | Supply (V)                                | 1.2            | 1.2                            | 1.2                  | 1.8                  | 1.2 <sup>o</sup>      |
|            | Signal BW (Hz)                            | 10k            | 10k                            | 187.5                | 10k                  | 1k                    |
|            | ENOB                                      | 11.4           | 8.76                           | 9                    | 8.7                  | 6.4                   |

Fig. 6. ASIC power and area breakdown and benchmarking table