Low-Power Process and Temperature-Invariant Constant Slope-and-Swing Ramp-Based Phase Interpolator

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***Abstract*— This article presents a process- and temperature-invariant high-resolution and highly linear low-power phase interpolator (PI) as an enabler for discrete-time spatial signal processors (SSPs) and for various mixed-mode RF transceiver architectures. Using current integration techniques, the proposed PI generates an adaptable constant slope-and-swing ramp signal to achieve significantly lower power suited for multiple antenna elements. Switched-capacitor-based bias generation enables tracking the ramp generator over process, voltage, and temperature enhancing the PI linearity. The 7-bit PI realized in the 65-nm CMOS technology can generate full delay range with a resolution of 4.88 ps at 1.6-GHz input frequency. The PI consumes a power of 503 μW and occupies an active area of 0.021 mm^2 with a jitter of 0.410 ps for a 1.6-GHz operation and measured DNL and INL of 0.52 and 0.52 LSB, respectively.**

***Index Terms*— Baseband time delay, constant slope-and-swing, phase interpolator (PI), pulse width modulation, ramp-rate tracking.**

I. Introduction

THE exponential growth in data rates enabled by the sub-micron CMOS technology leads to terabits-per-sec data communication at significantly lower power consumption. While migrating to a smaller technology node can improve area and energy efficiency, it also increases the likelihood of mismatches and variations in process, voltage, and temperature (PVT), which require extensive digital trimming. Active research in functionality-driven digitally reconfigurable mixed-mode transceivers [1] is increasingly focusing on time-based circuits and systems at millimeter-wave and sub-THz [2], [3] frequencies. Phase interpolator (PI) forms a critical component in these circuits and systems.

PIs have been widely adopted in clock-data recovery circuits [4], [5], out-phasing transmitters [6], fractional phase-locked loops [7], and more recently in discrete-time beamformers [8], [9], [10]. The need for terabits-per-sec data rates leveraging millimeter-wave and sub-THz frequency bands requires fine timing resolution PI at low-power controlling skews per antenna element [11], [12], [13].

The PI linearity depends on both the RC time constant of output current addition circuit and input signal rise time [14]. PI linearity degrades with step input but improves with finite rise time. Thus, the input clock needs to pass through a slew rate generator or a low-pass filter to remove high-frequency contents. PIs can be broadly classified based on current mode logic (CML) and arrayed inverter architectures. The CML-based PI [4], [15], [16] shown in Fig. 1(a) has small output swing that leads to less dynamic power consumption, whereas static power consumption in the slew rate generator and the core circuit still dominates. The nonlinearity due to the current steering DAC is known to limit the overall performance. A fundamental tradeoff in the design of CML-based PI is explained next. The input of CML-based PI with a low-pass filter behaves like a sinusoidal clock. If the inputs to PI are $A\sin\omega t$ and $B\sin(\omega t+\phi)$, where ω is the input clock frequency and A and B are the amplitudes given to two clocks, respectively. The phase interpolated signal can be written as

$$\begin{aligned} V\text{out}(t) &= A\sin\omega t + B\sin(\omega t+\phi) \\ &\approx C\sin(\omega t+\alpha) \end{aligned} \tag{1}$$

where $C = (A^2+B^2+2AB\cos\phi)^{1/2}$ and $\alpha = \tan^{-1}[(B\sin\phi)/(A+B\cos\phi)]$. For $\phi \leq 45°$, $C \approx A+B$ is a constant and defined by the total tail current. Thus, by varying B only, the PI phase shift (α) can be changed. The dependency of PI phase shift on B is linear only over a small input phase difference range and then becomes nonlinear when the difference (ϕ) exceeds 45°. To overcome this issue, cascaded PI structures [15] have been implemented where each stage interpolates input signals with small phase differences leading to more power consumption. Different calibration techniques can avoid linearity issues, however, adding complexity. As shown in Fig. 1(b), the inverter-based PIs [5] vary the drive strengths of complementary MOS devices achieving different rise and fall times at the PI output leading to different delayed outputs. The inverter-based PI is linear over a wider range; however, full rail-to-rail swing at the output causes high dynamic power consumption. Other than that, injection-based PIs [17], [18], [19], [20], [21] have

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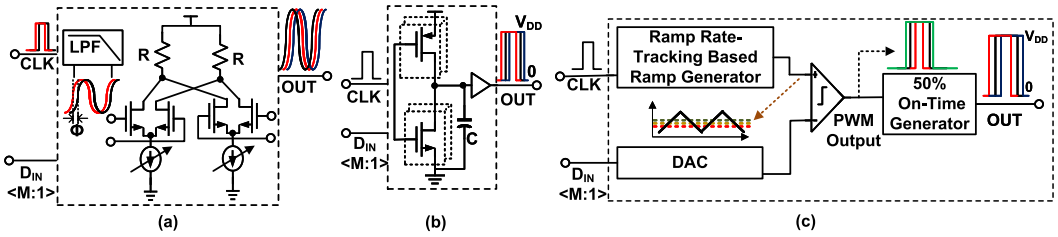

Fig. 1. PI architectures. (a) CML-based PI. (b) Inverter-based PI. (c) Proposed constant slope-and-swing ramp-based PI.

been implemented as phase generators. However, injection-based PIs face issues related to PVT variations. Especially, PI INL/DNL can be reduced when the injection frequency is exactly equal to the free-running oscillator frequency. Thus, it needs extra loops to monitor the frequency properly which is power-hungry.

Mohapatra et al. [10] have demonstrated a constant slope-and-swing ramp-based PI to address both the linearity issue in CML-based PI and dynamic power consumption in inverter-based PI. As shown in Fig. 1(c), I/C integration based on clock input generates a linear ramp signal which gets compared with different DAC levels producing pulse width modulated (PWM) output with different delays. The PWM output is applied to 50% on-time generator creating interpolated clock signal with different delays. The dynamic power is reduced by limiting the ramp swing instead of using full rail-to-rail swing. The ramp generator with ramp-rate tracking in PI ensures a PVT-invariant highly linear constant slope and constant swing ramp signal.

In contrast to [10], this article provides noise and power analysis of the proposed PI architecture with detailed design of PVT-invariant ramp generation. The authors have fabricated the other PI to address design shortcomings such as clock-feed through in the ramp generator, DAC output fluctuation due to input parasitic of the next comparator stage, and higher bandwidth of opamp in ramp-rate tracking in [10] to operate the PI up to 1.6 GHz at a similar power consumption which is 60% higher operating frequency than [10]. The new chip further enables characterizing the noise performance of the PI.

This article is organized as follows. Section II describes the system implementation of the proposed constant slope-and-swing ramp-based PI including the circuit components. Section III presents the noise and power analysis of the PI. Section IV shows a measurement setup followed by Section V illustrating the application of PI in a true-time-delay (TTD)-based discrete-time beamformer. Finally, Section VI describes the conclusions and future works.

II. Proposed Constant Slope-and-Swing Ramp-Based PI

This section presents the architecture of the proposed ramp-based PI. Fig. 2 shows the PI block diagram comprising four main components: 1) resistor-divider-based DAC; 2) CML-to-CMOS converter; 3) ramp generator with ramp-rate tracking; and 4) threshold-based comparator along with a 50% on-time

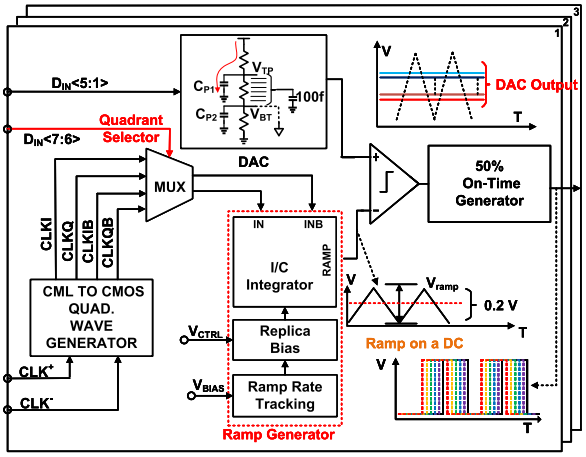

Fig. 2. Top level architecture of the proposed PI.

generator. The following sub-sections expand on the design for each block.

A. Resistor-Divider-Based DAC

As shown in Fig. 2, out of 7-bit PI control signal, 5-bit digital input code (D_{IN}[5:1]) is applied to a low-power resistor-divider-based DAC. It generates 32 reference voltages from V_{TP} (=0.55 V) to V_{BT} (=0.647 V) based on the input code with LSB of 3.125 mV. DAC output gets fluctuated by the parasitic coupling at next-stage comparator's input. To mitigate this fluctuation, a decoupling capacitor of 100 fF has been added at the DAC output. Due to the voltage division by the resistor, the DAC output is affected by the power supply noise. Power supply is periodically fluctuated due to the sudden current drive by loading of PI during transition period of internal nodes. To remove this noise at the operating frequency (1.6 GHz), C_{P1} has been placed at V_{TP}, as shown in Fig. 2. Another capacitor of C_{P2} has been used at V_{BT} to keep that node at AC ground for better power supply rejection ratio (PSRR).

B. CML-to-CMOS Quadrature Wave Generator

As shown in Fig. 3(a), an external 3.2-GHz clock with 0.2-V swing is applied to the CML-to-CMOS quadrature wave generator which generates four quadrature rail-to-rail outputs (CLKI, CLKQ, CLKIB, and CLKQB) with phases (0°, 90°, 180°, and 270°) at half of the input frequency. Frequency divider generating quadrature output is designed by two CML latches. Fig. 3(b) shows the block diagram of CML latch which

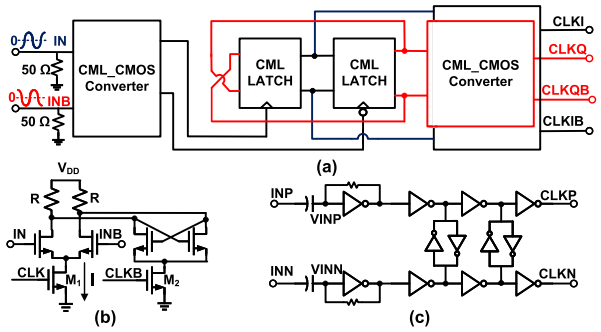

Fig. 3. (a) CML-to-CMOS quadrature wave generator to generate four quadrature outputs for an input signal of 3.2 GHz. (b) CML latch. (c) CML–to-CMOS generator.

generates output from V_{DD} to V_{DD}-IR, where I is the bias tail current and R is the resistor load of the latch. The CML outputs are converted into full rail-to-rail swing by the CML-to-CMOS converter. Then, the rail-to-rail output is applied to the gate of the frequency divider tail current transistors, M_1 and M_2. The divider output passes through the CML-to-CMOS converter which generates four rail-to-rail outputs (CLKI, CLKQ, CLKIB, and CLKQB).

Fig. 3(c) shows the diagram of the CML-to-CMOS converter comprising a series capacitor to avoid loss in the signal swing at the input of the first inverter. The inverter inputs are biased by the resistive feedback and provide gain that easily triggers the output of the first inverter stage. Cross-coupled inverter latch is used between the differential cascaded inverter stages to synchronize and sharpen the quadrature output clock edges.

C. Ramp Generator With Ramp-Rate Tracking

The ramp generator shown in Fig. 4(a) integrates the capacitor current based on the input clock phase. The capacitor voltage ramps up when the input clock is high and ramps down with low input clock. The DC of the ramp signal is V_{CTRL} defined by the replica bias circuit. This integrated capacitor current generates a ramp waveform with a reduced peak-to-peak swing (V_{ramp} = 0.2 V) to ensure minimum dynamic power loss. However, mismatches in both the mirrored current for integration and the capacitor in the ramp generator directly affect the PI linearity. PVT variation of the current and capacitor in the ramp generator leads to the variation in ramp slope (defined as the integrating current over capacitor), which leads to different delays for various PVT conditions. For extreme PVT variation with minimum current and maximum capacitor condition for the integration, the ramp signal swing reduces causing a challenge for the comparator to detect the difference between the PI ramp and the DAC output. To alleviate this issue and make delay invariant across PVT, we propose a ramp-rate tracking with replica bias which ensures that the integrating current is a function of the capacitor.

1) *Ramp-rate tracking* consists of a switched-capacitor-based voltage-to-current (V2I) converter, and a nonoverlapping clock generator is shown in Fig. 4(a). The OTA in the feedback loop, A1, of the ramp-rate tracking ensures that the loop has enough gain across PVT and sets the V_{FB} node to V_{BIAS} with minimum systematic offset. In ϕ_1, C_{BIAS} is connected to V_{FB}. The charge stored in C_{BIAS}

$$Q_1 = C_{BIAS} \cdot V_{FB}. \tag{2}$$

In ϕ_2, C_{BIAS} is connected to GND. The charge stored in C_{BIAS}

$$Q_2 = 0. \tag{3}$$

The total change in charge across a full-time scale: $\Delta Q = Q_1 - Q_2 = C_{BIAS} \cdot V_{FB}$. So the average current flow through V_{FB}

$$I = \frac{\Delta Q}{T} = C_{BIAS} \cdot V_{BIAS} \cdot f \tag{4}$$

where f represents the switching frequency of ϕ_1 and ϕ_2. By observing (4), the current, I, is proportional to C_{BIAS}. The nonoverlapping clock phases for the switched-capacitor circuit, ϕ_1 and ϕ_2, are generated by dividing one of the unused phases of the CML-to-CMOS converter output. The ramp-rate tracking V2I needs to set the current bias only once based on the corner requirement. Once the bias node is set, the current will remain constant for all the PI input codes. Thus, we do not need a high-speed opamp in the ramp-rate tracking circuit. To reduce the bandwidth of the op-amp, the divider with a dividing ratio of 64 is chosen which results in the switching frequency of 1.6 GHz/64 = 25 MHz. Using C_{BIAS} = 100 fF, V_{BIAS} = 0.5 V, and switching frequency of 25 MHz for PI frequency of 1.6 GHz, V2I can generate I = 0.5 V·25 MHz·100 fF = 1.25 μA from (4). This V2I current gets mirrored by 5 to generate a bias current of 6.25 μA. In the ramp-rate tracking sub-block, the second-stage current driver MN_0 is NMOS to keep the input impedance (Z_o) down from the drain of MN_0 high (=$((A \cdot A_0)/(f \cdot C))$), where A_0 is the intrinsic gain of MN_0 and A is the gain of opamp in ramp-rate tracking loop L1. Thus, the gain between gate and source node of MP_0 = 1. This opamp (A1) has PMOS input pair to ensure the node V_{FB} has better PSRR. Therefore, the current generated in V2I has better PSRR. The input pair of opamp is kept in the subthreshold region to have low-power and high gain. Another bias capacitor, C_B (=2 pF), is added to reject the high-frequency switching noise at V_{FB}. Further switching noise mitigation is achieved by the low-pass filter at the gate of MP_0. Here, we have chosen LPF of cutoff frequency = 250 kHz (R = 200 KΩ, C = 3.2 pF) which can reject the noise by 40 dB.

2) *Replica bias* shown in Fig. 4(a) sets the DC level of the ramp signal to V_{CTRL}. The feedback loop (L2) in the replica bias consumes 20 μW. This power consumption is mainly contributed by the opamp (A2) with subthreshold PMOS input pair devices that help in limiting the overall power consumption of the PI. The PMOS input pair ensures the OTA output does not add extra supply noise at the gate of the current integrating PMOS transistor. Based on the bias requirement for the next comparator stage, V_{CTRL} can be tuned to set ramp DC

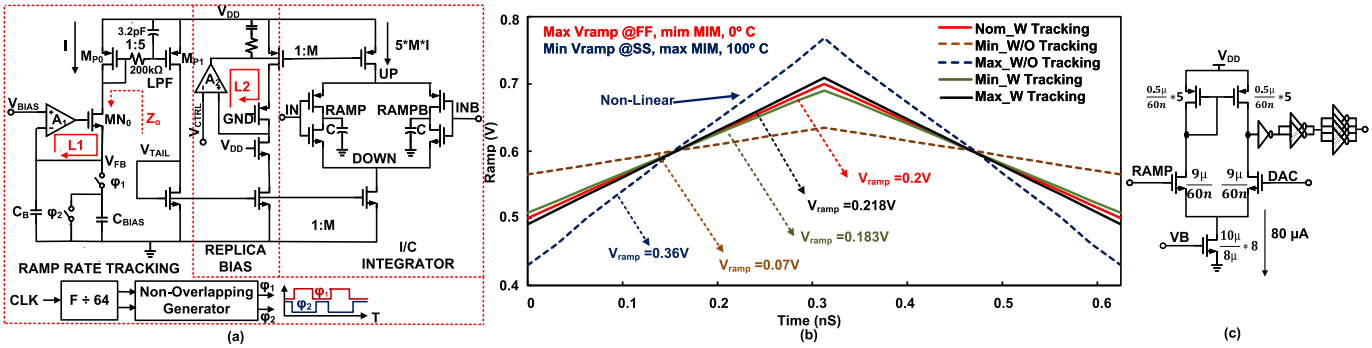

Fig. 4. (a) Proposed constant-swing-and-slope PVT-independent ramp generator with ramp-rate tracking, replica bias, and I/C integrator. (b) Ramp generator output with and without ramp-rate tracking circuit across process corners and temperatures. (c) Circuit schematic of the comparator made of OTA loaded by series of FO4 inverters.

level according to the design requirement (set to 0.6 V in this work). The R in series with C compensation is used to keep the overall L2 loop stable. The replica bias opamp gain has been kept as 60 dB so that the overall loop gain of L2 $\geq$ 80 dB. Thus, systematic offset due to loop gain is less than 0.1 mV.

3) *I/C integrator* multiplies the V2I current from the ramp-rate tracking by M and generates the integrating current of $5 \cdot M \cdot C_{\text{BIAS}} \cdot f \cdot V_{\text{BIAS}}$. Therefore, the ramp slope, S, is expressed as

$$S = (5 \cdot M \cdot C_{\text{BIAS}} \cdot f \cdot V_{\text{BIAS}})/C. \tag{5}$$

Here, $C = 100$ fF is the loading cap of the I/C generator. From (5), S is proportional to C_{BIAS}/C. As both C_{BIAS} and C are implemented using metal–insulator–metal (MIM) capacitors, the effects of PVT variations are alleviated ensuring a constant ratio between them. This is verified by simulation across multiple corners as shown in Fig. 4(b) with the defined nominal RAMP swing, V_{ramp} (=0.2 V). Without the ramp-rate tracking, V_{ramp} varies significantly from 70 mV (SS, 100 °C, maximum MIM capacitor) to 335 mV (FF, 0 °C, minimum MIM capacitor). With the ramp-rate tracking enabled, the signal swing varies from 183 to 218 mV for these two extreme conditions. As observed in Fig. 4(b), for the minimum swing of 70 mV from 0.55 to 0.62 V, many DAC codes (0.55–0.647 V) are missed for comparison to generate the output voltage. Similarly, the maximum swing of ramp from 0.45 to 0.78 V affects the linearity of the swing as the current defining PMOS transistor is affected due to V_{DS} (drain-to-source voltage) variation.

Fig. 4(a) further shows a dummy capacitor on the complementary side of the integrator node, RAMPB for better matching of the differential outputs. Without the dummy capacitor, RAMPB has more swing variation which affects the node UP and DOWN voltages. These nodes do not come back to their original voltages significantly affecting the ramp linearity.

D. Threshold-Based Comparator With 50% On-Time Generator

The threshold-based comparator compares the DAC output with the ramp signal (RAMP) and produces a PWM output with variable delay based on the digital codes into the DAC. Due to unavailability of higher frequency clock signal, a high-speed OTA as static comparator is used. As shown in Fig. 4(c), additional inverter stages have been added in cascade to have high overall gain and faster output response. This high-speed OTA has NMOS input pair with minimum length so that it will have minimum area and does not impact the integrator loading. Minimum length also helps in having higher g_m which ensures the comparator has enough speed and gain with minimum input-referred noise.

The comparator only operates in the mid-region of the ramp signal (from 0.55 to 0.647 V) as shown in Fig. 5(a) to reduce its power consumption. To ensure that the entire ramp range is covered while maintaining the required comparator performance, two differential phases out of the four phases of the CML-to-CMOS output are used for one quadrant operation. Fig. 5(b) shows the selected quadrant for each clock phase. Thus, CLKI is selected for the 1st quadrant (45°–135°), CLKQ for the 2nd quadrant (135°–225°), CLKIB for the 3rd quadrant (225°–315°), and CLKQB for the 4th quadrant (315°–45°). The PWM comparator output does not have fixed pulse width. To make it constant on-time (50%) as shown in Fig. 5(c), the PWM output is divided by 2 by a D-FF to generate frequency ($f/2$) at DIV node where f is the operating frequency of the PI. The divider output passes through a delay stage with delay time, T_d (equal to the PI time period) and generates DIVD. Delay stage is designed by multiple inverters in series which can be tuned through an independent power supply control (V_{DDCTRL}) to keep the delay constant. This T_d defines the ON-time of the final PI output. To have an output of 50% ON-time with frequency f, DIV is XORed with DIVD which generates the final PI output clock, PI_{OUT}.

Fig. 5(a) shows the timing diagram of the proposed PI for two quadrant operations using CLKI (DIN[7:6] = 00) and CLKQ (DIN[7:6] = 01). The figure shows the ramp generator output RAMPI and RAMPQ corresponding to CLK and CLKQ, DAC output, PWM comparator output, and the final PI output, respectively.

The proposed PI is designed to produce well-controlled delays. However, noise, PVT variations, and mismatches introduce timing errors. Detailed noise contributions of each block are discussed in Section III. The ramp generator, DAC, and comparator have been designed such that DNL/INL of PI remains within the required range across PVT. Fig. 6 shows the simulated linearity of the PI covering the entire 360° operation

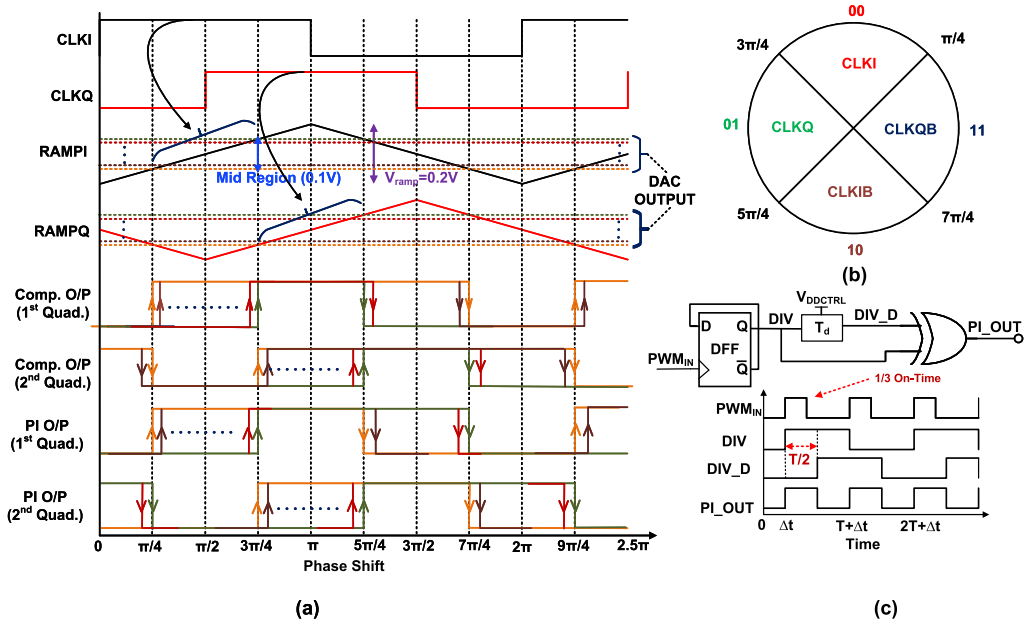

Fig. 5. (a) PI timing diagram for DIN[7:6] = 00, and 01. (b) Quadrant section for the ramp signal input to the comparator using different DIN[7:6]. (c) 50% on-time generator with the timing diagram.

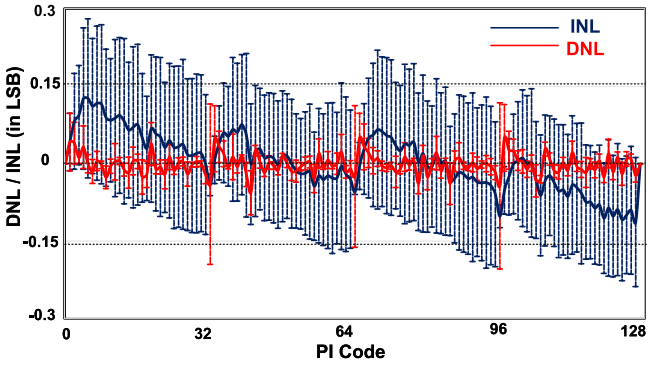

Fig. 6. Simulated DNL and INL for PI covering complete 360° range operating for TT/SS/SF/FS/FF corners, voltage supply 0.95 and 1.05 V and two extreme temperatures (0° and 100°). Red and blue lines show the average DNL and INL, respectively. Dotted lines: deviation from the corresponding average.

across TT/SS/SF/FS/FF corners, voltage supply 0.95 and 1.05 V, and two extreme temperatures (0° and 100°). As per the simulation result, PI has DNL within 0.32 LSB and INL within 0.46 LSB. PI linearity is affected by the mismatch inside the PI block. To quantify the contributions of mismatch in each block on the linearity of PI output, the Monte Carlo simulation with 100 iterations has been performed for four different cases: 1) mismatch in the ramp generator; 2) mismatch in the DAC; 3) mismatch in the comparator; and 4) mismatch in all the PI blocks combined. Maximum DNL (μ, 3σ) of (0.180, 0.078) LSB and INL (μ, 3σ) of (0.258, 0.072) LSB are observed due to mismatch in all the PI blocks combined based on the simulation results. From our simulations, it is observed that out of all the blocks ramp generator contributes the most to mismatch leading to a maximum 3σ variation in DNL and INL of 0.064 LSB and 0.062 LSB, respectively.

III. Noise and Power Analysis

This section analyzes noise and power consumption of different blocks that are important for the design of the proposed PI.

A. Noise Analysis

Fig. 7 shows the diagram of PI with noise contributing sources. The following discussion shows the details of the noise contribution of each block to the PI output.

Noise analysis of the RAMP generator: As shown in Fig. 7(a), the ramp voltage is compared with the comparator's DAC voltage and generates time-delayed output. The noise of node RAMP is going to directly translate to jitter in the time-domain output. The time-domain jitter injected by the voltage-to-time conversion in the comparator needs to be addressed accounting for the second-order effects such as the ramp slope and DAC output. The noise current due to mirror devices M_{1P}, M_{2P}, M_{1N}, and M_{2P} will be represented as $I_{n,1P}$, $I_{n,2P}$, $I_{n,1N}$, and $I_{n,2N}$, respectively, as shown in Fig. 7(a). When the ramp generator output, IN, is ON (i.e., from 0 to T/2, where I is the time period of the RAMP generator output), the noise currents due to the mirror devices (M_{1P}, M_{2P}, M_{1N}, and M_{2P}) are integrated on the capacitor, C, that ramps up the node RAMP. Similarly, when IN is OFF (i.e., from T/2 to T), the noise currents flow out from C ramping down the node RAMP. Note that the noise currents are in addition to the static current ($=5 \cdot M \cdot I$) charging and discharging C. Thus, the average power of the ramp signal can be obtained by integrating the noise signal for each period and dividing the result by the time period [22] and is expressed as

$$P_{\text{AVG}} = \lim_{T\to\infty} \frac{1}{T}\int_0^{T/2} \left[I_{n1}^2(t)\right]dt + \lim_{T\to\infty} \frac{1}{T}\int_{T/2}^{T} \left[I_{n2}^2(t)\right]dt$$

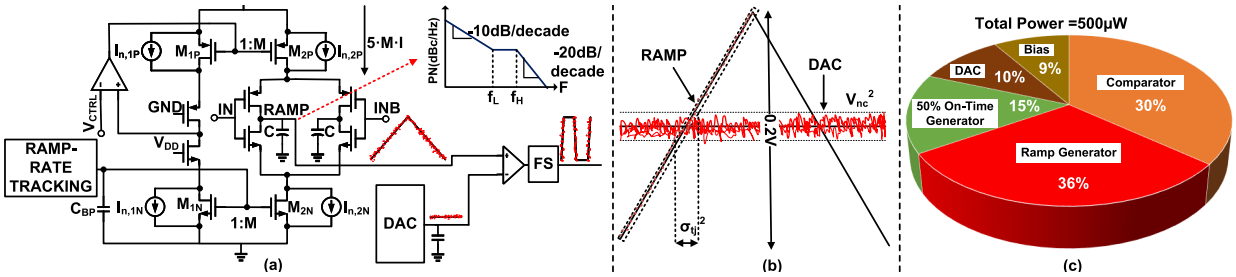

Fig. 7. (a) PI with noise contributing source. (b) Ramp point of crossing and voltage–time noise projection for different slopes. (c) Pie chart showing PI power breakdown: ramp generator and comparator contribute the maximum (66%) of the total power.

TABLE I
COMPARISON WITH STATE-OF-THE ART

Metrics	**This Work**	[4]	[25]	[26]	[27]	[16]	[28]	[7]	[24]	[20]
Arch.	**Const. Slope-Swing Ramp Based**	CML	Inverter based	Edge Interpolation	Charge Based	CML	RC	Current Steering	Integrating	Injection Locking
Tech. (nm)	**65**	65	65	28	40	28	16	65	5	45
Res. (bits)	**7**	4	8	11	12	7	6	5	9	7
Freq. (GHz)	**1.6**	0.5	0.1-1.5	2	2.5	2-11	0.081	0.04	14	3.5-11
DNL (LSB)	**0.52**	0.23	0.52	1.25	0.87	0.5	0.1	0.18	2	0.6
INL (LSB)	**0.52**	0.6	1.33	4.9	3.83	1.1	0.5	0.1	3.47	2.2
Power (mW)	**0.503**	1.508	4.3	19.8	7.1	18.6	0.2	2.3	6	9.5
Power/freq (mW/GHz)	**0.315**	3.16	2.866	9.9	2.84	1.69	2.5	57.5	0.43	1.35
Supply (V)	**1**	1	1.2	1.1	1.1	1	0.8	1	0.75	1.2
Area (mm^2)	**0.021**	N/A	0.06	0.009	N/A	0.022	0.004	0.0055	0.006	0.012

$$= \frac{1}{2} \cdot \lim_{T\to\infty} \frac{1}{T} \int_0^T \left[I_{n1}^2(t) + I_{n2}^2(t)\right] dt$$
$$= \frac{1}{2} \cdot \int_0^\infty \left[I_{n1}^2(f) + I_{n2}^2(f)\right] df. \quad (6)$$

Here, $I_{n1}^2 = I_{n,2P}^2 + M^2 \cdot (I_{n,1N}^2 + I_{n,1P}^2)$ and $I_{n2}^2 = I_{n,2N}^2 + M^2 \cdot (I_{n,1N}^2 + I_{n,1P}^2)$. Here, $I_{n,iP/N}^2 = 4KT\gamma g_{m,iP/N} + K/C_{\text{ox}}WLfg_{m,iP/N}^2$, where $i = 1$ and 2 and P stands for PMOS and N stands for NMOS, respectively.

As shown in Fig. 7(a) for low frequency, the output noise power of ramp decreases by -10 dB/dec which is predominantly dominated by the flicker noise ($1/f$) of M_{1N} and M_{1P}. To have better $1/f$ noise, the device size can be optimized. While maintaining minimum M, a decoupling cap at the gate of M_{1N}, M_{2N}, M_{1P}, and M_{2P} is placed to filter out noise coming from I_{1N} and I_{1P}. This decoupling capacitor improves supply noise rejection. After frequency f_L, the phase noise is going to be 0 dB/dec as thermal noise current of M_{1P} and M_{1N} dominates. For high frequency beyond f_H, due to integrating capacitor C, the slope of phase noise of the ramp generator is -20 dB/dec.

Noise analysis of DAC: Similarly, the resistor mismatch in DAC defines the LSB of DAC and directly impacts the phase noise of PI output as the DAC value defines the PI delay. The mismatch in the resistor is defined by the size of the unit resistor R_u. Resistors are chosen such that the relative mismatch is $\leq$1/2 LSB. The decoupling cap at the output DAC rejects thermal noise at the output.

Noise analysis of comparator: Input-referred noise of the comparator also plays an important role in defining the resolution of the PI. Thus, the input pair of the comparator is kept in the saturation region with high current consumption with minimum L to have maximum g_m and minimum parasitic cap which loads the ramp generator.

Noise analysis of V2I: High-frequency noise due to switching in the V2I block mainly affects the integrating current as its noise is multiplied by M. Primarily this noise causes spurs at the PI phase noise output at the harmonics of switching frequency. It is reduced by a low-pass filter on the mirrored current source of V2I.

By defining the input-referred noise of the comparator, the noise due to DAC and ramp generator as $V_{n,\text{comparator}}$, $V_{n,\text{dac}}$, and $V_{n,\text{ramp}}$, respectively, the total input-referred noise added to the input voltage difference is

$$V_{\text{nc}}^2 = V_{n,\text{comparator}}^2 + V_{n,\text{ramp}}^2 + V_{n,\text{dac}}^2. \quad (7)$$

Assuming the voltage ramp has a time window of Δt with a peak-to-peak swing of 0.2 V as shown in Fig. 7(b), the ramp output and DAC reference are compared with the uncertainty noise V_{nc}^2 as expressed in (7). To simplify analysis further, V_{nc}^2 noise is added on top of V_{DAC}. It is clearly seen that the ramp slope at the point of crossing with V_{DAC} changes with the ramping time ($\Delta T = T/2$) and its voltage span (ΔV) [23]. The ramp slope defines the comparator input-referred noise projection with respect to time error (σ_{tj}^2) which can be expressed as

$$\sigma_{\text{tj}}^2 = V_{\text{nc}}^2/S, \quad \text{where } S = \frac{\Delta V}{\Delta T}. \quad (8)$$

In (8), S is set to 640 MV/s (=200 mV/0.3125 ns) as mentioned in (5). Assuming the comparator has infinite gain through a combination of the opamp and multiple inverter stages, the input-referred time jitter is considered the same as the output final jitter.

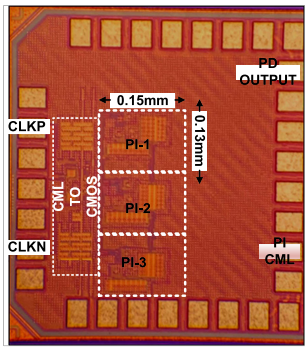

Fig. 8. Chip photograph of the standalone three PIs realized in the 65-nm CMOS with an active area of 0.195 mm^2.

The overall PI noise is defined by the total noise power seen at the input of the comparator (V_{nc}^2) which is a sum of the input-referred noise power of the comparator ($V_{n,\text{comparator}}^2$), thermal noise due to DAC ($V_{n,\text{dac}}^2$), and the noise of the ramp generator circuit ($V_{n,\text{ramp}}^2$). As per the periodic noise simulation, the ramp generator is contributing nearly 75% to the PI output noise. The remaining noise contributions come from the bias circuit, DAC, and final stage including the comparator. To reduce the overall noise of the PI, the size of the current defining transistors of the ramp generator (which are the main contributors to the overall noise) should be optimized.

B. Power Analysis

Fig. 7(c) shows the power consumption breakdown of the proposed PI. Out of 503 μW, the ramp generator (36%) and the comparator consume 30% power. The power consumed by the ramp generator is divided equally between the I/C integrator and the ramp rate tracking circuit. The power consumed in the I/C integrator can be expressed as

$$P_{\text{INT}} = V_{\text{DD}} \cdot 5 \cdot I + C \cdot (0.2\ V_{\text{DD}})^2/12 \cdot f_{\text{PI}} \qquad (9)$$

where f_{PI} is the PI operating frequency. Unlike the inverter-based PIs [5], the dynamic power of the proposed PI is much smaller in comparison to minimal static power consumption. The V2I circuit uses 50 μA including the power in the feedback opamp loop. The comparator power consumption (=150 μW) is set high to ensure it is fast enough to detect minor changes between the DAC and the integrator ramp output. Other contributors include resistive DAC (10%), bias generator (9%), and 50% on-time generator (15%). Other than that the cascaded inverter stages consume dynamic power too.

IV. Measurement Results

The measurement results are reported for two chipsets. In this section, the measured results of the standalone PI are reported followed by the characterization of the PI in a TTD-based four-element discrete-time SSP.

Fig. 8 shows three PIs integrated on the same IC in the TSMC 65-nm CMOS process. PI-1 is used to characterize noise and linearity behavior. The 2nd PI is used to show how much mismatch exists between PIs by the 2nd PI output XORed with the 1st PI output. The 3rd PI is used to test the internal critical node of the ramp generator. Each PI occupies an active area of 0.02 mm^2 (0.156 $\times$ 0.13 mm^2).

As shown in Fig. 9(a), the output (OUT) of PI-1 is XORed with the reference clock (REF) generated from the CML-to-CMOS converter. The XOR output is averaged by an RC low-pass filter (LPF). The averaged DC output after the LPF shows the phase delay between REF and OUT which increases linearly across each code and decreases when the phase difference between the REF and OUT crosses 180°, as shown in Fig. 9(b). XOR gate has enough drive strength for the LPF. XOR gate nonlinearity also affects the PI linearity.

Based on the phase detector output, the PI linearity has been characterized at 1.6 GHz. This experiment is repeated for ten different chips with power supply variation by ±5% from 0.95 to 1.05 V. As shown in Figs. 10 and 11, DNL of 0.52 LSB and INL of 0.52 LSB are observed. The probe station in the laboratory does not have the ability to measure temperature variations. Hence, the post layout simulation results including temperature variation along with the variation in process and voltage are plotted in Fig. 6. Fig. 9(a) also shows a CMOS-to-CML buffer that converts the PI rail-to-rail output into a limited swing output. The buffer is matched with the input impedance (=50 Ω) of the spectrum analyzer. The buffer has 200-mV swing consuming nearly 4-mA current.

Fig. 12 shows the measured phase noise plot of ten PI chips operating at 1.6 GHz. It is observed that the phase noise (PN) varies by −10 dB/dec from 100 Hz to 300 kHz, and 0 dB/dec from 300 kHz to 1 GHz with a frequency spur at 25 MHz, and later due to parasitic capacitance it decays by −20 dB/dec. The noise hump is predominantly seen at 25 MHz due to V2I switching and this hump gets worsened by the parasitic capacitance due to the layout routing between V2I bias and RAMP node. Thus, PI has a maximum of 410-fs jitter integrated from 100 Hz to 10 MHz. Noise can be reduced further by varying the PI bias current. The phase noise is also affected by the CMOS-to-CML buffer due to the noise created by its own resistor and device. From the current value coming out from the power supply V_{DD}, the measured total power is 510 μW.

Table I shows comparison of the PI with other recent works. This PI demonstrates fine time resolution with minimum power/frequency ratio and achieves good INL compared with similar full-scale PIs. The power/frequency ratio is 0.312 which is 27% better than [24] and 4.3× better than [20] with similar or better DNL/INL performance. The measured DNL/INL is comparable to other GHz PIs. Further device scaling can be done to implement a high-speed PI as it will have minimum parasitic for a ramp generator.

V. Application of the PI in Discrete Time SSP

Large-antenna arrays with wide modulated bandwidths require precise time delays to avoid error in coherently combining the beams [29] at the antenna necessitating a TTD

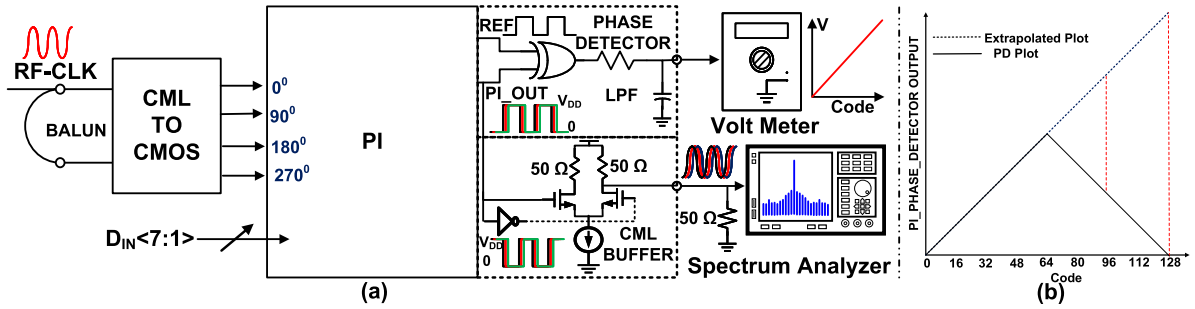

Fig. 9. (a) Measurement setup to calculate the linearity and phase noise of the PI. (b) PD output with extrapolated PD linearity plot.

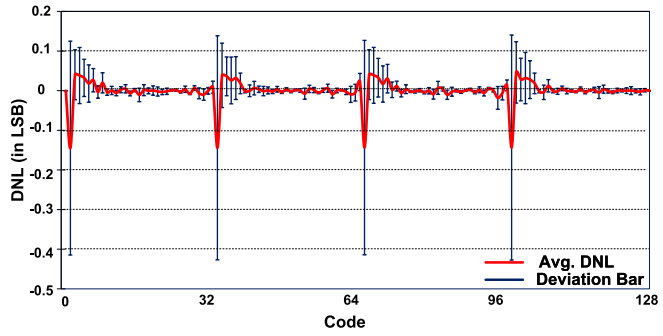

Fig. 10. DNL versus PI code for ten chips with power supply variation by ±5%.

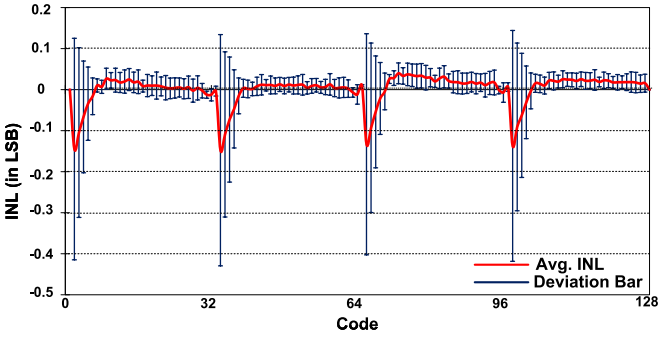

Fig. 11. INL versus PI code for ten chips with power supply variation by ±5%.

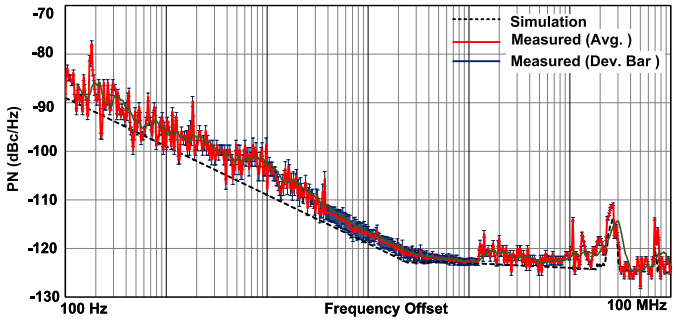

Fig. 12. Measured phase noise plot of the PI operating at 1.6 GHz for ten chips.

implementation. Prior works using delay compensation in RF faced several limitations in linearity, noise, area, mismatch, and delay range. In contrast, delay compensation in digital beamforming consumes significant power due to power-hungry

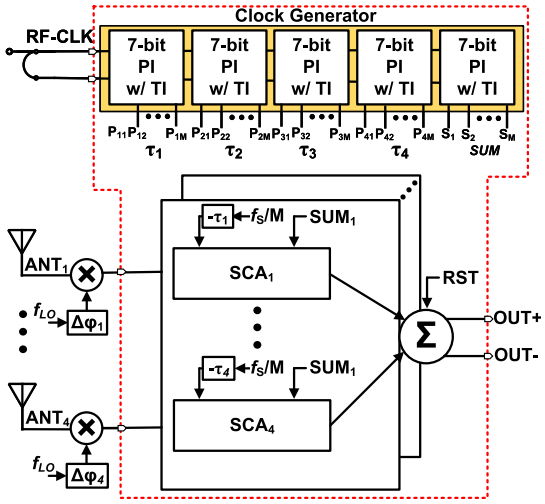

Fig. 13. Four-channel SCA BB TTD SSP diagram with five PIs.

ADCs in each channel [30], [31], [32]. Recent works by the authors have shown large delay range-to-resolution TTD circuits through discrete-time switched-capacitor-based beamforming [8], [33]. The PI enables nonuniform delays between each consecutive element which not only cancels multiple independent interferences [34], [35] but also corrects for interelement delay mismatches. PI takes the input clock and generates interpolated phases that are the weighted sum of input signal phases determined by the digital code. In the TTD SSP shown in [8] and [33], delay compensation between each antenna element is performed in base band (BB) by generating the delay sampling clock relative to the other antenna elements. No signal path was added avoiding significant losses in the analog/RF domains. Tuning interelement delays (ΔT), however, requires individual PIs and time-interleavers in each clock generator per element necessitating $N + 1$ PIs for an N-element TTD SSP out of which N PIs do delay compensation for N-signals and extra one PI to generate $(N + 1)$th nonoverlapping for signal summation. Fig. 13 shows a diagram of a four-channel TTD array with five clock generators, where PIs consume more than 50% of the overall power [9], causing a bottleneck for scaling up the antenna arrays. Hence, low-power PI with high linearity and low resolution is required. The proposed low-power and linear PI can generate a delayed clock signal up to $(F_S) = 1.6$ GHz so it can do delay compensation of the signals of a maximum bandwidth of 800 MHz as per

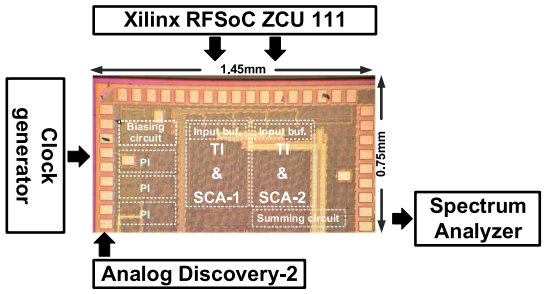

Fig. 14. Simplified test bench setup for beamforming measurement.

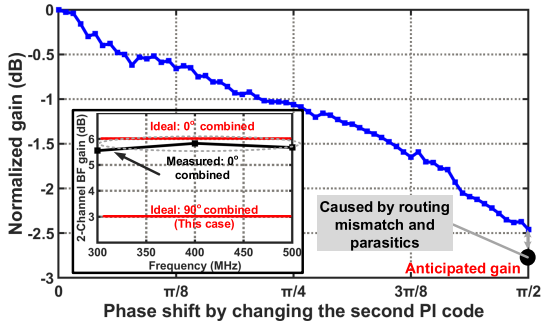

Fig. 15. Measured normalized beamforming gain plot for two channels.

the Nyquist criterion. After the PI, time-interleaving produces a longer delay. For the interleaving factor $(M) = 5$, it can do the maximum delay compensation of $(M-1)/F_S = 2.5$ ns [8].

The proposed PI is integrated in a two-channel beamformer enabling TTD arrays. Assuming critically spaced antenna and the phase shift, the line-of-sight (LOS) effect is emulated using the Xilinx ZCU111 RFSoC and applied to the two-channel TTD SSP adapted from [33]. For PI functionality characterization, a single-tone 400-MHz sinusoidal input is generated and applied to the TTD SSP from the Xilinx RFSoC ZCU111 operating under multitier synchronization mode. The control words to the PI are applied using the Analog Discovery-2 platform through the ON-chip serial-to-parallel interfaces. The simplified test setup is illustrated in Fig. 14.

The beamforming gain is measured by varying only the control word of the second PI for the first quadrant while the other PI control words are fixed to zero. This technique emulates the scenario of sweeping the sampled timing within a quadrant. The two-channel signals are summed on-chip and brought out to the spectrum analyzer.

The measured result is shown in Fig. 15 realizing a maximum beamforming gain of 2.5 dB (ideally 3 dB). As the PI code is changed, it creates a partially destructive combining scenario, which results in a drop in the output magnitude from the TTD SSP. The deviation from the ideal beamforming gain of 3 dB is due to the mismatch and the stray resistor and capacitor in the signal routing within the chip (Fig. 14). To validate this assumption, the PIs on the chip are bypassed and the time delay effect is emulated directly by ZCU111. As illustrated in Fig. 15, a 0.2-dB deviation is observed which indicates the mismatch exists and influences the beamforming performance. It is also worth mentioning that the PIs in the BB SSP do not require fast switching as long as the delay setting behavior is deterministic.

VI. Conclusion

This article demonstrates that to scale further number of arrays of BB TTD SSP, low-power PIs need to be used since the clock generator using PIs consumes major portion of power. The proposed 7-bit PI is implemented in the TSMC 65-nm process operating upto 1.6-GHz clock input.

This proposed PI compares the DAC output based on the input codes with the RAMP signal corresponding to the input clock to generate different delayed outputs. The PI includes a ramp-rate tracking circuit producing constant-slope and constant-swing ramp across PVT alleviating linearity and dynamic power issues.

The PI performance is measured with standalone PIs and PIs in a two-channel TTD SSP successfully demonstrating the delay shift required to compensate for the interelement delay. The measurement results show that the INL is within 0.52 LSB and DNL is within 0.52 LSB with power/freq of 0.315 mW/GHz. By implementing other architectures of DAC with high PSRR, the proposed PI can be made overall PVT-independent.

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References

[1] J. Walling, "Mixed-mode transceivers: A brief tutorial," *IEEE Solid State Circuits Mag.*, vol. 14, no. 3, pp. 53–64, Aug. 2022.

[2] M. Zhang, Y. Zhu, C.-H. Chan, and R. P. Martins, "An 8-bit 10-GS/s 16× interpolation-based time-domain ADC with <1.5-ps uncalibrated quantization steps," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3225–3235, Dec. 2020.

[3] W. Yuan and J. S. Walling, "A multiphase switched capacitor power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1320–1330, May 2017.

[4] R. K. Nandwana et al., "A calibration-free fractional-N ring PLL using hybrid phase/current-mode phase interpolation method," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 882–895, Apr. 2015.

[5] M. Mansuri et al., "A scalable 0.128–1 Tb/s, 0.8–2.6 pJ/bit, 64-lane parallel I/O in 32-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3229–3242, Dec. 2013.

[6] P.-E. Su and S. Pamarti, "A 2.4 GHz wideband open-loop GFSK transmitter with phase quantization noise cancellation," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 615–626, Mar. 2011.

[7] A. Tharayil Narayanan et al., "A fractional-N sub-sampling PLL using a pipelined phase-interpolator with an FoM of -250 dB," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1630–1640, Jul. 2016.

[8] E. Ghaderi, A. Sivadhasan Ramani, A. A. Rahimi, D. Heo, S. Shekhar, and S. Gupta, "An integrated discrete-time delay-compensating technique for large-array beamformers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 9, pp. 3296–3306, Sep. 2019.

[9] E. Ghaderi, A. S. Ramani, A. A. Rahimi, D. Heo, S. Shekhar, and S. Gupta, "Four-element wide modulated bandwidth MIMO receiver with >35-db interference cancellation," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 9, pp. 3930–3941, Sep. 2020.

[10] S. Mohapatra et al., "A 345μW 1 GHz process and temperature invariant constant slope-and-swing ramp-based 7-bit phase interpolator for true-time-delay spatial signal processors," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2022, pp. 147–150.

[11] T. S. Rappaport et al., "Millimeter wave mobile communications for 5G cellular: It will work!" *IEEE Access*, vol. 1, pp. 335–349, 2013.
[12] H.-T. Kim et al., "A 28-GHz CMOS direct conversion transceiver with packaged 2×4 antenna array for 5G cellular system," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1245–1259, May 2018.
[13] H. Chung, Q. Ma, Y. Yin, L. Gao, and G. M. Rebeiz, "A 25–29 GHz 64-element dual-polarized/dual-beam small-cell with 45 dBm 400 MHz 5GNR operation and high spectral purity," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 1267–1270.
[14] D.Weinlader, "Precision CMOS receivers for VLSI testing applications," Ph.D. dissertation, Dept. Elect. Eng., Stanford, Nov. 2001.
[15] G. Wu et al., "A 1–16 Gb/s all-digital clock and data recovery with a wideband high-linearity phase interpolator," *IEEE Trans. Very Large Scale Intgr. (VLSI) Syst.*, vol. 24, no. 7, pp. 2511–2520, Jul. 2016.
[16] E. Monaco, G. Anzalone, G. Albasini, S. Erba, M. Bassi, and A. Mazzanti, "A 2–11 GHz 7-bit high-linearity phase rotator based on wideband injection-locking multi-phase generation for high-speed serial links in 28-nm CMOS FDSOI," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1739–1752, Jul. 2017.
[17] S. Chen et al., "A 4-to-16GHz inverter-based injection-locked quadrature clock generator with phase interpolators for multi-standard I/Os in 7nm FinFET," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 390–392.
[18] Z. Wang and P. R. Kinget, "A 65nm CMOS, 3.5-to-11GHz, less-than-1.45LSB-INL$_{pp}$, 7b twin phase interpolator with a wideband, low-noise delta quadrature delay-locked loop for high-speed data links," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 292–294.
[19] Y.-C. Huang and B.-J. Chen, "30.7 An 8b injection-locked phase rotator with dynamic multiphase injection for 28/56/112Gb/s serdes application," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 486–488.
[20] Z. Wang, Y. Zhang, Y. Onizuka, and P. R. Kinget, "11.4 A high-accuracy multi-phase injection-locked 8-phase 7GHz clock generator in 65nm with 7b phase interpolators for high-speed data links," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 186–188.
[21] F. O'Mahony, B. Casper, M. Mansuri, and M. Hossain, "A programmable phase rotator based on time-modulated injection-locking," in *Proc. Symp. VLSI Circuits*, Jun. 2010, pp. 45–46.
[22] D. Dhar, P. T. M. van Zeijl, D. Milosevic, H. Gao, and P. G. M. Baltus, "Noise analysis of a BJT-based charge pump for low-noise PLL applications," in *Proc. Eur. Conf. Circuit Theory Design (ECCTD)*, Sep. 2017, pp. 1–4.
[23] D. Levski, M. Wäny, and B. Choubey, "Ramp noise projection in CMOS image sensor single-slope ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, pp. 1380–1389, 2017.
[24] A. K. Mishra, Y. Li, P. Agarwal, and S. Shekhar, "A 9b-linear 14GHz integrating-mode phase interpolator in 5nm FinFET process," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 1–3.
[25] M.-S. Chen, A. A. Hafez, and C.-K. K. Yang, "A 0.1–1.5 GHz 8-bit inverter-based digital-to-phase converter using harmonic rejection," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2681–2692, Nov. 2013.
[26] S. Sievert et al., "A 2 GHz 244 fs-resolution 1.2 ps-peak-INL edge interpolator-based digital-to-time converter in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2992–3004, Dec. 2016.
[27] H. Jiang et al., "A 12-bit 0.5–2.4-GHz 0.65°-peak-INL parasitic-insensitive digital-to-phase converter," *IEEE Micro Wireless Compon. Lett.*, vol. 31, no. 1, pp. 68–71, Jan. 2021.
[28] A. Jakobsson, A. Serban, and S. Gong, "A low-noise RC-based phase interpolator in 16-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 1, pp. 1–5, Jan. 2019.
[29] H. Hashemi, T.-S. Chu, and J. Roderick, "Integrated true-time-delay-based ultra-wideband array processing," *IEEE Commun. Mag.*, vol. 46, no. 9, pp. 162–172, Sep. 2008.
[30] S. Jang, R. Lu, J. Jeong, and M. Flynn, "A 1-GHz 16-element four-beam true-time-delay digital beamformer," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1304–1314, May 2019.
[31] B. Yang, Z. Yu, J. Lan, R. Zhang, J. Zhou, and W. Hong, "Digital beamforming-based massive MIMO transceiver for 5G millimeter-wave communications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 7, pp. 3403–3418, Jul. 2018.
[32] X. Zhang, A. F. Molisch, and S.-Y. Kung, "Variable-phase-shift-based RF-baseband codesign for MIMO antenna selection," *IEEE Trans. Signal Process.*, vol. 53, no. 11, pp. 4091–4103, Nov. 2005.
[33] C.-C. Lin et al., "A 4-element 800MHz-BW 29 mW true-time-delay spatial signal processor enabling fast beam-training with data communications," in *Proc. ESSCIRC IEEE 47th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2021, pp. 287–290.
[34] E. Ghaderi, C. Puglisi, S. Bansal, and S. Gupta, "10.8 A 4-element 500MHz-modulated-BW 40 mW 6b 1GS/s analog-time-to-digital-converter-enabled spatial signal processor in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 186–188.
[35] E. Ghaderi and S. Gupta, "A four-element 500-MHz 40-mW 6-bit ADC-enabled time-domain spatial signal processor," *IEEE J. Solid-State Circuits*, vol. 56, no. 6, pp. 1784–1794, Jun. 2021.

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