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## The new monolithic ASIC of the preshower detector for di-photon measurements in the FASER experiment at CERN

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**ABSTRACT:** The ForwArd Search ExpeRiment (FASER) is an experiment searching for new light and weakly-interacting particles at CERN’s Large Hadron Collider. FASER is composed of different sub-detectors, including silicon microstrip detectors, scintillator counters and an electromagnetic calorimeter. In this paper, a new preshower detector for the FASER experiment is presented. The new detector, based on monolithic pixel ASICs, will provide excellent spatial and time resolutions and a large charge dynamic range. First results from a prototype chip produced by IHP in 130 nm SiGe BiCMOS technology are shown.

**KEYWORDS:** Particle tracking detectors; Particle tracking detectors (Solid-state detectors); Timing detectors

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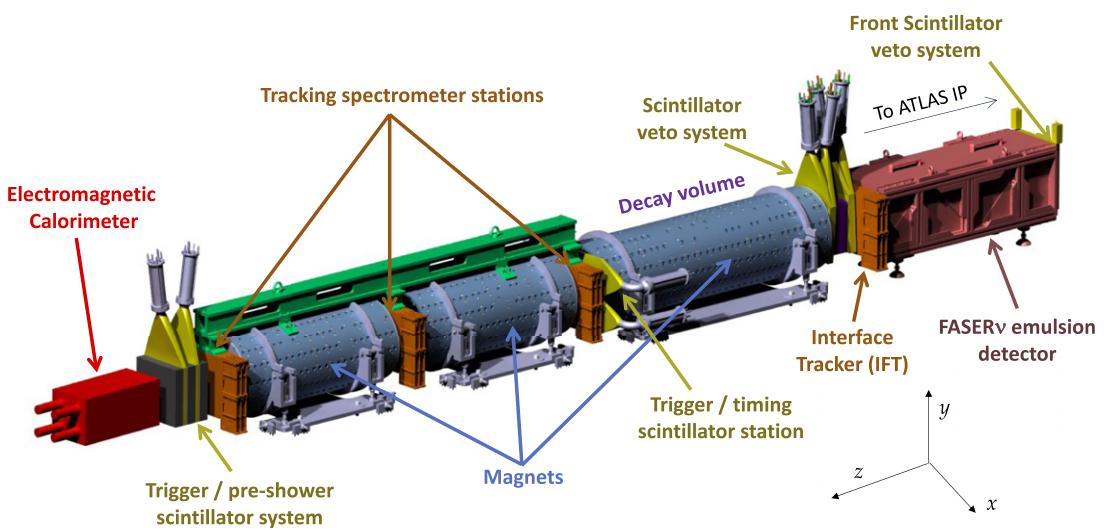
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## 1 Introduction

The quest for New Physics by the large experiments at the Large Hadron Collider (LHC) is typically based on signatures from heavy and strongly interacting particles (e.g. high transverse momentum  $p_T$ , large missing transverse energy). FASER (ForwArd Search ExpeRiment) [1] adopts an alternative approach and will search for light (MeV to GeV range) and weakly-interacting new particles (long-lived particles, LLPs), dominantly produced at low  $p_T$  from rare meson decays [2]. As these new particles are very weakly coupled, large production rates are needed to enhance their detection. FASER will exploit the large total inelastic proton cross section at the LHC ( $\sim 75$  mb at 13 TeV), where  $\sim 10^{16}$  inelastic events are expected to be produced in Run 3 ( $150 \text{ fb}^{-1}$ ), mostly in the forward direction. FASER is located  $\sim 480$  m downstream the ATLAS interaction point (IP1) along the beam collision axis line-of-sight (LOS) in the unused service tunnel TI12. A LLP produced at IP1 (e.g. dark photon  $A'$  produced from the rare decay of  $\pi^0$  or  $\eta$  mesons) may travel in the very forward direction along the LOS before decaying to visible particles in the decay volume of the detector.

A sketch of the experiment is shown in figure 1. The main detector consists of a magnet system, three tracking stations, three scintillator stations and a calorimeter [3]. It is complemented with the FASER $\nu$  [4] emulsion detector (to study neutrino interactions), a fourth tracking station (Interface Tracker, IFT) and an additional upstream scintillator station. The magnet system comprises three permanent dipole magnets with a 20 cm-diameter aperture each providing a field of  $\sim 0.57$  T. A first upstream 1.5 m-long magnet serves as decay volume to the LLPs. The tracking spectrometer [5] is formed by the other two (1 m-long) magnets interleaved between three tracking stations. Each tracking station is composed of three planes of eight double-sided silicon microstrip detectors, spares from the ATLAS Semiconductor Tracker (SCT) [6] barrel module production. The electromagnetic (EM) calorimeter consists of four spare modules from the LHCb outer EM calorimeter [7]. The first two scintillator stations are used to veto with high efficiency ( $>99.9\%$ ) any incoming charged particle, typically high energy muons produced at IP1. The third scintillator station placed in front of the spectrometer provides a trigger signal for charged particles

emerging from the decay volume (e.g.  $A' \rightarrow e^+e^-$ ). Finally, the last scintillator station, consisting of two scintillator counters interleaved with two tungsten absorber plates, provides an additional trigger signal in coincidence with the first trigger station and acts as a simple preshower for the EM calorimeter. All scintillator counters are optically coupled to photomultiplier tubes. The scintillator and calorimeter signals are digitized and sent to a custom FPGA-based board (GPIO [8]) that combines them using look-up tables and generates a global trigger signal (L1A) in case of signals above pre-defined thresholds. The L1A trigger is sent to the different detector readout boards to retrieve the data. The expected trigger rate is  $\sim 650$  Hz at  $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ , dominated by muons produced at IP1 collisions [8].



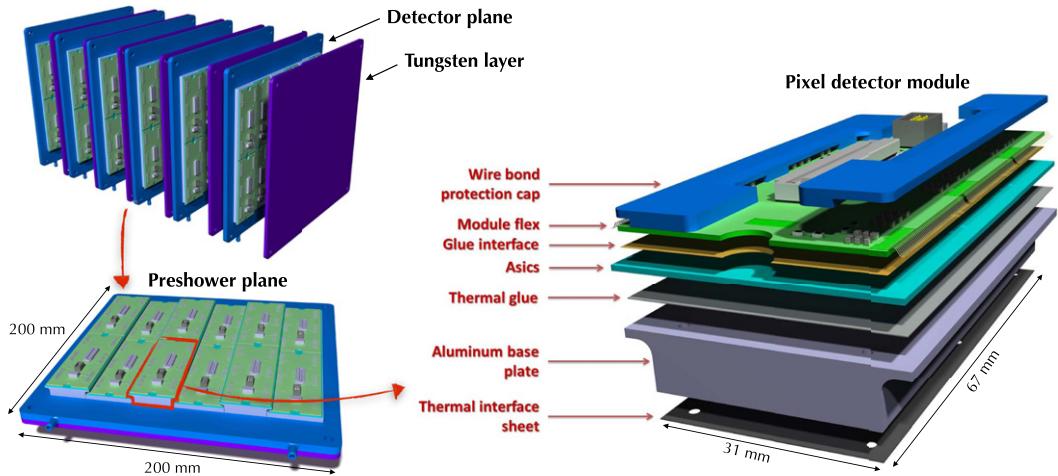
**Figure 1.** The FASER detector. Particles produced from the collisions at the interaction point 1 of the LHC enter the detector from the right. The aperture radius of the magnets is 10 cm and the total length of the experiment is  $\sim 7$  m. The sensitive area in the transverse direction ( $x - y$  plane) is larger than the magnets' aperture, approximately  $30 \times 30 \text{ cm}^2$  for the tracking layers and the veto and preshower stations, and  $40 \times 40 \text{ cm}^2$  for the timing station.

The main FASER detector was installed in the TI12 tunnel in March 2021. It was successfully commissioned in-situ with cosmic rays ( $\sim 125$ M events recorded) and with LHC pilot beam test runs in October 2021. The front veto scintillator station, the IFT tracking station and approximately 1/3<sup>rd</sup> of the FASERv emulsion detector were installed few months after, in time to start the full detector commissioning with the first LHC Run 3 beams in spring 2022. FASER is now regularly taking data at the nominal LHC beam energy of 6.8 TeV.

## 2 A new preshower detector

The role of the current preshower station in FASER is to distinguish between signals coming from deep inelastic scattering of high energy neutrinos in the calorimeter and photons. The calorimeter modules have a Shashlik layout, with wavelength shifting fibers running along the

module length perpendicularly to the absorber plates. Due to the lack of longitudinal segmentation of the sampling modules, two close-by high energy photons (e.g. coming from the decay of an axion-like particle, ALP) can't be resolved. For example, in the case of a light ( $m \sim 100$  MeV) and highly boosted ( $E \sim 1$  TeV) ALP decaying to a photon pair, the separation between the two photons is less than one millimetre. To enhance the experiment's sensitivity to the di-photon final state, a new high-granularity preshower detector based on monolithic pixel sensors has been recently proposed [9]. The baseline layout of the new preshower is shown in figure 2. It consists of six pixel detector planes interleaved with 3.5 mm-thick ( $\sim 1X_0$ ) tungsten absorber layers. This layout ( $6X_0$ ) ensures a photon conversion probability  $>99\%$  for events with one or two photons, and  $>95\%$  in the case of events with four photons. Each pixel plane is made of  $6 \times 2$  detector modules mounted on a  $\sim 20 \times 20$  cm<sup>2</sup> aluminum cooling plate. A pixel module consists of six monolithic pixel ASICs glued to an aluminum base-plate. On top of the ASICs, a flex circuit implements the SMD components, connectors and wire-bonds required to drive power and control signals. The preshower layout has been optimized given the space constraints imposed by the current FASER detector. In particular, the longitudinal gap between the last tracking station and the EM calorimeter is only 280 mm, with the additional requirement of keeping one scintillator layer for triggering purposes.

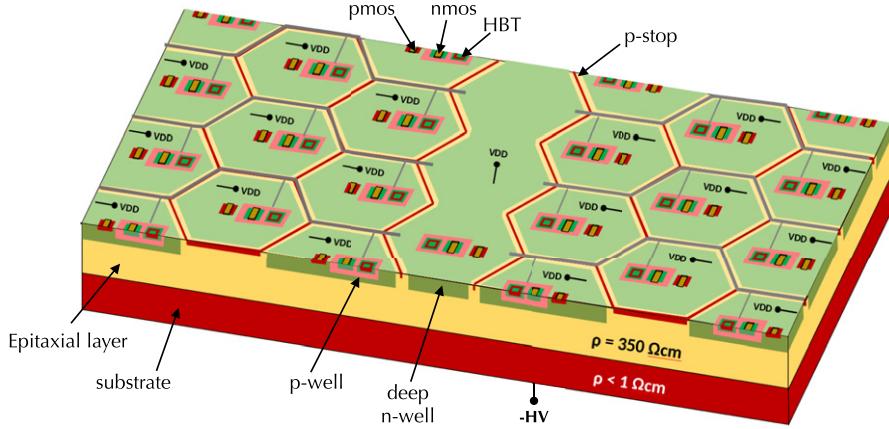


**Figure 2.** Layout of the new preshower. On a detector plane the modules are staggered with an overlap of 2 mm to minimize the effect of the dead area of the chip periphery.

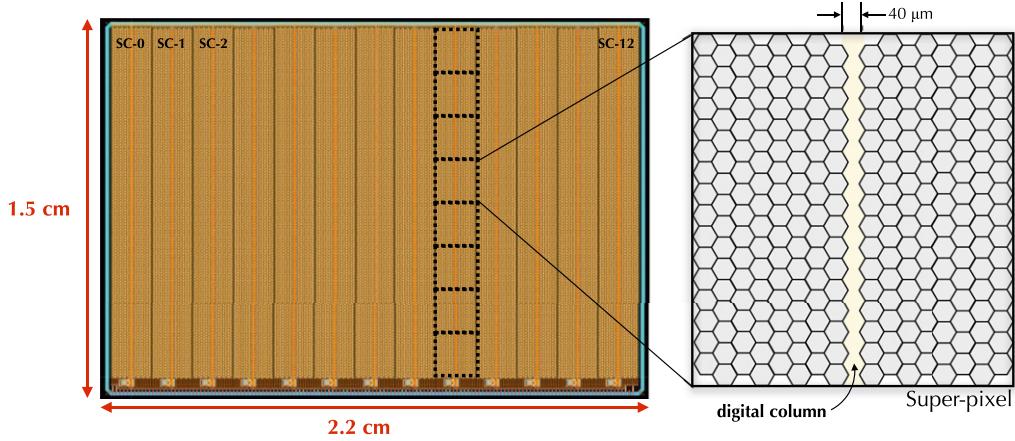
### 3 The SiGe monolithic ASIC

The proposed ASIC for the new FASER preshower modules is a monolithic pixel chip designed in 130 nm Silicon-Germanium (SiGe) BiCMOS technology (SG13G2 process by IHP Microelectronics [10]). The IHP BiCMOS technology combines heterojunction bipolar transistors (HBT) with CMOS transistors on the same die using a triple well structure. The SiGe BiCMOS technology provides fast signal amplification with low noise, resulting in excellent time resolutions [11]. Figure 3 shows a sketch of the chip structure. The pixels have an hexagonal shape (65  $\mu$ m side) for

a smoother distribution of the electric field lines on the edges. The pixel capacitance is 80 fF and the inter-pixel pitch is  $\sim 100 \mu\text{m}$ . A deep n-well implanted on a p-type substrate acts as collecting electrode. A shallow p-well embedded in the deep n-well isolates the NMOS and HBT transistors from the substrate that is set to a negative bias voltage.



**Figure 3.** Sketch of the SiGe BiCMOS chip for the new FASER preshower. An example of die with a high resistivity ( $350 \Omega\text{cm}$ ) p-type epitaxial layer on top of a low resistivity ( $1 \Omega\text{cm}$ ) p<sup>+</sup>-type substrate is shown.

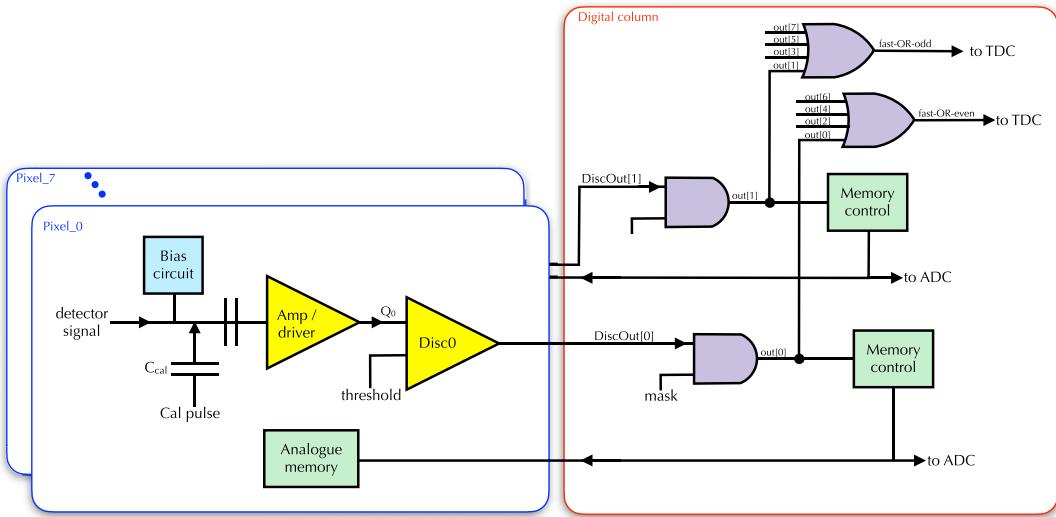


**Figure 4.** Floorplan of the FASER chip. The digital periphery is at the bottom of the chip. The sketch on the right shows the arrangement of the  $16 \times 16$  pixels inside a super-pixel. A digital column is located in the middle of each super-column.

The floorplan of the preshower chip is shown in figure 4. The  $\sim 2.2 \times 1.5 \text{ cm}^2$  ASIC contains a matrix of 26'624 hexagonal pixels arranged in thirteen *super-columns* of 2048 pixels each. Each super-column is composed of an active region and a 40  $\mu\text{m}$ -wide digital column in the middle. The digital column is in a separated n-well isolated from the surrounding pixels via a p-stop guardring. The pixels inside a super-column are arranged in so-called *super-pixels*, with a super-pixel

containing  $16 \times 16$  pixels, i.e. a single super-column consists of eight super-pixels. The  $\sim 1$  mm-wide chip periphery includes the main digital circuits (TDC, arbitration logic, slow control), a seven guard-ring structure and the input/output pads. The main specifications of the chip are a large charge dynamic range from 0.5 fC to 65 fC, a maximum readout time of 200  $\mu$ s, a power consumption less than 150 mW cm $^{-2}$  and a time resolution better than 300 ps.

A pixel row corresponds to 16 pixels, i.e. eight pixels from each side of the digital column. Figure 5 shows the basic structure of one side of the row. Each pixel contains a preamplifier, a discriminator, the bias circuitry and an analogue memory. A test-pulse of selectable amplitude can be injected directly to the preamplifier via a 55 fF calibration capacitor. Due to the large dynamic range, the preamplifier has been designed to produce a signal (time-over-threshold, ToT) proportional to the logarithm of the input charge. In the digital column, while the signal is above threshold, the memory control connects the pixel analogue memory to a load current to produce a linear charge (corresponding to the ToT). Each pixel can be masked after the discrimination stage.

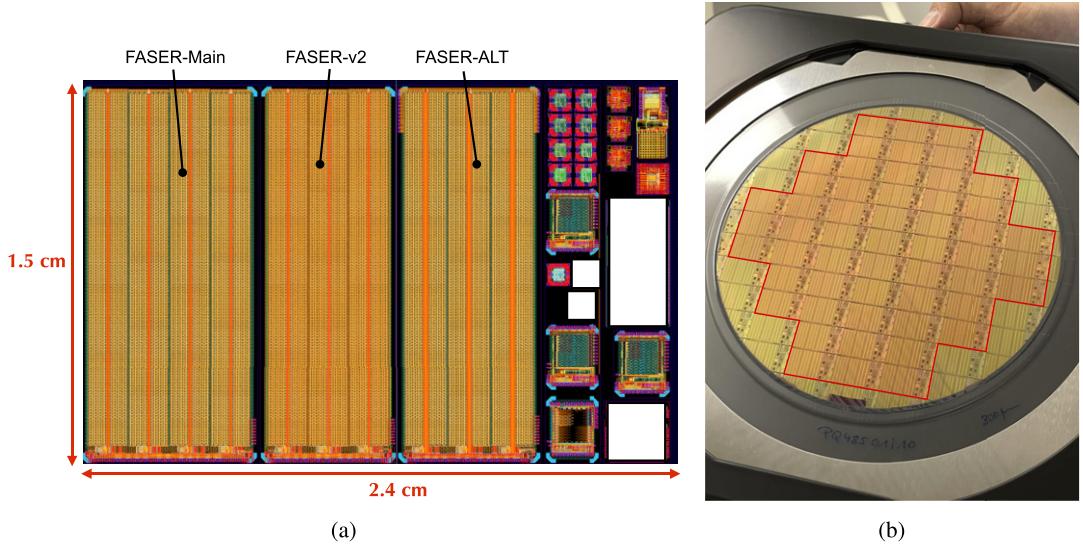


**Figure 5.** Conceptual diagram of a pixel row. For simplicity, only one side of the row is shown.

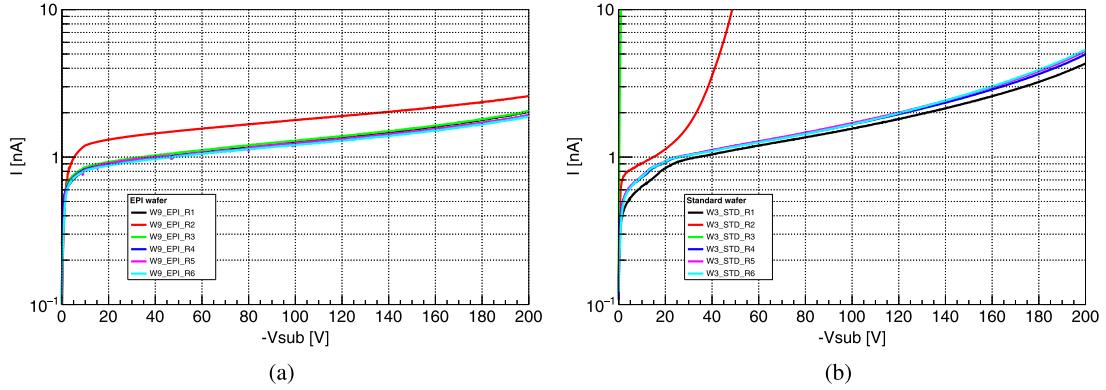
Inside a super-pixel the pixels are arranged in three different groups, with a fast-OR output signal per group connected to the digital periphery. At the periphery, the time of arrival of the fast-OR signals is digitized by a multi-channel Time-to-Digital Converter (TDC) and a trigger signal is generated from the arbitration logic to initiate the chip readout. At this stage, the charge stored in the analogue memories is digitized with a 4-bit flash-ADC. The data is then output on a single Low Voltage Differential Signal line at 200 Mbps toward the backend acquisition boards.

## 4 The pre-production chip and first results

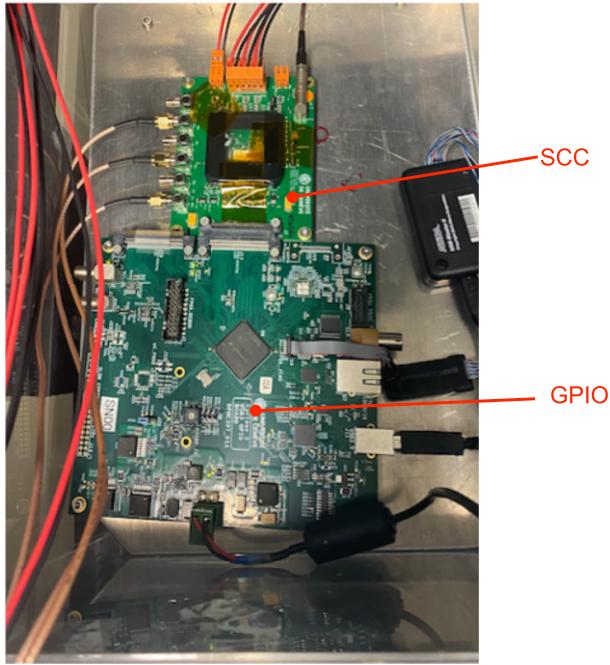
A first prototype chip has been produced. The chip reticle contains three pixel matrices, so-called FASER-Main, FASER-v2 and FASER-ALT (figure 6(a)). FASER-v2 contains  $128 \times 48$  pixels arranged in three super-columns, with the same design as explained in section 3. FASER-Main has  $128 \times 64$  pixels (four super-columns), with the same design as FASER-v2 excepting the discriminator is now located in the digital column. FASER-ALT contains  $128 \times 48$  pixels (three super-columns), without analogue memories and including a counter for charge information. The chips have a total thickness of  $\sim 300 \mu\text{m}$  and have been produced by IHP in 8" (200 mm) wafers (figure 6(b)) on two different substrates: three wafers in a  $1 \Omega \text{ cm}$  resistivity  $230 \mu\text{m}$ -thick p-type substrate with on top a  $350 \Omega \text{ cm}$  resistivity  $50 \mu\text{m}$ -thick epitaxial layer, and three other wafers in a standard  $50 \Omega \text{ cm}$  substrate (without epitaxial layer). The wafer back-side was metallized for the application of the high-voltage to the substrate. After dicing, the current-voltage (IV) characteristics of some chips have been measured on a probe-station at the University of Geneva. Figure 7 shows the IV curves of six chips from a wafer with (figure 7(a)) and without (figure 7(b)) epitaxial layer. The measurements were taken at room temperature with the innermost guard-ring connected to ground. The IV-curves are in general very good, with most of the chips reaching 200 V without breakdown with a leakage current less than 6 nA.



**Figure 6.** (a) Reticle of the first prototype chip. Several test structures (diodes, TDC, etc.), also included in the reticle, are visible on the right side next to the FASER-ALT matrix. (b) Photograph of one of the 8-inch wafers produced. The highlighted region shows the 53 chips available per wafer.



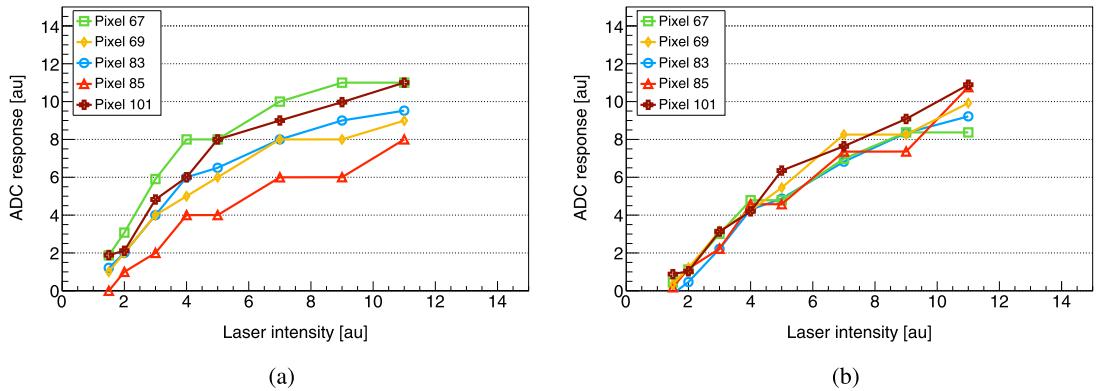
**Figure 7.** IV curves for chips from wafers produced with a low resistivity substrate and epitaxial layer (a), and with a standard resistivity substrate (b).



**Figure 8.** Single Chip Card (SCC) and GPIO board. The GPIO is based on a Cyclone V A7 FPGA and is interfaced to the control PC via USB3. The SCC is connected to the GPIO via one EMR8 40-pin connector.

Individual pixel matrices have been installed in so-called Single Chip Cards (SCCs), custom PCBs developed to test several chip features. The SCC board (figure 8) includes different independent power domains for the analogue supplies, SMA ports to access the fast-OR output lines and provides access to the guard-rings. The SCC is interfaced to a GPIO board that provides a 10 MHz Serial Peripheral Interface (SPI) for the slow control commands and a 200 MHz clock signal for the data transmission. The readout of the chip has been successfully validated using

both the internal test-pulse injection and a 1060 nm infrared laser. Figure 9 shows the response of the ADC for different laser intensities. In this example, several pixels from a FASER-v2 matrix (substrate with epitaxial layer) with a larger amplifier output mismatch were tested. The laser was focused on selected pixels using three micrometric moving stages. For each laser intensity setting, 2000 pulses were shot and the response of the ADC recorded. The charge is then corrected using calibration curves from the measurement of the ADC response to injected test-pulses of different amplitudes. The resulting spread is largely reduced, these pixels providing now a more uniform response to the same input charge.



**Figure 9.** ADC response for different laser intensities before (a) and after (b) calibration using test pulses from the internal injection circuit.

## 5 Summary

A new preshower detector is being developed for the FASER experiment at the LHC. The new preshower will allow to resolve two close-by high energy photons, typically coming from the decay of an axion-like particle produced in the decay volume of the detector. The baseline layout for the new preshower is an array of six pixel detector planes, each composed of twelve modules, interleaved with tungsten absorber layers. The building block of the modules is a new monolithic pixel ASIC developed in 130 nm SiGe BiCMOS technology. The chip has been designed with hexagonal pixels of 65  $\mu\text{m}$  side and a pitch of  $\sim 100 \mu\text{m}$ . The electronics is contained in a triple-well structure. A first prototype chip has been produced by IHP in 8-inch wafers with different substrates. Three different pixel matrices have been included in a  $1.5 \times 2.4 \text{ cm}^2$  reticle. First results indicate good IV characteristics up to 200 V and a functioning readout scheme as tested with the internal charge injection and with an external infrared laser. The detailed characterization of the chip is currently on-going, including the analysis of a testbeam (20 to 120 GeV electron beam) performed at CERN in August 2022 that included several chip prototypes and a FASER calorimeter module.

## Acknowledgments

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