Lite-Sparse Hierarchical Partial Power Processing for Heterogeneous Degradation of Batteries in Energy Storage Systems

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***Abstract*—Power conversion is a significant cost in second-use battery energy storage systems (2-BESS). 2-BESS is a sustainable pathway for retired batteries of electrical vehicles (EV) to provide energy storage for the grid and EV fast charging. We present and demonstrate the optimization of Lite-Sparse Hierarchical Partial Power Processing (LS-HiPPP) for battery degradation over the potential lifetime of the 2-BESS. LS-HiPPP has a significantly better performance tradeoff with lower power processing than other partial and full power processing architectures.**

***Index Terms*—battery energy storage systems, LS-HiPPP, heterogeneous batteries, partial power processing, second-use batteries.**

I. Introduction

Second-use batteries from electrical vehicles (EV) will be an environmental problem by 2030 [1]. These batteries still have 80% capacity remaining when they are retired. Motivated by the growth of the EV industry, the predicted available energy capacity from second-use batteries will be 3.6 GWh by 2030 [2], of which 63% will potentially be wasted [3]. Second-use battery energy storage systems (2-BESS) are a sustainable tap of the economic potential of these batteries [1] for a grid with high renewable energy penetration [4] and EV charging [5], while eliminating greenhouse gases from new battery production.

Decreasing the cost of power conversion enables the price-competitiveness of second-use batteries in 2-BESS by reducing the processed power. Other significant costs include transportation [6] and inventory [7]. Local production and just-in-time manufacturing reduces these costs, but increases the heterogeneity of supply [8], which can be addressed by sparse partial power processing [9] together with standardizing the types of power converters for economies of scale [10].

The heterogeneity of second-use batteries significantly increases with degradation [8] [11]. The conventional way to deal with battery heterogeneity is to individually process all the power from each battery. Full power processing (FPP) can fully access the battery capacity, but processes 100% of the battery power. Our goal is to maximize the utilization of battery despite degradation over its second-life, while minimizing the amount of processed power. Maintenance cost can be minimized by keeping the battery and converter interconnections through the 2-BESS lifetime and fewer converter types increase the economies of scale [10].

In this paper, we present a new dynamic optimization method for Lite-Sparse Hierarchical Partial Power Processing (LS-HiPPP) [5], [9], [12], which is an optimization over battery degradation, with results demonstrated in hardware. Compared with other power processing architectures, LS-HiPPP demonstrates high utilization despite high battery heterogeneity [5], [9], [12] for the same converter ratings. We use a stochastic model of a statistical distribution's parametric evolution, which is estimated from battery data to model the degradation process. The paper is organized as follows. Section II discusses the modeling and integration of battery degradation in the LS-HiPPP optimization; Section III presents and discusses the simulation results; Section III demonstrates the hardware testbed and the corresponding hardware results; Section V summarizes and concludes the paper.

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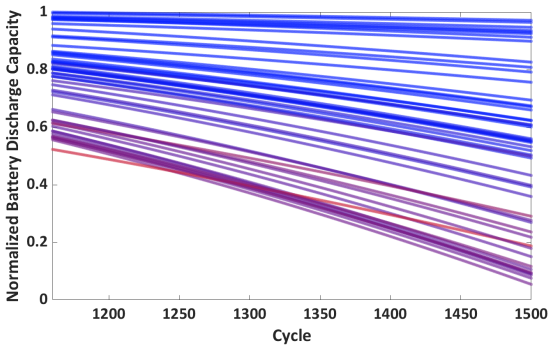
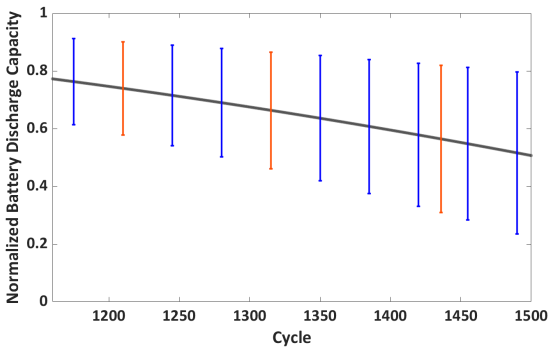


(a)



(b)

Fig. 1. Model data for battery degradation: (a) Data extrapolated from [13] using quadratic models [14]. (b) Expected value with heterogeneity (standard deviation) bars.

II. Modeling and Integration of Degradation in LS-HiPPP

Although LS-HiPPP architecture has demonstrated strong performance with heterogeneity of battery supply, previous works [5], [9], [12] used statistical models rather than actual data. The data set by [13] is used in this paper as a large public data set for degradation of cycled Li-ion batteries. As shown in Fig. 1(a), the statistical characteristics of the batteries' capacity evolve over time. The capacity heterogeneity manifests as increasing deviations over charge/discharge cycles while the decreasing average discharge capacity is modeled as a decreasing expected value as illustrated in Fig. 1(b).

Note that, although this data is for battery capacity degradation over time, we can use it to determine the battery power capability as it decreases from degradation. In this paper, we choose the power capability so that the operational C-rate is relative to the battery's full capacity at the time of operation. For example, if the battery's capacity reduces by 20 % because of degradation, then its power capability also reduces by 20 %.

A. Modeling of Degradation

Discretization in time, which is a typical method for dynamic programming [15], is used in this paper for the modeling of degradation. This procedure is illustrated in Fig. 2 and is described as follows.

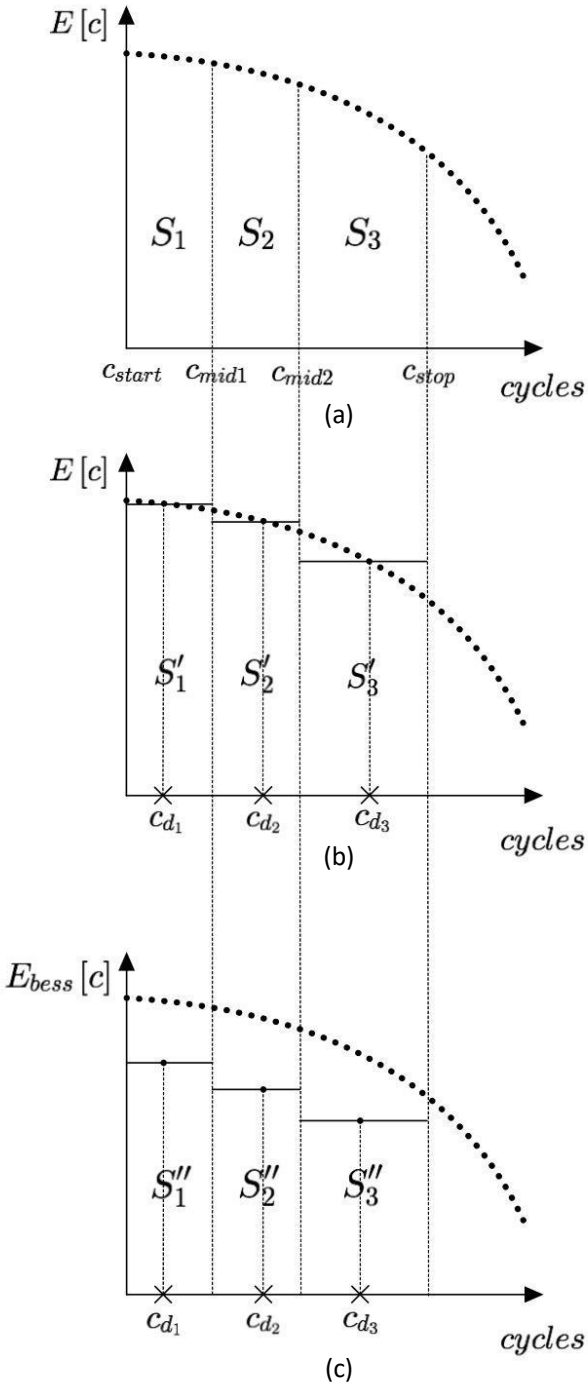


Fig. 2. Procedure for time discretization of the degradation.

First, as depicted in Fig. 2(a), the expected value of the battery capacity/power capability over time is discretized into three intervals of equal area, i.e., $S_1 = S_2 = S_3$. Then, indicator cycles c_{d1}, c_{d2}, and c_{d3} are chosen such that $S_1 = S'_1$, $S_2 = S'_2$, and $S_3 = S'_3$, as shown in Fig. 2(b). Finally, as in Fig. 2(c), the battery energy/power utilization for

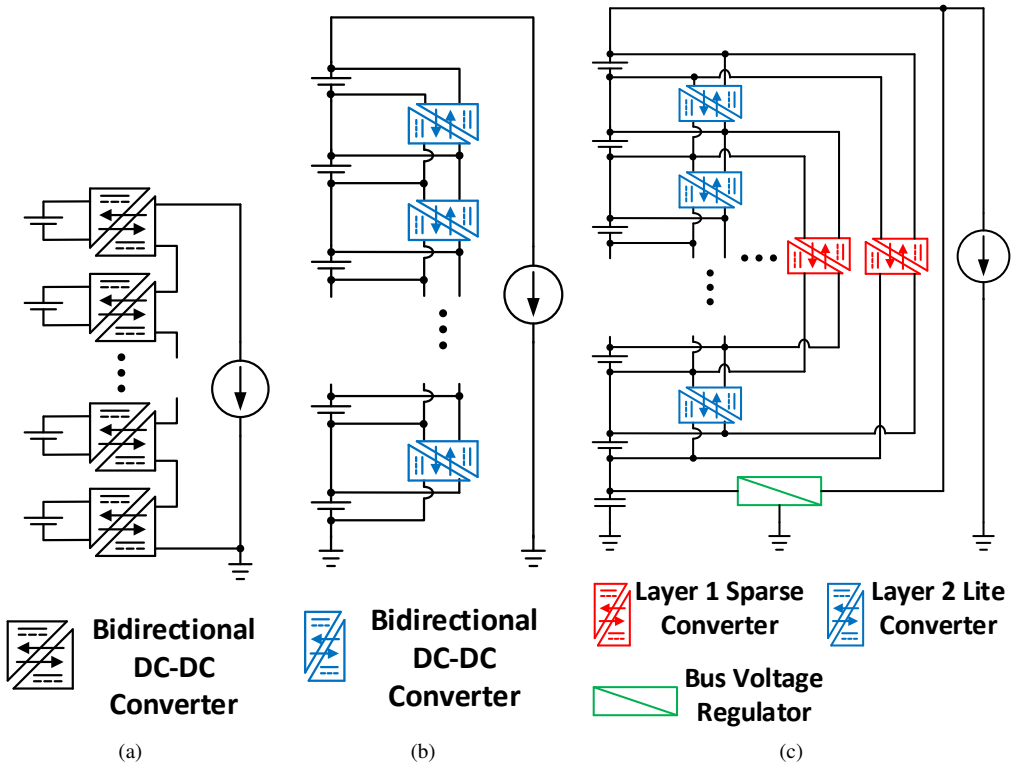


Fig. 3. Interconnection architectures for energy storage and power processing: (a) Full Power Processing (FPP). (b) Conventional Partial Power Processing (C-PPP). (c) Lite-Sparse Hierarchical Partial Power Processing (LS-HiPPP).

interval i is defined to be

$$U_i = \frac{S_i''}{S_i}, \tag{1}$$

where S_i'' refers to the energy/power utilized by the 2-BESS during interval i, and S_i refers to the overall intrinsic energy/power of batteries during interval i in the 2-BESS. In Fig. 1(b), the red error bars correspond to the resulting c_{d1}, c_{d2}, and c_{d3} of the discretization procedure.

B. Integration of Degradation in LS-HiPPP

The series LS-HiPPP architecture in Fig. 3(c) is composed of two layers of bidirectional, isolated power converters [9]. The Sparse Layer 1 processes the larger expected power mismatch while the Lite Layer 2 processes the much lower remaining power mismatch variation. The optimization goal is to maximize the overall battery power utilization,

$$U = \frac{S_1'' + S_2'' + S_3''}{S_1 + S_2 + S_3}. \tag{2}$$

The two-step optimization uses [9] to solve the subproblems over future time intervals using predicted degradation data.

Separating the design optimization of Layer 1 and Layer 2 power processing allows the design space to conform to the structure of the heterogeneity. LS-HiPPP optimally spans the technology gap between FPP, shown in Fig. 3(a), and conventional partial power processing (C-PPP) architecture, shown in Fig. 3(b), through the use of statistical decomposition and hierarchy [5], [9], [12].

For each interval, a Weibull distribution is fit to the statistical data of the corresponding indicator cycle. The fitted Weibull distribution at the indicator cycle is then mapped to the batteries in Fig. 3(c) to initiate the optimization as described in [5], [9].

The design of Layer 1 can be formulated as a linear optimization problem over all indicator cycles,

$$\max_{p_m^{(1),i}, p^i_{\text{utilized},j}} \sum_{1\le i\le I} \Big(l_i \sum_{1\le j\le J} p^i_{\text{utilized},j}\Big) \tag{3a}$$

$$\text{subject to :} \quad -\bar{P}_j^i \le p^i_{\text{output},j} \le \bar{P}_j^i, \tag{3b}$$

$$p^i_{\text{output},j} = \sum_{k\in K_j^{(1)}} p_k^{(1),i} + p^i_{\text{utilized},j}, \tag{3c}$$

$$p^i_{\text{utilized},j} = I^i_{\text{string}} V^i_j, \tag{3d}$$

$$\text{for all } 1 \le i \le I, 1 \le j \le J, 1 \le m \le M,$$

where J is the number of batteries, M is the number of Layer 1 converters (set by the user), I is the number of intervals (in our case $I = 3$), the decision variable $p^i_{\text{utilized},j}$ is the 2-BESS's output power contributed by the j^{th} terminal during the i^{th} interval, the decision variable $p_m^{(1),i}$ is the power processed by the m^{th} Layer 1 converter during the i^{th} interval, $p^i_{\text{output},j}$ is the output power of the j^{th} battery during the i^{th} interval, l_i denotes the length of the i^{th} interval, and $K_j^{(1)}$

is the j^{th} column of the interconnection matrix for Layer 1 converters that indicates the connections with the j^{th} battery in the architecture. Constraint (3b) enforces the battery input and output power limits, while constraint (3c) denotes the power conservation law for each battery. Constraint (3d) states that the power delivered at the j^{th} terminal during interval i is the product of the interval string current I^i_{string} and the individual battery's voltage; in other words, the battery determines the terminal voltage.

Note that the topology matrix $K^{(1)}$ is the same thoughout the second-life of the batteries. After Layer 1 optimization, we obtain the optimal interconnection for Layer 1 converters, $K^{(1)*}$, and also the power processed by Layer 1 for each of the different time intervals. The Layer 1 converter power rating $p^{(1)*}$ is chosen according to the highest required processed power for economies of scale.

Layer 2 converters that process the remaining battery mismatch are determined from a power flow optimization embedded in Monte-Carlo. The design of Layer 2 can be formulated as a linear optimization problem over all indicator cycles,

$$\max_{p_m^{(1),i}, p_n^{(2),i}, p^i_{\text{utilized},j}} \sum_{1\le i\le I} (l_i \sum_{1\le j\le J} p^i_{\text{utilized},j}) \quad (4a)$$

$$\text{subject to}: -(\bar{P}^i_j + \delta P^i_j) \le p^i_{\text{output},j} \le (\bar{P}^i_j + \delta P^i_j), \quad (4b)$$

$$p^i_{\text{output},j} = \sum_{k\in K^{(1)*}_j} p^{(1),i}_k + \sum_{k\in K^{(2)}_j} p^{(2),i}_k + p^i_{\text{utilized},j}, \quad (4c)$$

$$p^i_{\text{utilized},j} = I^i_{\text{string}} V^i_j, \quad (4d)$$

$$p^{(2),i}_n \le p^{(2)}_{max}, \quad (4e)$$

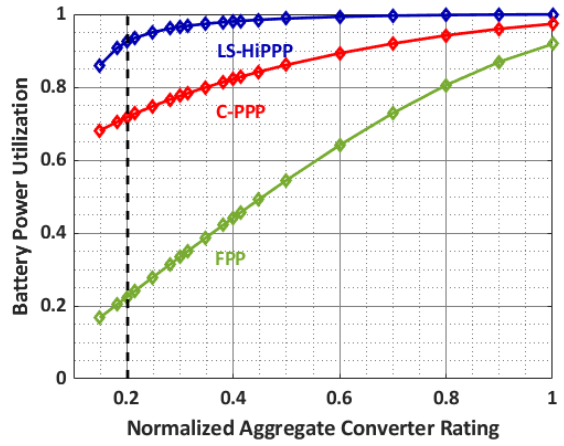
$$p^{(1),i}_m \le p^{(1)*}, \quad (4f)$$

$$\text{for all } 1 \le i \le I, 1 \le j \le J, 1 \le m \le M, 1 \le n \le N,$$

where N is the number of Layer 2 converters ($N = J - 1$), the decision variable $p^{(2),i}_n$ is the power processed by the n^{th} Layer 2 converter during the i^{th} interval, δP^i_j is the power uncertainty of the j^{th} battery during the i^{th} interval, $K^{(1)*}_j$ and $K^{(2)}_j$ are the j^{th} column of the interconnection matrices for Layer 1 and Layer 2, respectively. Note that constraint (4e) enforces that the power ratings for all Layer 2 converters are identically equal to $p^{(2)}_{max}$. Also, constraint (4f) enforces the power rating of the Layer 1 converters which was determined by the result of Layer 1 optimization.

III. Monte-Carlo Simulation Results

We use Monte-Carlo methods to validate the performance of LS-HiPPP over optimal solutions on tradeoff curves. The average performance of 2-BESS over degradation is evaluated through a large number of samples and the results (for 9 batteries, 8 Layer 2 converters, and 3 Layer 1 converters)



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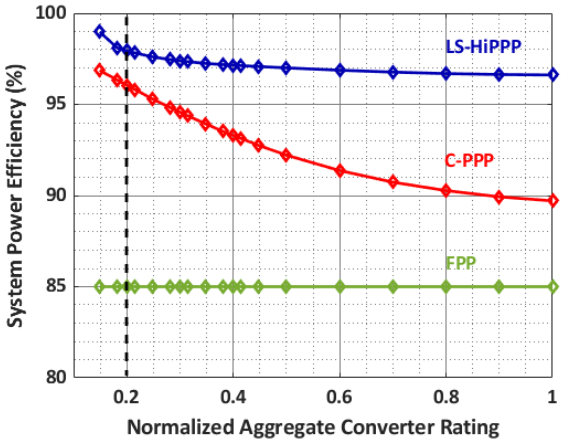

(b)

Fig. 4. Comparison of LS-HiPPP, C-PPP, and FPP performance: (a) Battery utilization as a function of aggregate converter rating. (b) System efficiency as a function of aggregate converter rating.

are illustrated in Fig. 4. In Fig. 4, the normalized aggregate converter rating is

$$\frac{\sum_{1\le m\le M} p^{(1)*} + \sum_{1\le n\le N} p^{(2)}_{max}}{\sum_{1\le j\le J} \bar{P}_j}, \quad (5)$$

and the system efficiency is

$$\eta_{\text{system}} = \frac{P_{\text{output,BAT}} - P_{\text{loss}}}{P_{\text{output,BAT}}} = \frac{P_{\text{output,BAT}} - (1-\eta_{\text{converter}})P_{\text{processed}}}{P_{\text{output,BAT}}}, \quad (6)$$

where all the converters are assumed to have individual efficiencies of $\eta_{\text{converter}} = 85\,\%$.

Economic outcome in a 2-BESS is proportional to the utilization of the battery power. LS-HiPPP performs better than the other two architectures (C-PPP and FPP), as shown by the optimal utilization tradeoff frontiers between battery power utilization over degradation and aggregate power converter

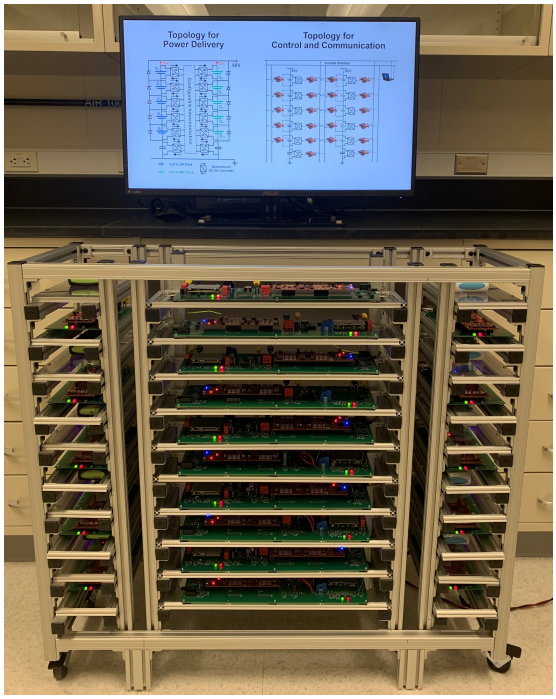

Fig. 5. Battery energy storage testbed.

rating in Fig. 4(a). When the aggregate power converter rating is 0.2, the average battery power utilization of LS-HiPPP over degradation is 0.92, as opposed to 0.72 for C-PPP and 0.22 for FPP. LS-HiPPP utilizes approximately 20 % more battery power than C-PPP when using converters with a low aggregate power rating. The power utilization difference between LS-HiPPP and FPP is 60-70 % at low power converter rating. LS-HiPPP is significantly more tolerant to lower aggregate power converter rating. As the converter rating decreases from 1 to 0.2, the power utilization reduces by less than 0.1, compared to approximate 0.25 for C-PPP and 0.7 for FPP.

High efficiency is essential in decreasing the cost of thermal management for 2-BESS. As is indicated by Fig. 4(b), LS-HiPPP has the best average efficiency over degradation among the three architectures for different converter ratings. Moreover, LS-HiPPP maintains system efficiency over the choice of converter ratings. The efficiency decreases by 1.4 % when the aggregate power converter rating increases from 0.2 to 1 for LS-HiPPP, as opposed to 6.4 % for C-PPP.

IV. Hardware Demonstration

A. Hardware Setup

A 1 kW energy storage testbed, as shown in Fig. 5, was used for hardware demonstration. The testbed is universally configurable, consisting of nominally 5 Ah NMC and 2.5 Ah LFP batteries, and bidirectional/isolated power converters for the Layer 1 and Layer 2 converters. All power converters and battery monitoring boards are controlled through Texas Instruments LAUNCHXL-F28379D kits and networked over Controlled Area Network (CAN) bus to a PC as a central

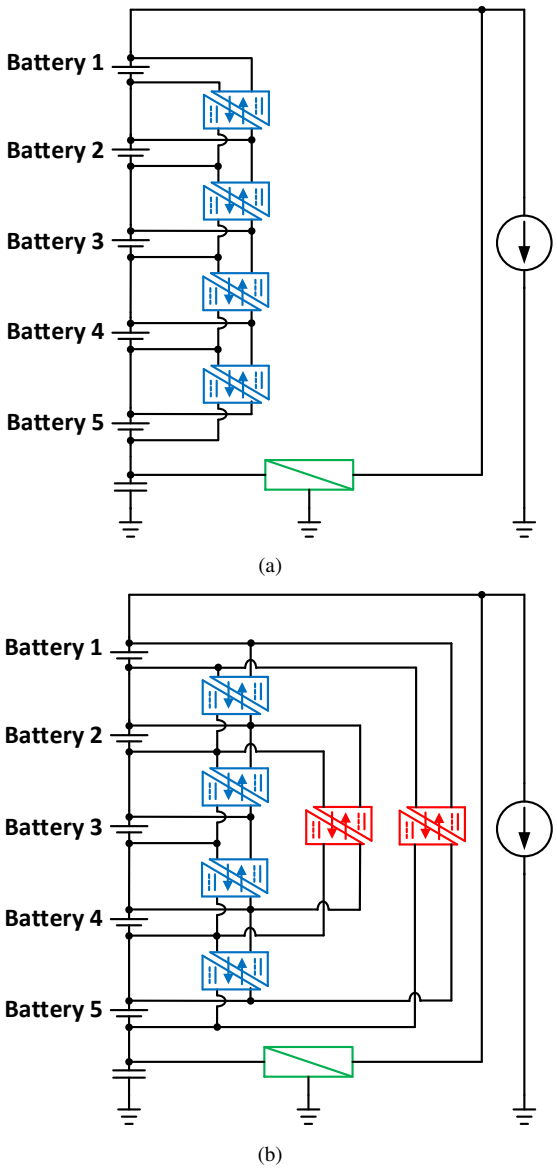

Fig. 6. Testbed configuration for: (a) Conventional Partial Power Processing (C-PPP). (b) Lite-Sparse Hierarchical Partial Power Processing (LS-HiPPP).

controller. Both centralized and distributed fault handling and protection are implemented for scalability to megawatt-level systems.

For the hardware demonstration five 2.5 Ah LFP batteries, 4 Layer 2 converters, and 2 Layer 1 converters were used. The instantiation of the 2-BESS from the data of the first indicator cycle in Fig. 1(b), resulted in Battery 1, Battery 2, Battery 3, Battery 4, and Battery 5 modules with capacity of 2.5 Ah, 2.175 Ah, 1.975 Ah, 1.725 Ah, and 1.325 Ah, respectively. The placement and power flow of the Layer 1 converters, and the power flow of the Layer 2 converters are optimized using the methods outlined in Section II. For both LS-HiPPP and C-PPP, the load was a constant current sink of 1 A and the load voltage was regulated with a bus voltage regulator converter to approximately 72 V. In other words, the performance of

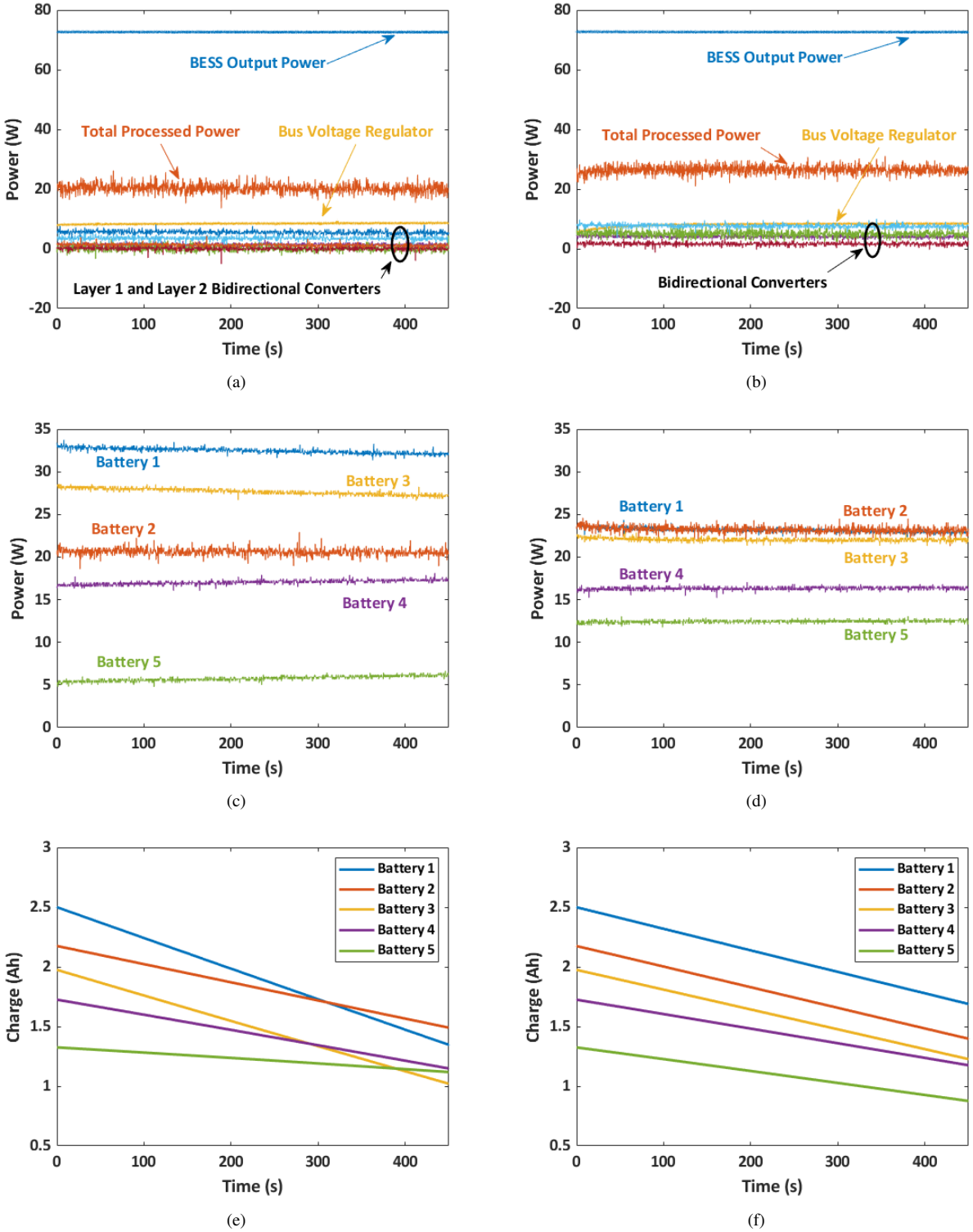

Fig. 7. Hardware results: BESS output power, and total processed and individual converter power for (a) LS-HiPPP and (b) C-PPP. Power delivered by individual batteries for (c) LS-HiPPP and (d) C-PPP. Remaining charge of individual batteries for (e) LS-HiPPP and (f) C-PPP.

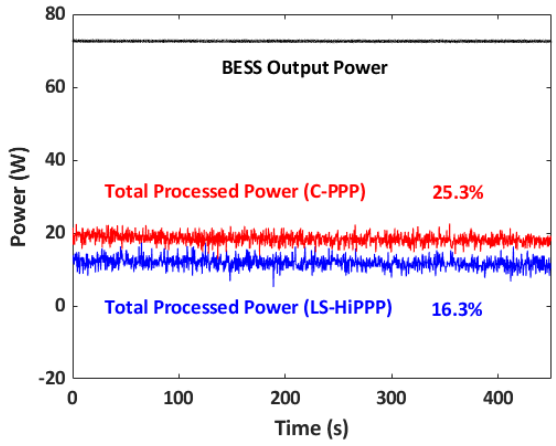

Fig. 8. Comparison of the processed power for LS-HiPPP and C-PPP, excluding bus voltage regulator.

LS-HiPPP and C-PPP were compared using identical output power and power utilization. This means that the power processed by each converter and hence the aggregate converter ratings are the metrics of performance. The configurations of the energy storage testbed for hardware demonstration are shown in Fig. 6.

B. Hardware Results

The hardware demonstration shows a snapshot of the operation of a particular 2-BESS at the beginning of its second-life use when the power converter interconnection and ratings are optimized for the entire 2-BESS lifetime. The battery ratings for this 2-BESS are supplied from the family of evolving distributions described in Section II.

In both LS-HiPPP and C-PPP, the processed power is much lower than the BESS output power because of partial power processing as shown in Figs. 7(a) and 7(b), respectively. Because of identical output power, the bus voltage regulator, which maintains the bus voltage, also processes the same power in both. In Figs. 7(c) and 7(d), LS-HiPPP allows more power to be drawn from the battery with the largest capability (Battery 1) and less from the battery with the least capability (Battery 5); the power outputs from each battery in LS-HiPPP are better optimized. The charge distribution among batteries is narrower for LS-HiPPP than C-PPP as illustrated in Figs. 7(e) and 7(f), respectively.

Ultimately, the processed power using LS-HiPPP (16.3 %) is lower than C-PPP (25.3 %), which results in higher system efficiency and power converters with significantly lower power ratings, as illustrated in Fig. 8.

V. Conclusion

In this paper, we have presented a new stochastic method for Lite-Sparse Hierarchical Partial Power Processing to optimize 2-BESS power processing over lifetime degradation. We optimize the power processing by determining the best tradeoff between converter ratings and battery power utilization by selecting the optimal power converter interconnections and power flow. We show in simulation that LS-HiPPP over 2-BESS lifetime has an expected battery power utilization of 92 % using only 20 % aggregate converter power rating as opposed to conventional partial power processing at 72 %. When using low-cost power converters with individual efficiencies of 85 %, LS-HiPPP has an estimated system efficiency of 98 % as opposed to C-PPP at 96 %, which means half the thermal management is needed for LS-HiPPP. We demonstrated in hardware a comparison in the operation between a 2-BESS using LS-HiPPP versus C-PPP.

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