

# Fabrication Development for SPT-SLIM, a Superconducting Spectrometer for Line Intensity Mapping

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**Abstract**—Line Intensity Mapping (LIM) is a new observational technique that uses low-resolution observations of line emission to efficiently trace the large-scale structure of the Universe out to high redshift. Common mm/sub-mm emission lines are accessible from ground-based observatories, and the requirements on the detectors for LIM at mm-wavelengths are well matched to the capabilities of large-format arrays of superconducting sensors. We describe the development of an  $R = 300$  on-chip superconducting filter-bank spectrometer covering the 120–180 GHz band for future mm-LIM experiments, focusing on SPT-SLIM, a pathfinder LIM instrument for the South Pole Telescope. Radiation is coupled from the telescope optical system to the spectrometer chip via an array of feedhorn-coupled orthomode transducers. Superconducting

microstrip transmission lines then carry the signal to an array of channelizing half-wavelength resonators, and the output of each spectral channel is sensed by a lumped element kinetic inductance detector (leKID). Key areas of development include incorporating new low-loss dielectrics to improve both the achievable spectral resolution and optical efficiency and development of a robust fabrication process to create a galvanic connection between ultra-pure superconducting thin-films to realize multi-material (hybrid) leKIDs. We provide an overview of the spectrometer design, fabrication process, and prototype devices.

**Index Terms**—Superconducting device fabrication, Microstrip Resonators, Millimeter wave detectors, Submillimeter wave detectors, Superconducting resonators

## I. INTRODUCTION

**S**TUDIES of the mm-wave sky have provided a wealth of information about the history of the universe. The cosmic microwave background (CMB) at a redshift of  $z = 1100$  provides a window to the earliest stages of the universe as high-energy photons are redshifted down into the mm-wave band. Similarly, far-infrared photons in the later universe are redshifted into the mm-wave band. Line intensity mapping (LIM) is a technique that uses integrated line emissions to trace the large-scale structure of the Universe out to high redshift [1]. LIM techniques have the potential to constrain cosmology (e.g., inflation, dark energy, neutrino mass) with higher precision than CMB and galaxy surveys [2]–[4]. Many common mm/sub-mm emission lines are accessible from ground-based observatories, matching with atmospheric transmission windows. Additionally, the requirements for detectors in future LIM experiments are well aligned with existing capabilities achievable with large-format arrays of superconducting sensors [5]. Many early detector plans for LIM experiments [6]–[8] draw on the heritage from decades of CMB and leKID detector development incorporating features such as low-loss superconducting microstrips [9], [10], otrrho-mode transducer (OMT) optical coupling [11], [12], and leKIDs [13] to realize OMT coupled KIDs [14]–[16]. The combination of accessible mm/sub-mm emission lines and large-format arrays of superconducting sensors makes LIM experiments a promising pathway for future cosmological breakthroughs.

The spectrometer development described below is aimed at producing the focal plane for the planned South Pole Telescope Summertime Line Intensity Mapper (SPT-SLIM) experiment [17]. SPT-SLIM is a pathfinder LIM instrument for the South

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Pole Telescope. It is designed to use the same primary mirror as the SPT-3G experiment with new pickoff mirrors and a dedicated cryostat. The cryostat will be cooled to 100 mK through the combination of a pulse tube cryocooler and an adiabatic demagnetization refrigerator (ADR). The focal plane will be filled with 18 dual-polarization pixels, each coupled to an  $R = 300$  microstrip spectrometer covering the 120–180 GHz band. Additional details on the spectrometer design are provided below in Section II. SPT-SLIM will be the first demonstration of on-chip spectroscopy in LIM-style observations that is sensitive to CO emission from  $0.5 < z < 3$ . SPT-SLIM is scheduled to deploy to the South Pole for observations in the 2023–2024 austral summer.

## II. SPECTROMETER DESIGN

SPT-SLIM employs filterbank-style spectrometers [18], [19]. The key components for the spectrometer are shown in Figure 1. Optical signals from the telescope are coupled to the spectrometer via a feedhorn to an ortho-mode transducer (OMT) coupling. The signal from opposing OMT probes are combined in a hybrid-tee and the resulting signal continues down a microstrip transmission line. For each filter bank channel one end of a  $\lambda/2$  channelizing resonator is capacitively coupled to the microstrip feedline, with each filter picking off a narrow frequency band. The channel filters are arranged from high to low frequency along the feedline with the higher-frequency channels closer to the hybrid-tee. The channel filters are designed to oversample the 120–180 GHz band. The other end of the channelizing resonator is capacitively coupled to the inductor of a lumped element kinetic inductance detector (leKID) that is used to detect the power in each channel and provides readout multiplexing. The capacitor of the leKID is capacitively coupled to a co-planar waveguide that serves as the readout line. The leKIDs are designed to resonate at 2 GHz with a frequency spacing of 500 kHz between each resonance. The frequency range was selected to match the chosen readout hardware [20] and balance the trade-off between lower resonance frequencies and larger resonator size.

## III. FABRICATION PROCESS

Spectrometer fabrication was carried out at the Center for Nanoscale Materials at Argonne National Laboratory. The superconducting microstrip and capacitors of the readout leKID are made from a Nb-NbN/dielectric/Nb stack that uses a silicon-based dielectric as described in Section III-A. The readout leKID is a hybrid device that pairs the Nb capacitors to an Al inductor. A NbN cap layer is grown on the top of the bottom Nb layer to provide a galvanic contact to the Al inductor as described in Section III-B. Nb was used in the capacitors both due to reports of lower two-level systems (TLS) noise levels for Nb grown on Si as compared to Al on Si [21] and to boost the effective kinetic inductance fraction by minimizing additional kinetic inductance from the capacitor.

The process flow to fabricate the filter bank spectrometer is shown in Figure 2. The spectrometer begins with a silicon on insulator wafer (SOI) with a high-resistivity device layer ( $> 10$  kOhm-cm) to limit losses from the substrate. The spectrometer

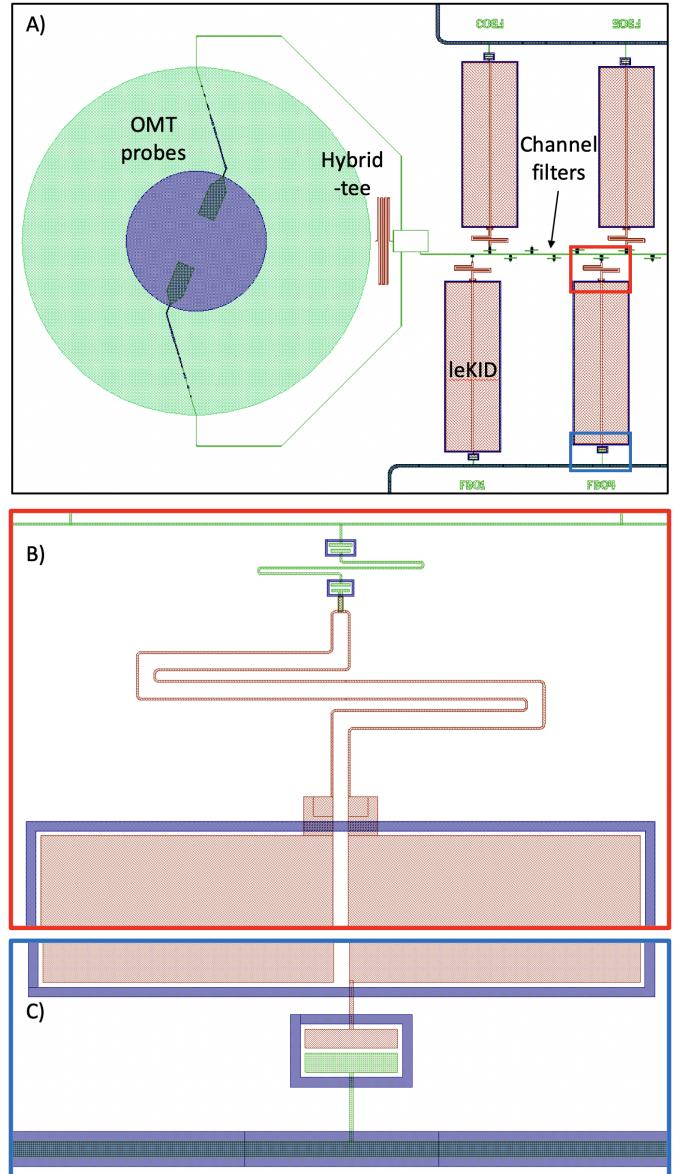


Fig. 1. Layout for a filter bank spectrometer. (A) Layout showing main spectrometer features including the OMT probes, hybrid-tee, central microstrip, channelizing filters, and readout leKIDs. (Note: while SPT-SLIM will use dual-polarization pixels we show a single polarization for simplicity) (B) Zoom-in showing channelizing filter coupled to the meander inductor and capacitor of readout leKID. (C) Zoom-in showing readout leKID connected to the readout microstrip via a coupling capacitor. For a description of the entire focal plane the reader is directed to [18].

design uses an inverted microstrip layout; using this geometry reduces the number of processing steps prior to the deposition of the Al inductors and deposits the Al layer on the high-resistivity silicon substrate in an effort to yield the highest quality Al film. The first layer is the spectrometer wiring including OMT probes, transmission lines, channelizing filters, and leKID capacitors. This layer consists of 170 nm thick Nb with a 30 nm thick NbN capping layer, which is used to form a galvanic contact to the Al inductor (for additional details on the NbN capping layer see Section III-B). The Nb/NbN layer is patterned using a fluorine-based reactive ion etch. Next the 30 nm Al inductors are patterned using a bilayer

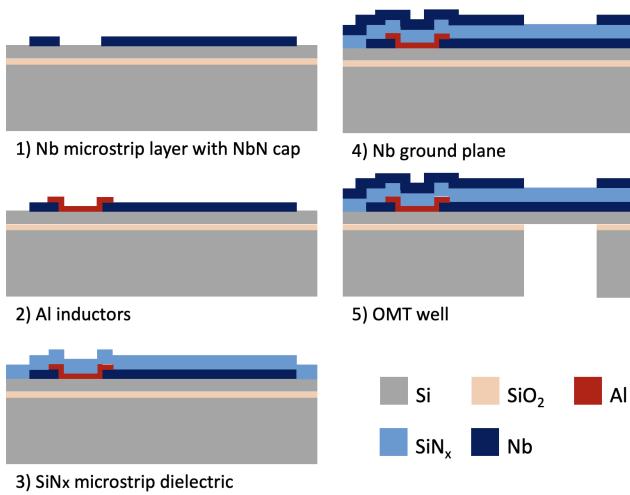


Fig. 2. Process flow for fabrication of a superconducting spectrometer with inverted microstrip on a SOI wafer.

lift-off process. The Al thickness is chosen based upon the inductor volume to achieve the required responsivity for the expected optical loading from the South Pole [18]. Following the wiring layers is the dielectric layer. The current baseline is a Si-rich  $\text{SiN}_x$  deposited by plasma-enhanced chemical vapor deposition (PECVD) at a temperature of 100°C to avoid damaging the Al inductors. After the dielectric, the Nb ground plane is deposited and patterned via lift-off. Using a lift-off process avoids any shorting that could occur from material that is deposited on the sidewall of steps; sidewall material may not be removed by an anisotropic reactive ion etch process. Next, the OMT membrane is formed by a deep reactive ion etch (DRIE) from the back side of the wafer to remove the SOI handle wafer from behind the OMT probes. Lastly, a wet etch with 10% HF buffered oxide etch is used to remove the buried oxide layer in the OMT well.

Realization of this fabrication process required addressing key technical challenges which are addressed in more detail below. The first key challenge was identifying a low-temperature dielectric deposition process that yields a low-loss dielectric. The second challenge was achieving a robust galvanic contact between the Al and Nb layers in the hybrid leKIDS despite the presence of native oxides. The last challenge seeks an alternative substrate to SOI wafers. Although high quality leKIDs have been fabricated on SOI [22] the increased cost and lead time for SOI wafers with high-resistivity device layers makes them difficult to work with in a development project where detector designs are still iterating. We explore an alternate substrate using isolated  $\text{SiN}_x$  membranes.

#### A. Low-loss Dielectrics

The quality of the dielectric used in the microstrip transmission lines and half wave channelizing filters plays a key role in the overall performance of the spectrometers. The dielectric loss tangent sets a practical limit on the spectrometer's resolution by placing a lower limit on the channelizing filter

TABLE I  
DIELECTRIC MATERIALS CHARACTERIZED IN THE SEARCH FOR A LOW TEMPERATURE DEPOSITION PROCESS FOR LOW-LOSS DIELECTRICS

Material	Process	Temp (C)	Loss Tangent (4 GHz)
SiN	CVD	275	2E-3
a-Si	CVD	275	4E-5
SiN	PECVD	100	2E-3
Si-rich SiN	PECVD	100	2E-4
$\text{SiO}_2$	IBAS	20	8E-4
$\text{SiN}$	IBAS	20	2E-3
Si-rich SiN	IBAS	20	8E-4
a-Si	IBAS	20	5E-4

bandwidth. It also impacts the overall filter efficiency. Previous work [19] simulating the performance of the SPT-SLIM filters targets a loss tangent of  $7 \times 10^{-4}$  at mm-wave frequencies. From microstrip dielectric loss measurements we expect the loss tangent at mm-wave to be up to a factor of 10 higher than the loss tangent measured at microwave frequencies [?] and thus seek a dielectric with a loss tangent near  $1 \times 10^{-4}$  at microwave frequencies. A wide range of potential dielectrics are available with many of these achieving the desired loss tangent, e.g.,  $\text{SiN}_x$  [9], [23], amorphous silicon (a-Si) [?] and amorphous silicon carbide (a-SiC) [24]. However, many of the deposition processes used for these high quality dielectrics involve heating the substrate to temperatures of several hundred degrees (250°C to 350°C). This poses challenges for the inverted microstrip process. We have observed degradation to Al inductors - formation of hillocks - when heated above 150°C and avoid any subsequent processing temperatures above this. We surveyed a range of different materials and deposition processes to identify a low-loss dielectric that can be deposited at low temperatures [25]. A summary of materials and processes used is shown in Table 1. The ideal dielectric will have low intrinsic stress, high thickness uniformity, and limited pin holes. a-Si deposited via chemical vapour deposition (CVD) meets many of these criteria, but requires substrate temperatures above 250°C. Alternatives process with lower temperature requirements include PECVD and ion-beam assisted sputtering (IBAS). The IBAS process is especially attractive as it allows for room temperature depositions compatible with lift-off processing. After evaluating several films we have identified a Si-rich  $\text{SiN}_x$  film deposited via PECVD that meets all the criteria for use with inverted microstrip. With a loss tangent of  $2 \times 10^{-4}$  at microwave frequencies (1 GHz) this dielectric loss is the lowest of the evaluated dielectrics with a low-temperature process. Additional testing of the loss tangent at mm-wave frequencies will be needed to make sure the performance does not degrade at higher frequencies.

#### B. Galvanic Contacts Using a NbN Interface Layer

The hybrid structure of the kinetic inductance detectors—Al inductors and Nb capacitors—poses an additional fabrication challenge in ensuring a clean galvanic contact between the Al and Nb layers. Early attempts at fabricating inverted microstrip devices deposited the Al inductors first followed by the Nb capacitors. These devices showed inconsistent contact between the layers with some devices open and others with various

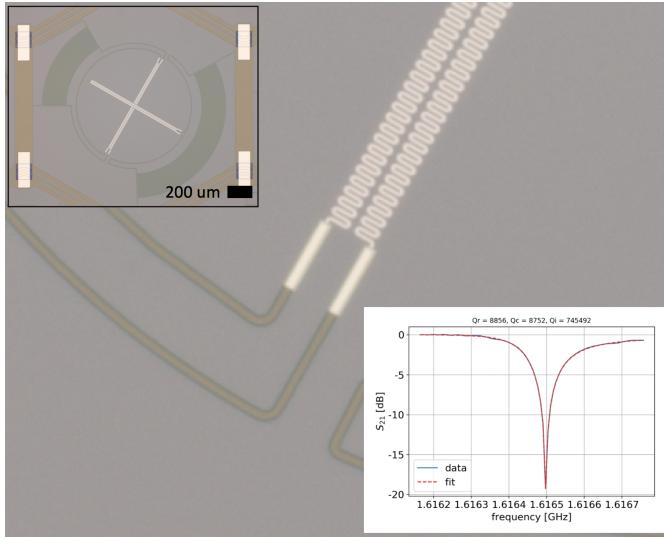


Fig. 3. Photo of a SPT-3G+ style hybrid leKID with Al inductor and Nb capacitor used to verify the RF performance of the NbN capping layer. A 30nm layer of NbN caps the Nb and provides galvanic contact between the Nb and Al. (Upper left inset) Photo of complete leKID showing meander inductor and interdigitated capacitor. (Lower right inset) Plot of  $S_{21}$  frequency sweep of leKID with corresponding parameter fit, indicating good performance of the NbN cap layer due to the high leKID quality factor.

level of contact resistance. The deposition system at Argonne does not have an ion mill, but historically has used an RF substrate bias to clean surfaces prior to deposition. This cleaning step proved insufficient in removing the native aluminum oxide from the inductors prior to the subsequent Nb deposition. Similar devices fabricated at the University of Chicago using an ion mill were sensitive to the ion mill settings and also yielded inconsistent contact between the layers. To provide a clean galvanic contact between the layers, the process steps were flipped with the Nb deposited first and a thin ( 30 nm) NbN capping layer added to the top of the Nb. The NbN cap limits oxidation of the Nb when the Nb layer is removed from vacuum and patterned. Both DC and RF test structures have been fabricated to evaluate the performance of the cap layer. The DC test structures consist of a pair of Nb-NbN-Al-NbN-Nb connections with various contact geometries. The measured resistance of the DC test structures dropped to zero when below the Al transition temperature with no sign of an interface resistance. To verify the performance at microwave frequencies we fabricated leKIDs using an SPT-3G+ design we have previously characterized and shown to have high quality factors [26], [27]. A photo of one such device along with a trace of  $jS_{21}^2$  for an example resonator are shown in Figure 3. Hybrid leKIDS made using the NbN capping layer demonstrated high internal quality factors, indicating the NbN layer was not degrading device performance.

### C. Membrane Step Down

The baseline design for SPT-SLIM calls for the spectrometers to be fabricated on a silicon on insulator (SOI) wafer with a high-resistivity device layer. This provides a high-quality surface on which to deposit the inverted microstrip

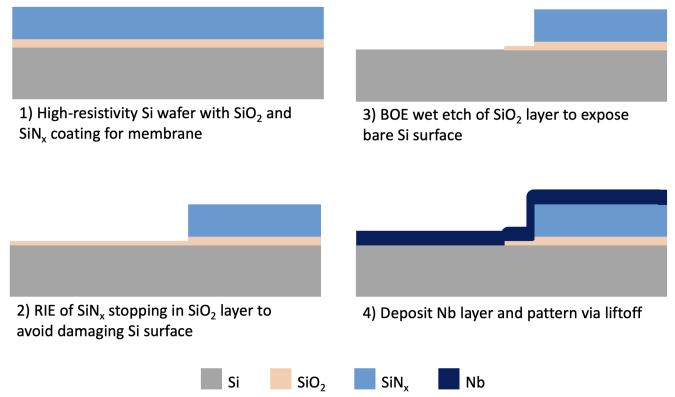


Fig. 4. Fabrication steps for membrane step down process. The SiO<sub>2</sub> layer serves as an etch stop layer for the SiNx etch to avoid damaging the Si surface.

layers. However, SOI wafers can be significantly more expensive than bulk wafers and can have long lead times when requiring specific device layer properties (e.g., thickness and resistivity). As an alternative we are exploring using bulk high-resistivity Si wafers coated with thin SiO<sub>2</sub> and SiNx layers. The SiO<sub>2</sub>/SiNx layers are used to create a membrane for the OMT probes [28]. But these amorphous dielectric layers are expected to degrade the  $1=f$  noise performance of the resonators by introducing an additional source of TLS [21]. To reduce the presence of TLS in the vicinity of the mm-wave components, we have developed a process for removing the majority of these dielectrics from the wafer. A cartoon cross section of the process is shown in Figure 4. The first step is to lithographically pattern circles slightly larger than the diameter of the OMT probes. The SiNx layer is etched in a RIE with an optical end point detection system to ensure the etch stops in the SiO<sub>2</sub> layer. The resist is stripped and a second lithography step is completed with a slightly larger diameter (roughly 10 μm) than the SiNx pattern. The SiO<sub>2</sub> layer is then etched in 10% HF buffered oxide etch to remove the SiO<sub>2</sub>, a common practice for reducing TLS for superconducting circuits. A final lithography step is performed to define the probe and wiring layer. The Nb wiring with a NbN cap layer is deposited and patterned via liftoff. Because material deposited with the sputtering process is not fully line-of-sight, the sidewalls of the membrane step are also coated with Nb providing a continuous film from the top of the membrane layer, over the sidewalls, and on to the bare silicon surface. DC connectivity tests demonstrated electrical connectivity of the Nb film over the step edge.

To fully characterize the stepdown process we have fabricated test arrays using the same well-characterized SPT-3G+ leKIDs described above that now incorporate different amounts of SiNx under the resonator. Photos of a representative chip are shown in Figure 5. There are three resonator types: resonators that sit entirely on the SiNx, resonators with inductors on the SiNx and capacitors on bare silicon, and resonators entirely on bare silicon. Figure 6 shows the internal quality factors for a similar chip with sixteen resonators: four entirely on SiNx, eight with inductors on the SiNx and

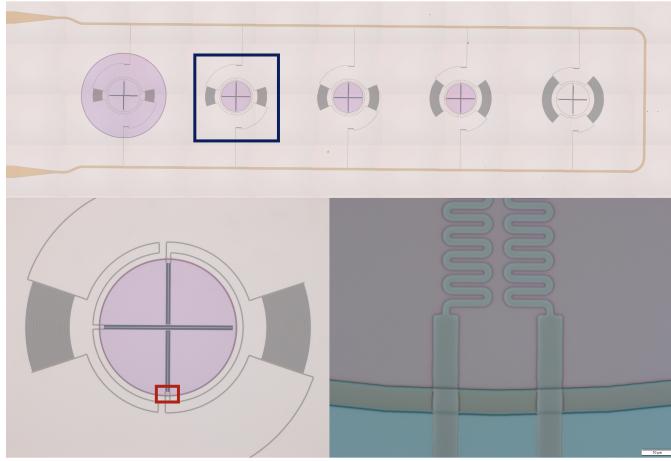


Fig. 5. (Top) Photo of a membrane step test chip with three different SPT-3G+ style leKID variations used to characterize the impact of the  $\text{SiN}_x$  membrane layer: left leKID - entire leKID on  $\text{SiN}_x$  membrane; center three leKID - inductors on  $\text{SiN}_x$  membrane and capacitors on bare silicon; and right leKID - entire leKID on bare silicon. (Bottom left) Closeup of leKID in blue box. The leKID Nb layer transitions from  $\text{SiN}_x$  to  $\text{SiO}_2$  to bare silicon, pink to grey to light blue, respectively.

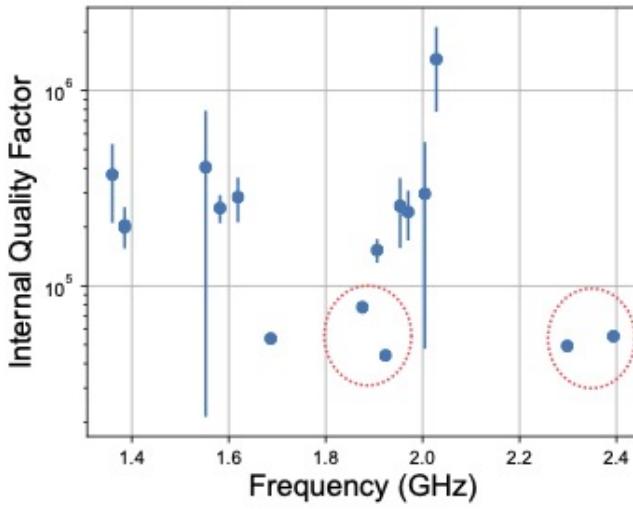


Fig. 6. Measured internal quality factors for resonators on a stepdown test chip. Resonators circled with the dashed lines were identified by frequency schedule as those entirely on  $\text{SiN}_x$ . All the resonators fabricated with capacitors on bare silicon, with the exception of one, have internal quality factors greater than  $10^5$ . Each resonance was measured five times with the median value indicated by a dot and the standard deviation shown with error bars.

capacitors on bare silicon, and four entirely on bare silicon. All sixteen resonators are present suggesting that the stepdown does not impact resonator yield. Based upon frequency scheduling we identify the resonators circled by the dashed line as those resonators entirely on  $\text{SiN}_x$ , which also are among the lowest internal quality factors. Eleven of the twelve other resonators have internal quality factors greater than  $10^5$ ; the cause of the 5th resonator with low internal quality factor is unclear. Following quality factor measurements, the next step for this test is to measure the noise performance.

#### IV. PROTOTYPE CHIPS

Prototype chips to test isolated components of the spectrometer are in development. A layout for this chip is shown in Figure 7. The layout consists of four sets of spectrometer-like devices (optical coupling structures have been left out to simplify the fabrication process). Two of the devices consist of four readout banks, each bank containing 194 leKID channels with the entire device spanning 2.011–2.489 GHz; the 500 kHz resonator spacing is the targeted spacing for the final SLIM instrument. Two of the devices have sparse spacing with 194 leKIDs spanning the entire 500 MHz readout bandwidth. Fabrication of these devices is currently ongoing.

Following testing of the isolated components several steps of integrated testing are required on the path to a deployable focal plane. This testing will be done using a layout that combines a series of test chips and a spectrometer sub-module on a single wafer. Fabrication and testing rounds are needed to verify our resonator trimming process, the optical pass bands, and the microstrip transmission loss at mm-wave for the selected dielectric, which is still to be determined. By combining test chips and sub-modules on a single wafer, once testing verifies a successful fabrication process we will have a potentially deployable portion of the focal plane in hand. Design and layout of these wafers is ongoing.

#### V. CONCLUSIONS

Line Intensity Mapping is a promising experimental technique for uncovering answers to some of the most fundamental questions about the nature of the universe. Superconducting spectrometers operating in the mm-wave frequency band are well matched to the needs of future mm-wave LIM experiments. We describe the development of superconducting spectrometers designed to operate in the 120–180 GHz band for the upcoming SPT-SLIM instrument which is scheduled to deploy in the 2023–2024 austral summer. This instrument will serve as a pathfinder to demonstrate the viability of ground-based LIM measurements in the mm-wave bands.

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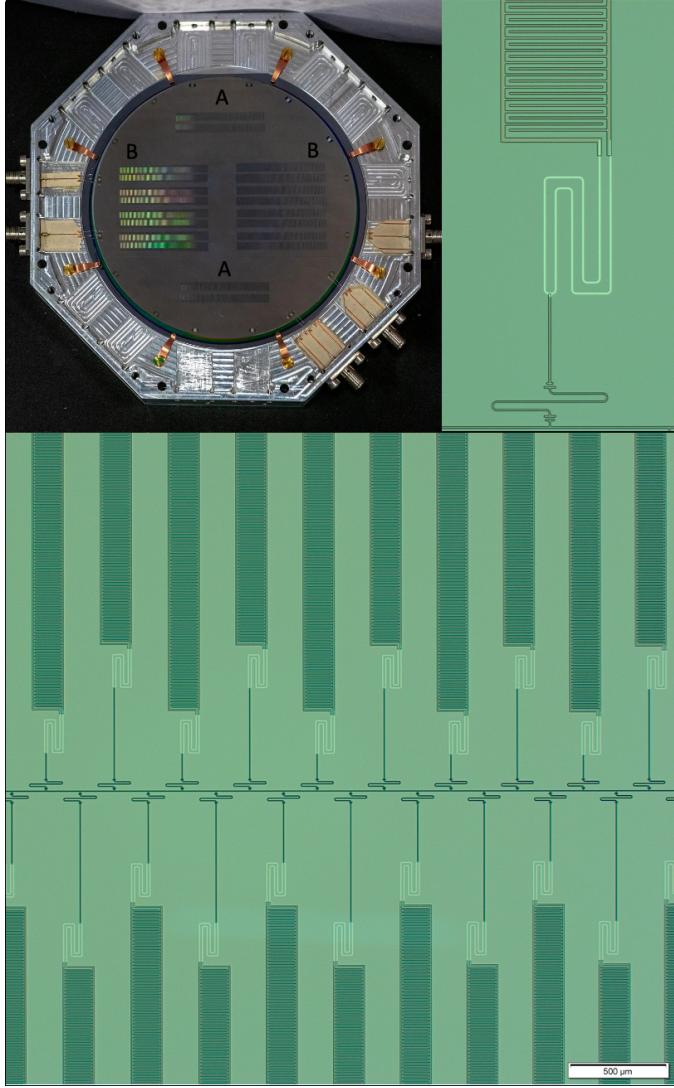


Fig. 7. Photos of a multiplexing test wafer designed to evaluate the multiplexing factor of filter-bank spectrometer readout leKIDs. (Upper left) Wafer mounted in sample box. The wafer contains four test spectrometer banks: two (A) with a single, sparsely spaced readout bank and two (B) with four closely-spaced readout banks. (Bottom) Zoom-in on a filter bank showing the array of filters connected to readout leKIDS. (Upper right) Photo of a single channel with channelizing filter at bottom and leKID at top.

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