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Imperfection-enabled memristive switching in van der Waals materials

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Memristive devices can offer dynamic behaviour, analogue programmability, and scaling and integration capabilities. As a result, they are of potential use in the development of information processing and storage devices for both conventional and unconventional computing paradigms. Their memristive switching processes originate mainly from the modulation of the number and position of structural defects or compositional impurities—what are commonly referred to as imperfections. While the underlying mechanisms and potential applications of memristors based on traditional bulk materials have been extensively studied, memristors based on van der Waals materials have only been considered more recently. Here we examine imperfection-enabled memristive switching in van der Waals materials. We explore how imperfections—together with the inherent physicochemical properties of the van der Waals materials—create different switching mechanisms, and thus provide a range of opportunities to engineer switching behaviour in memristive devices. We also discuss the challenges involved in terms of material selection, mechanism investigation and switching uniformity control, and consider the potential of van der Waals memristors in system-level implementations of efficient computing technologies.

Internet of Things and artificial intelligence technologies, which rely on large data streams and data-centric computing, require efficient data processing and storage components. Memristive devices can offer non-volatile storage capabilities, multiple storage states and compatibility with silicon technology, and have the potential to overcome the limitation of conventional von Neumann computing architectures and act as building blocks for the next generation of computing technologies[1–3]. Typically, the devices are based on electrical-bias-induced switching between a high-resistance state (HRS) and a low-resistance state (LRS)—known as a SET and RESET process[4]. The resistive switching originates from the generation, annihilation and/or rearrangement of material imperfections at the atomic scale. The presence of even a tiny number of imperfections can substantially change the electronic/ionic interactions, ion distribution or migration kinetics, giving rise to rich switching characteristics in memristive materials.

Comprehensive investigations of traditional oxide materials (including titanium-, tantalum-, hafnium- and silicon-based devices) have revealed several types of memristive switching mechanism and demonstrated a variety of potential applications[5–7]. For higher integration density and energy efficiency, researchers keep shrinking the minimal dimensions of memristors. However, this scaling creates challenges in terms of achieving reliable resistive switching. At thicknesses below 3 nm, local non-uniformity and random defects severely impact the switching invariability[8]. For instance, because the device resistance

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depends strongly on the dielectric thickness, even a tiny fluctuation results in a substantial device-to-device variation, which becomes a severe problem for most applications, which involve millions to billions of such devices. Moreover, it has been shown theoretically and experimentally that a thinner dielectric layer lowers the forming threshold of conductive pathways (also called conduction channels or filaments), leading to multiple conduction channels and working currents elevated to hundreds of microamperes or milliamperes, which would reduce energy efficiency[9,10]. The possibility of channel overgrowth will be further aggravated if the thickness decreases to a nanoscale or subnanoscale, as the effect of defects will be amplified and the enlarged switching region seriously threatens the switching reliability[11]. Thus, innovation of switching media is necessary to further improve memristive performance.

As an alternative, layer-structured van der Waals (vdW) materials with a lower electron density of states enable low-current resistive switching below nanoampere levels[12–15]. A high-quality vdW crystal offers atomic-level local uniformity in both morphology and dimension. Such a uniform switching medium is expected to reduce variations between different devices and switching cycles. Their all-surface geometry makes vdW systems an excellent platform for introducing and characterizing various defects. Defects and ionic activities can be effectively controlled in atomically thin vdW layers via electric, magnetic, thermal or optical fields[16,17], and novel properties emerge in polymorphic phase structures of transition metal chalcogenides (TMCs)[18]. These unique features of vdW materials provide a greater freedom for creating precisely engineered memristive devices.

Recent work on vdW memristive devices has shown the importance of understanding the interplay between the intrinsic physicochemical properties of the materials and the imperfections in the system. For example, a single vacancy defect in a vdW monolayer represents the smallest switching dimension in terms of thickness and area[19]. The electrostatic gating effect enables vacancies to multidirectionally migrate in planar devices to tune the Schottky barrier heights and conductivity[16,20]. The migration process can be driven by existing grain boundaries that provide faster paths for ion motion[15,21]. The layered structure and layer-number-dependent structural symmetry of TMCs render metal-ion intercalation accessible and manipulable, and can be used to control phase distribution and regulate local resistance[22]. Compared with traditional oxide materials, some oxidized vdW materials can retain their pristine crystal structures and are more robust against high temperature[23,24]. Recent work has already highlighted how various imperfections contribute to the switching processes in vdW memristors. However, a more comprehensive understanding of the imperfection-enabled switching mechanisms and characteristics is fundamental to realizing the full potential of vdW memristive devices.

In this Review, we examine work on vdW memristors that provides insight into how different imperfections in vdW systems enable memristive behaviours. We consider three imperfection-enabled memristive mechanisms and characteristics, which can be used for applications in data storage, neuromorphic computing and radiofrequency devices. We also discuss the key challenges that need to be addressed to develop high-performance memristive devices and propose more precise imperfection engineering strategies for developing high-density and energy-efficient computing systems.

Imperfections in vdW memristive materials

'Imperfections' in this review refers to various defects, disorders or impurities in vdW materials, which are traditionally viewed as undesirable factors but play critical roles in memristive devices (Fig. 1a). As summarized in Supplementary Table 1, imperfections can be generated during crystal preparation or post-treatment. The defect type, density, size and distribution are primarily determined by the specific preparation technique (for example, chemical vapour transportation, chemical vapour deposition (CVD), mechanical or liquid exfoliation, and hydrothermal methods) and conditions (for example, temperature gradient, precursor concentration, substrate orientation, vapour flow rate, and exfoliating force)[25]. Vacancies are the most common defects in vdW materials, including single, double and multiple vacancies, depending on the number of atoms missing from the lattice sites[26]. Vacancy defects can serve as active sites in favour of the occupation and removal of metal atoms to change the resistance. In addition, they can migrate driven by electric field and induce structural or valence alteration to the host layer[21]. Grain boundaries, a group of dislocation cores stitching two grains, arise from the coalescence of neighbouring crystal domains[27,28]. A diversity of morphologies can be formed depending on the misorientation angles[29]. Grain boundaries can accommodate numerous mobile particles and introduce notable fluctuations in electronic states[29,30], as shown in Fig. 1b(i). For example, a metallic wire-like grain boundary in graphene induces a local doping effect on the Fermi level. Edge atoms in grain boundaries bond weakly to the interior ones and can be easily mobilized. These properties make grain boundaries an active factor in regulating the electrical transport of vdW materials.

Imperfections such as structural-distortion-induced phase boundaries and oxidization-induced dopants can be intentionally created by post-treatment[31–33]. The entropy difference between different phases of two-dimensional (2D) vdW systems is smaller than that of three-dimensional (3D) bulk systems, leading to a lower phase transformation barrier[34]. This makes polymorphic phase transition in vdW materials more accessible to enable resistive switching. For example, lithium intercalation can produce new phases by modifying the electronic states and inducing structural distortion (Fig. 1b(ii))[35,36]. 'Dopants' refers to the exotic atoms incorporated into the crystal lattice that modify the charge carrier type and density of the host materials, and can modulate the switching dynamics by either directly participating in the resistive switching or introducing other types of defect, such as vacancies. As a typical doping approach, the oxidization of vdW materials induced by surface plasma or thermal annealing can effectively enhance their memristive properties, as mobile oxygen anions can play a more active role in the resistive switching process[12,37]. Recent studies reported that resistive-switching-inactive TMCs that feature a low defect density—for example, ReS_2—can be doped by Mo irradiation using molecular beam epitaxy, during which lattice disorders and sulfur vacancies can be introduced[38]. Moreover, other mild doping strategies such as CVD-based alloying doping, surface charge transfer doping or chemical treatment doping may also be applicable to vdW materials[39,40].

Cracks and wrinkles are also imperfections in vdW materials. They are usually created over the course of device fabrication and regarded as undesirable factors for device yield in large-scale fabrication. For vdW memristors built in the pristine region, cracks and wrinkles outside the switching area have little impact on the switching behaviour because the working currents in these devices are driven locally and usually out of plane[41]. On the other hand, wrinkles within the switching area potentially offer a platform to investigate the strain effect on memristive dynamics. Furthermore, if we intentionally introduce some missing parts in vdW materials, for example, creating nanopores by ion bombardment or cracking gaps by strain engineering, then we can control the spatial distribution of ion permeability to better manipulate the conductive channel[42,43].

Imperfection-enabled memristive mechanisms

Recently reported vdW memristive devices can be categorized into three groups according to the microscopic switching physics: electrochemical metallization (ECM), valence-change mechanism (VCM) and phase-change mechanism (PCM). The three switching mechanisms rely on either the manipulation of conduction channels or the modulation of contact barrier heights and each of them involves a set of imperfections, as summarized in Fig. 2. This section will introduce the dominant

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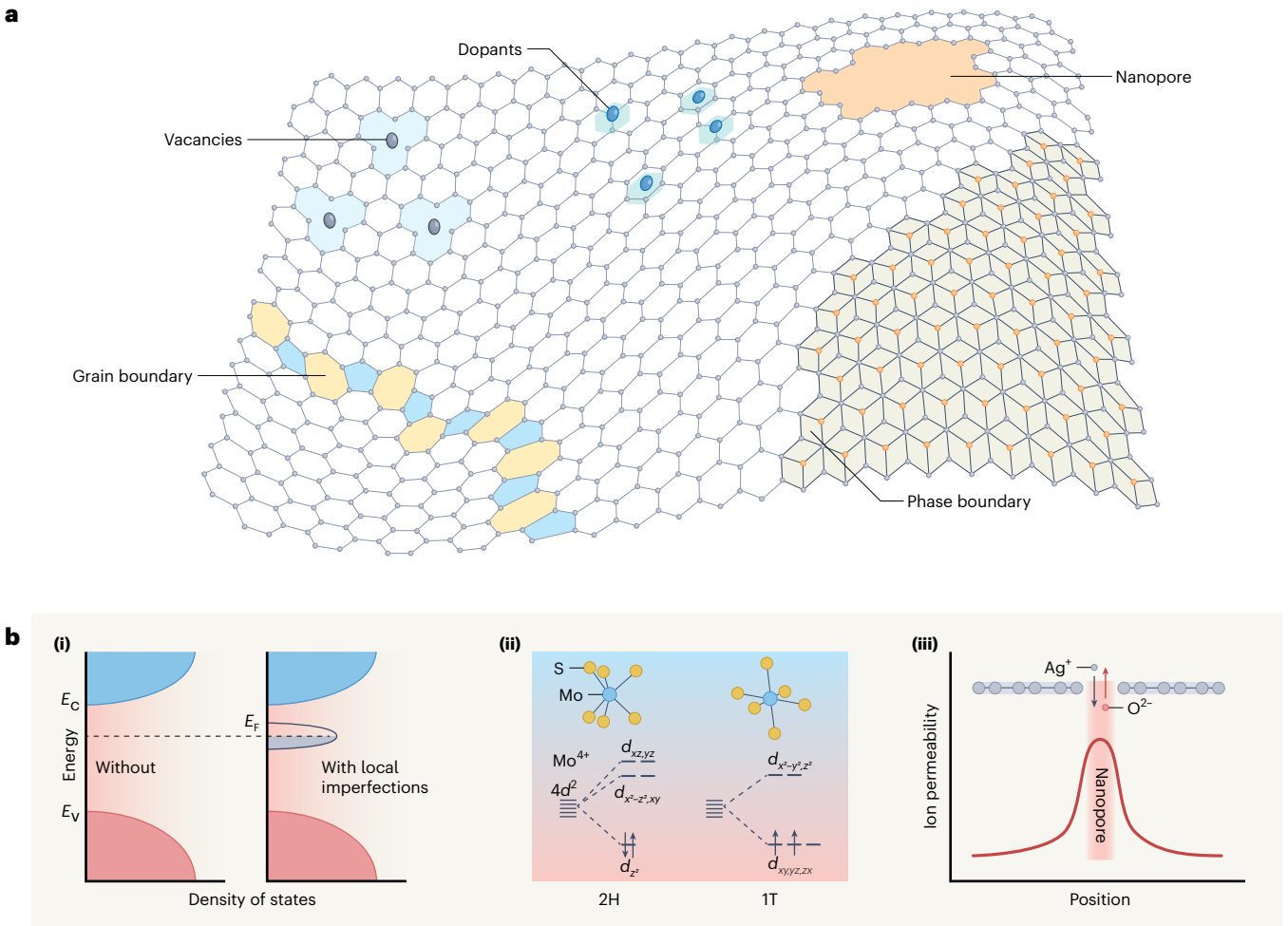

Fig. 1 | Various imperfections in vdW materials. a, Structural schematics of various imperfections generated during material preparation or post-treatment processes, including vacancies, dopants, grain boundaries, phase boundaries and nanopores in vdW materials. **b**, Typical imperfection-enabled properties of vdW memristive materials. (i) The introduction of finite electronic states near the Fermi level by material imperfections, such as metal atoms occupying chalcogen vacancies and grain boundaries, leading to local metallic behaviour[19,26,30]. (ii) The electronic states of Mo 4*d* orbitals of 2H and 1T MoS_2. The 2H semiconductive phase in the trigonal-prismatic unit originates from the three-group splitting of Mo 4*d* orbitals and completely occupied $4d_{z^2}$. The 1T metallic phase in the octahedral unit results from the two-group splitting and partially occupied $4d_{xy,yz,xz}$. (iii) The ion permeability of a defective vdW film[94]. The pristine part without nanopores shows a low ion permeability but the region with nanopores has a high ion permeability.

or assistant role of imperfections and analyse the microscopic picture of a specific switching process.

Electrochemical metallization

ECM-based memristors are basically electrochemical cells with electrochemically active metal electrodes. Their switching process features the formation and rupture of metallic conductive channels that bridge two electrodes, which determines the resistive states of the device stack. Metal atoms from the active electrode need to overcome a series of energy barriers during ionization, migration and reduction to realize resistive switching. Vacancies and grain boundaries in switching media serve as active host sites for metal atoms to form metallic conductive bridges[12,44,45].

Most ECM switching processes are contributed by both vacancies and grain boundaries (except in single crystals)[12,13,19,44–51]. In switching media, vacancies serve as active host centres for metal atoms to form metallic conductive bridges[12,44,45]. Grain boundaries are fast paths for metal ion migration and provide preferred forming locations for conduction channels[13,52,53]. Moreover, grain boundaries also have a low activation energy for the generation and transport of vacancy defects[21]. These factors work synergistically to promote the modulation of conductive channels in the ECM switching process. Generally, the larger the grain size, the lower the operation current, as there are fewer grain boundaries to help form conductive channels[52]. So far, memristive switching facilitated by grain boundaries has been demonstrated in few-layer vdW materials (for example, TMCs and hexagonal boron nitride (h-BN)) sandwiched by active electrodes (for example, Ag, Ti, Cu)[12,13,52,53]. The channel formation at grain boundaries can be confirmed by microscopic morphology and elemental distribution variation (Fig. 2b).

When the thickness of the switching medium decreases to a monolayer, even filling a single metal atom in or removing it from a vacancy can markedly change the resistance of vdW materials. This type of memristive device is called an atomristor (Fig. 2b), and shows great potential for overcoming the thickness bottleneck of bulk-oxide memristors[44,46]. ECM switching atomristors were first demonstrated in a vertical metal/monolayer MoS_2/metal device and then in a broad group of monolayer vdW materials (for example, disulfide, diselenide and h-BN)[44,47].

The role of native vacancies in ECM switching of a MoS_2 single-defect atomristor is visualized via in situ scanning tunnelling microscopy[19]. As shown in Fig. 3a, a gold probe and a MoS_2 monolayer

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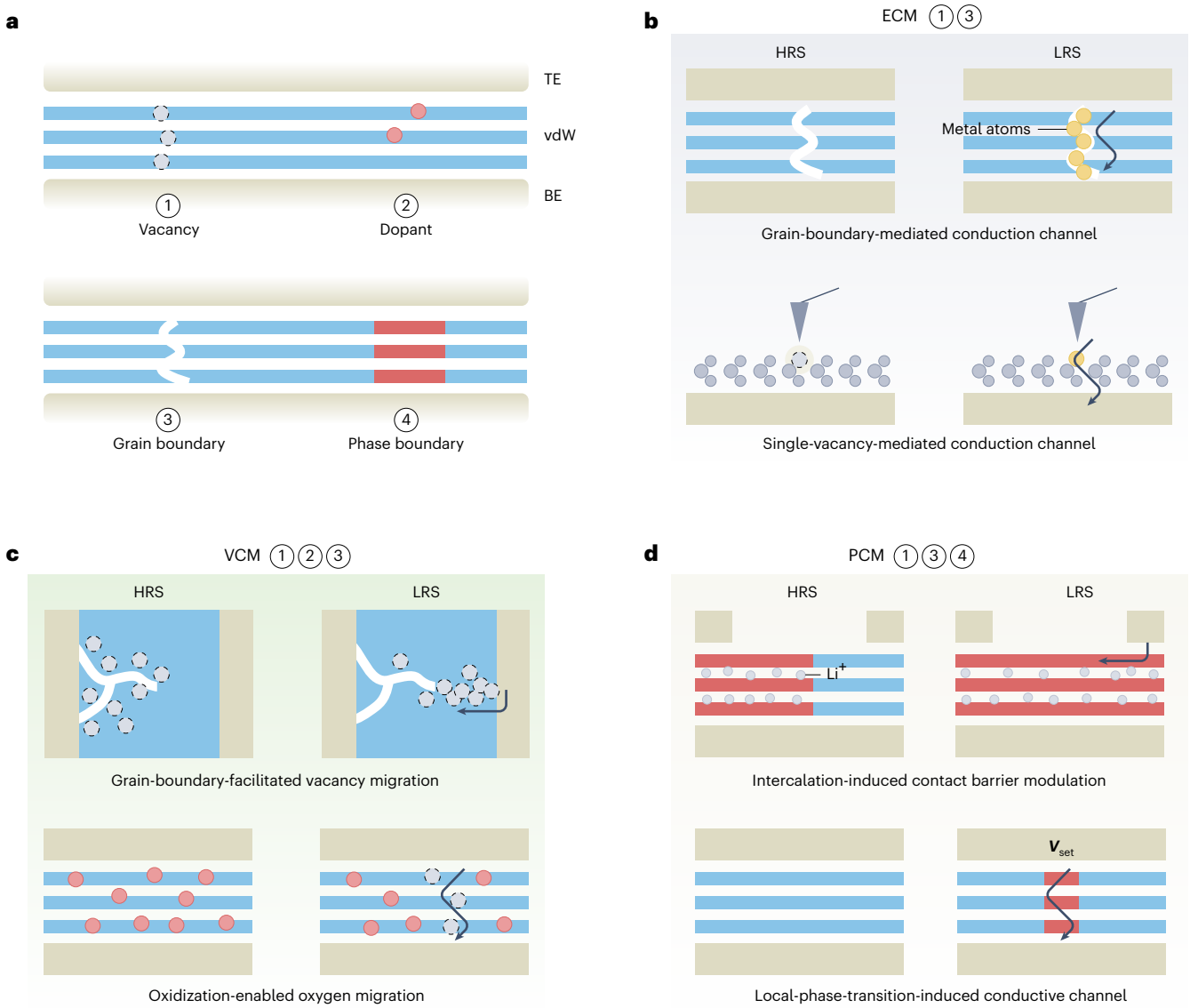

Fig. 2 | Imperfection-enabled switching mechanisms in vdW memristors. **a**, A schematic of a typical vertical vdW memristor with various imperfections. The numbers indicate different types of imperfection. In the case of lateral devices, the metal electrodes should be arranged at the left and right ends of the switching medium. TE and BE represent the top and bottom electrodes, respectively. **b**–**d**, Illustrations of the HRS and LRS of three resistive switching mechanisms. Each of them is contributed by a specific set of imperfections. The numbers indicate the related imperfection types. **b**, In ECM switching, vacancies and grain boundaries facilitate the formation of the conduction channel. The yellow circles represent metal atoms from the electrodes. **c**, In VCM switching, the intrinsic vacancies (for example, chalcogen vacancies) or introduced vacancies (for example, oxygen vacancies) dominate the switching process by forming conductive channels or modulating the contact barrier height. The presence of grain boundaries favours vacancy migration. **d**, In PCM switching, chemical intercalation or external electric field can induce reversible phase transition between two crystalline phases with different conducting properties[22,72]. The involved phases include 1T metallic phases, 2H semiconducting phases and their distorted structures (for example, T_d, T′ and $2H_d$ phases).

on top of a gold thin film form a Au/MoS_2/Au memristor. A gold atom occupying a single-sulfur vacancy serves as the conductive bridge. The ECM switching process involves dissociation of the gold ion/atom, moving on the surface of a defect-free region, occupying a vacancy site (SET) and departing from the vacancy site (RESET). However, there are two possible pathways for the switching process depending on whether a redox process of the gold atom occurs. In the first pathway, the gold atom undergoes ionization and reduction at the two electrodes, akin to the case of conventional oxide-based electrochemical memristors. The second pathway does not involve the redox process. An individual gold atom can detach itself from the electrode since gold has a relatively low atomization enthalpy[47]. The free gold atom is rather unstable. It would diffuse along the defect-free region and be captured by a vacancy site since the gold atom absorption is energetically more favourable at a vacancy site (route 1) than in the defect-free region (route 2). The rupture of the metal bridge needs to overcome the departing barrier energy to reset the sulfur vacancy, which defines the threshold voltage of the RESET operation. As a result, devices with different electrode materials and vacancy types possess different switching thresholds and characteristics[54]. For instance, a low binding energy between metal atoms/ions and vacancies results in a low switching voltage (for example, Ag/$MoTe_2$); a high binding energy typically leads to a high switching stability (for example, Ag/h-BN). Moreover, the absorption process and the kinetic profile are closely related to defect density and distribution[21]. Beyond the single-defect case in monolayer media, the physical processes of ECM switching in multilayer media are more complicated, especially if grain boundaries or dopants are involved.

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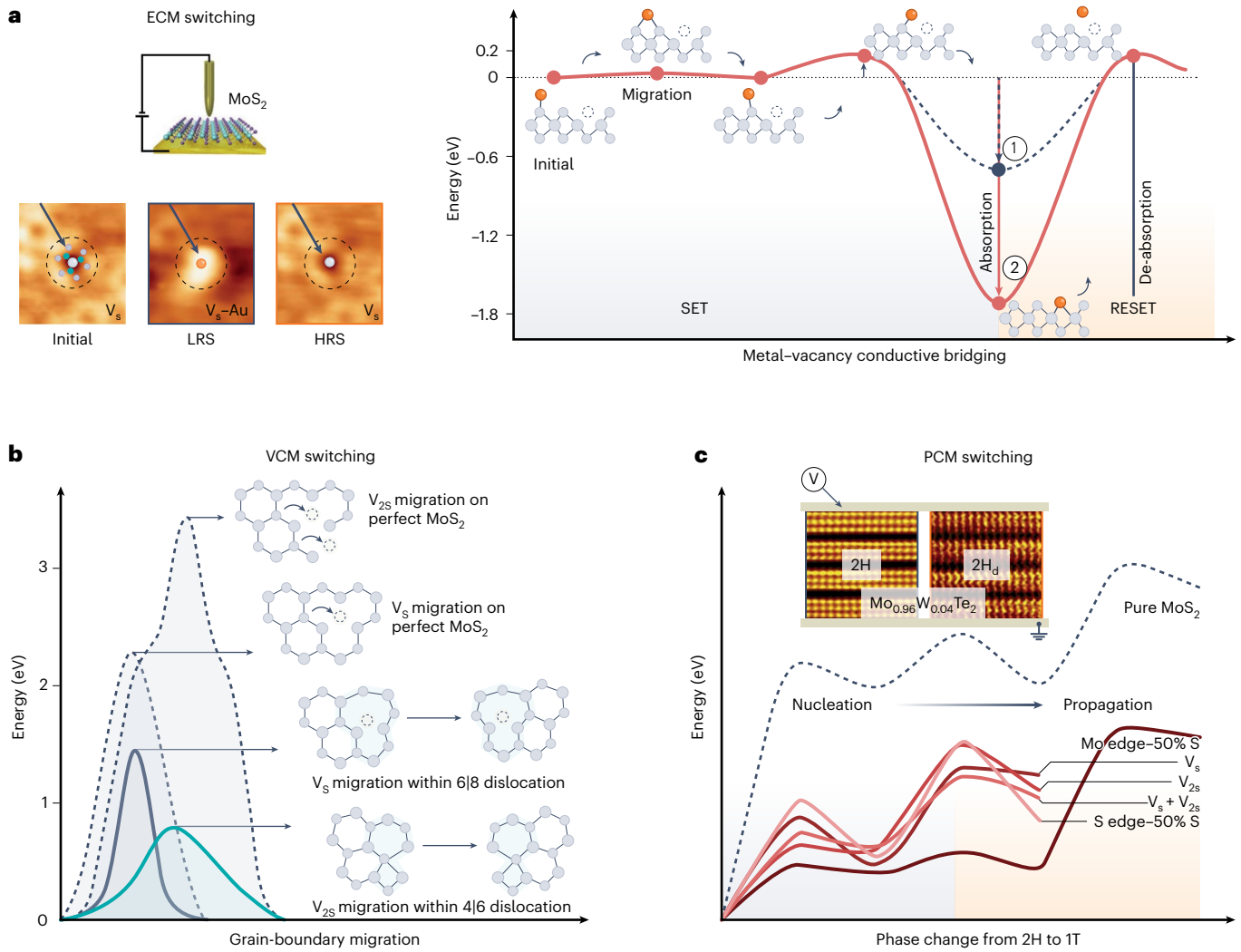

Fig. 3 | Imperfection-related kinetics of the resistive switching processes. **a**, Right: typical energy paths and corresponding structural schematics of metal atom diffusion in ECM switching[19,47]. The absorption process of the metal atom at a sulfur vacancy site releases energy and increases local conductance, corresponding to the SET operation. The desorption process consumes energy and results in a conductance decrease, corresponding to the RESET operation. Left: the in situ scanning tunnelling microscopy images, revealing the evolution of a defective MoS_2 monolayer during the switching process—an unoccupied sulfur vacancy (Initial), a vacancy filled by a Au atom (LRS) and a reset vacancy (HRS). **b**, The energy paths and corresponding structural schematics for vacancy migration in VCM switching[21,59]. The migration of a V_S or a V_{2S} faces a lower energy barrier on a MoS_2 surface with dislocations (6|8 and 4|6 dislocations) than on a pristine region, revealing the role of grain boundaries in promoting vacancy migration. **c**, The calculated energy paths of phase transition in PCM switching[72,74]. It involves the 1T phase nucleation and propagation on a base of 2H MoS_2 with different statuses: perfect region, V_S, V_{2S}, two separated V_S ($V_S + V_S$), sulfur edge with 50% sulfur coverage (S edge–50% S) and molybdenum edge with 50% sulfur coverage (Mo edge–50% S). Compared with the perfect region, defective areas have lower energy barriers for phase transition. Inset: high-magnification annular dark-field scanning transmission electron microscopy images of the 2H phase and the distorted transient $2H_d$ phase of a $MoTe_2$-based ($Mo_{0.96}W_{0.04}Te_2$) memristor driven by electric field. The *x* axis in **a**–**c** represents the reaction coordinate of the corresponding switching processes. Panels adapted with permission from: **a**, ref. 19, Springer Nature Limited; **b**, the curve for V_S migration within 6|8 dislocation, ref. 21, Springer Nature Limited; **b**, other curves, ref. 59, John Wiley and Sons; **c**, ref. 72, Springer Nature Limited.

Valence-change mechanism

The migration and redistribution of the anions (or equivalently charged vacancies), typically driven by electric field and/or thermal effect, can lead to conductance change in vdW media sandwiched by inert electrodes. This type of switching mechanism, VCM, is mainly based on the modulation of either filamentary conductive channels or contact barrier heights. The commonly involved imperfections in VCM are vacancies and grain boundaries[15,16,20,24,37,43,55–57]. Mobile vacancies either naturally exist in vdW materials—for example, chalcogen vacancies in TMCs—or can be introduced via extra treatments—for example, oxygen vacancies in oxidized TMCs (Fig. 2c).

The characteristics of VCM switching are primarily determined by ion-migration energy barriers[58]. In TMCs, the intrinsic chalcogen species, such as sulfur, selenium or tellurium anions, possess lower migration barriers than transition metal cations. Therefore, they are more mobile and dominant in VCM switching[16,24]. Grain boundaries can further reduce the migration barrier of vacancies and facilitate VCM switching. This phenomenon was experimentally confirmed in monolayer TMCs. Researchers revealed that the reconstruction of grain boundaries in a MoS_2 monolayer promotes the migration of neighbouring point defects[21,59]. Compared with the defect-free region, the migration energy barrier is lowered by about 40% for a single-sulfur vacancy (V_S) within the 6|8 dislocation core and reduced by 80% for a double-sulfur vacancy (V_{2S}) within a 4|6 dislocation core (Fig. 3b).

Grain-boundary-mediated VCM switching was first demonstrated in a lateral monolayer MoS_2 memristor[16]. Atomic force microscopy and

electrostatic force microscopy captured the reversible migration of grain boundaries in the switching process. The external electric field drives the lateral motion of sulfur vacancies to modify the Schottky barrier heights at the metal–semiconductor interfaces and switch the device between high- (vacancy depletion) and low- (vacancy accumulation) resistance states (Fig. 2c). Subsequent studies revealed that diverse grain-boundary topologies enhance the degree of freedom in shaping the switching polarity, volatility, linearity and additional gate tunability[20]. Although a couple of desirable characteristics are gained in grain-boundary-mediated memristors, two major engineering issues need to be addressed. First, the strong dependence of switching features on grain-boundary topologies gives rise to severe device-to-device variation. Second, the grain size, typically ranging from micrometres to tens of nanometres, limits the density of grain boundaries and the minimal size of the device, imposing a ceiling on their scalability. Both issues might be partially resolved by improving the synthesis homogeneity of vdW films or intentionally creating grain boundaries via electron-beam or laser irradiation[15].

Compared with intrinsic chalcogen and metal ions, oxygen ions possess an even lower migration barrier and a higher mobility[12,24,60]. Thus, the oxidized vdW materials have been studied as the switching media for realizing an ultrathin switching layer, lower energy consumption and reduced switching variation (Supplementary Fig. 1 and Supplementary Table 2)[12,24,37,55,61,62]. Oxygen element can be introduced into vdW materials by several gentle oxidization processes, such as thermal oxidization, oxygen plasma and ultraviolet ozone treatment[63,64]. For air-sensitive materials, natural oxidization under ambient conditions is adequate[65,66]. The substitutional oxygen ions can be redistributed by electric field, thermal gradient or chemical potential difference, leading to two types of VCM switching dominated by interface contact barriers and nanoconductive channels, respectively. The switching type is related to the specific oxidization method and oxidative topologies. In a mild low-temperature thermal oxidization, the thickness of the oxide layer is generally limited to less than 3 nm. The relevant switching characteristics are mainly determined by the metal/oxide interface because the thin oxide layer (the reservoir of oxygen ions) enables oxygen vacancy (V_O^{2+}) migration and metal valence change[37,61]. A region abundant in oxygen ions possesses a higher metal valence, leading to a higher interface contact barrier and lower conductance, and vice versa. In contrast to the interface effect, if oxidization occurs in a moist environment, many oxygen ions can deeply penetrate the vdW host and substitute the chalcogen ions of TMCs[24]. This creates more in-depth oxygen vacancies and allows them to form conductive bridges between the top and bottom electrodes. The motion of V_O^{2+} during the SET and RESET processes was visualized in a thermally oxidized $MoS_{2-x}O_x$ memristor, primarily involving thermophoresis and thermal dissolution (Fig. 2c)[24]. Additionally, using graphene to replace metal electrodes can provide a thermally and chemically stable interface to protect the conductive channel and avoid ion penetration into metal electrodes, which can reduce device failure caused by channel overgrowth[11,12].

Phase-change mechanism

TMCs have various crystalline phases with distinct electrical conduction properties[67]. A typical example of PCM switching is based on the reversible phase transition between metallic 1T, semiconductive 2H or their distorted structures of TMCs to modulate interface contact barriers or local conduction channels. Unlike the conventional phase-change memory devices that undergo a phase transition between amorphous and crystalline states, the phases involved in vdW-based PCM switching are all crystalline states with slight differences in atom dispositions[68]. Thus, the switching between the semiconductive and metallic phases of TMCs involves a lower energy barrier. The low phase transition barrier promises low-energy-consumption memristors; on the other hand, it may compromise the retention of memory states.

The phases of TMCs feature different electron arrangements in the *d* orbital of the transition metal atoms, and a slight variation of charge density can change their relative stability. The structural change of TMCs could be achieved by the electrostatic gating effect or interface charge injection[69]. Among the most investigated TMCs (MX_2, M = Mo, W; X = S, Se, Te), tellurides (for example, $MoTe_2$) are expected to possess the lowest polymorphic energy difference[67]. For example, a moderate electric voltage (usually below 1 V) can switch the resistance of a $MoTe_2$ memristor by forming a $2H_d$ conduction channel in the 2H semiconductive region (Fig. 2d). The conduction channel in TMCs can be vertically formed in a tiny region, indicating the scalability potential of PCM devices; however, it also implies switching variation if the randomness of the nanofilament formation cannot be well controlled. Compared with conventional phase-change materials such as $Ge_2Sb_2Te_5$, the phase transition between crystalline phases also endows TMCs with a fast switching speed (5 ns)[70,71]. Further studies uncovered that alloying engineering can be used to tune the PCM switching process. Taking $Mo_{1-x}W_xTe_2$ memristors as an example, the incorporation of W can facilitate the SET process since the 2H to 1T′ transition of WTe_2 is more thermodynamically favourable at room temperature than is that of $MoTe_2$[67,72].

Chemical intercalation is commonly used to achieve PCM switching owing to the layered feature of TMCs[73]. It results in the phase transition through transferring charges from the intercalants to the transition metal atoms and changing the electronic structure of the TMC. Thus, the motion of intercalated ions driven by electric field leads to the motion of phase boundaries in TMCs. Controlling lateral ion motion through chemical intercalation can modulate the charge transport barrier at the contact interface of MoS_2 and metal electrodes. A forward voltage drives Li^+ to move toward the right-hand metal electrode in Fig. 2d, leading to motion of the 1T/2H phase boundary in the same direction, thereby realizing an ohmic contact; a reverse voltage removes the Li^+ from this electrode region, resulting in opposite motion of the phase boundary and an elevated Schottky contact barrier. The intralayer migration barrier determines the mobility of the alkali metal ions for either drift or spontaneous diffusion. Thus, there is a trade-off between the required operating voltage and the retention of PCM devices. In addition, similarly to the planar vacancy migration, by controlling the migration direction of intercalants, researchers realized multidirectional resistance modulation in PCM devices. This property can be used to implement the multiple interactions between artificial synapses[22].

The switching process of PCM is also influenced by vacancies, grain boundaries or dopants in the switching region[74]. These defects can affect the nucleation and propagation of phase transition. For example, sulfur vacancies favour the resistive switching from HRS to LRS because the presence of one sulfur vacancy can reduce the energy barrier of the nucleation step from 2H to 1T phase transition by 60% when compared with a defect-free region (Fig. 3c)[74]. Introduced dopants, such as Re or Tc atoms in MoS_2 flakes, provide extra charges for filling incomplete orbitals and stabilizing the metastable phases, which benefits the stability of the PCM switching[18].

It is worth noting that some of the above-mentioned material imperfections can serve as charge traps by providing localized states. These localized states may impact the carrier transport in the dielectric materials and hence the electrical properties of devices. Some studies claim that charge trapping/detrapping events can lead to resistive switching in vdW devices[75]. However, other possible switching mechanisms, such as ECM or VCM, cannot be excluded. The exact impact of the charge trapping/detrapping event on the memristive switching process is still controversial and requires more solid evidence.

Electronic applications of vdW memristors

Different types of memristive switching show advantages in different aspects of performance metrics (Fig. 4c,d and Supplementary Table 3). They provide a palette of device designs for various applications

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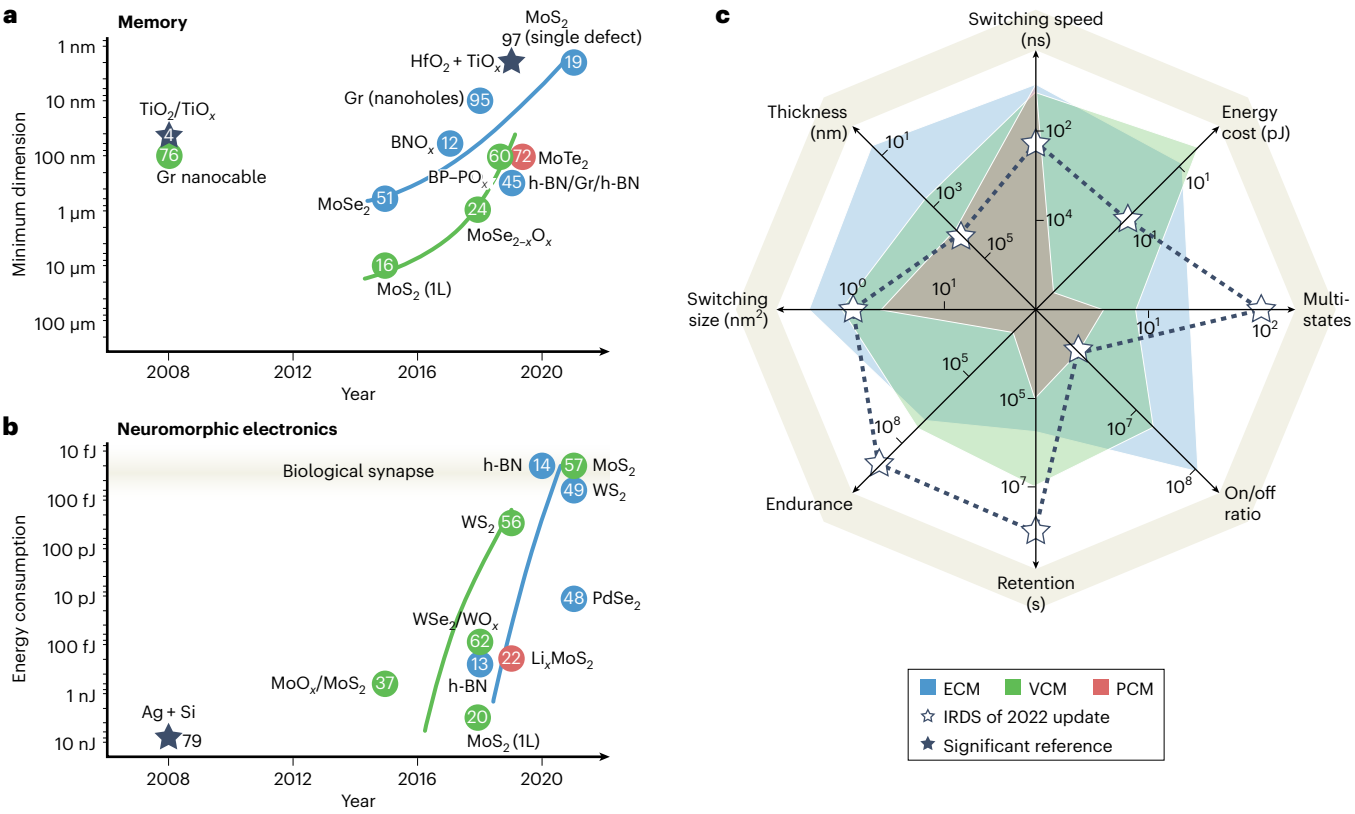

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Memristor	Switching layer thickness (nm)	Switching dimension (nm)	Switching speed (S_{speed}) (ns)	Switching energy (E_{con}) (pJ bit^{-1})	Multiple state number	HRS/LRS ratio	Retention (s)	Endurance (cycles)
ECM	0.33 (ref. [46])	2 (ref. [19])	10 (ref. [49])	0.02 (ref. [14])	25 (ref. [14])	10^8 (ref. [44])	3×10^6 (ref. [49])	10^7 (ref. [50])
VCM	0.7 (ref. [16])	25 (ref. [43])	13 (ref. [56])	0.02 (ref. [57])	8 (ref. [57])	2×10^7 (ref. [60])	10^7 (ref. [77])	2×10^7 (ref. [24])
PCM	2 (ref. [73])	100 (ref. [72])	5 (ref. [72])	30 (ref. [72])	4 (ref. [22])	10^6 (ref. [72])	10^5 (ref. [22])	10^3 (ref. [73])
Non-vdW	3 (ref. [8])	2 (ref. [78])	0.085 (ref. [78])	0.115 (ref. [78])	2,048 (ref. [3])	$>10^{10}$ (ref. [78])	$>10^8$ (ref. [78])	$>10^{10}$ (ref. [78])

Fig. 4 | The development and benchmarks of vdW memristors for various applications. a,**b**, Minimum dimension and energy consumption are selected as the representative metrics for memory (**a**) and neuromorphic electronics (**b**), respectively. Circles and guiding lines of different colours correspond to different switching mechanisms. Filled stars indicate some examples based on non-vdW materials for each application. The numbers in the symbols are the respective reference numbers. The top yellow region in **b** highlights the energy cost per spike in biological synapses (10–100 fJ). Gr, graphene; BP–PO_x, black phosphorus–phosphorous oxide; 1L, monolayer. **c**, Radar graphs of the critical benchmarks for three types of switching mechanism. Open stars indicate the performance requirements set by ref. 103. Different coloured regions represent different switching mechanisms. **d**, The values corresponding to the graphs in **c**. Several representative non-vdW resistive switching devices are also included for comparison.

(Fig. 4 and Supplementary Fig. 2). In this section, the state-of-the-art vdW memristive devices for data storage, neuromorphic electronics and radiofrequency switches are summarized.

Memory

One of the most effective strategies for realizing memory cells with ultrahigh density and capacity is to reduce the device size. The enhancement of integration density for traditional transistor-based memory has been approaching an end. As an alternative, vdW-based memristors enable resistive switching in subnanometre-thick media without compromising the switching window or reliability (Supplementary Fig. 1a).

From the perspective of device miniaturization, Fig. 4a maps the development of vdW memristive devices in terms of time and feature dimension. Although resistive switching in a graphene nanoscale system was observed as early as 2008, the actual switching mechanism was proved to be the breakdown of oxide substrates instead of the proposed nanogap between graphene flakes[76]. Solution-processed memristors based on VCM switching attracted attention due to their low-temperature fabrication[37,55,77]. Oxidized vdW materials were then employed in VCM switching devices to obtain exceptional thermal robustness and durability (Fig. 5a and Supplementary Fig. 1c)[12,24]. The feature sizes of the devices mentioned above are all at a tens-of-micrometres level, possibly due to the difficulty of fabrication. Subsequent studies on PCM switching demonstrated local phase transformation within several crystal cells, showing its potential in further size downscaling[71,72].

Over the past five years, imperfection-engineered ECM switching has gained more research attention since the conductive channels can be repeatably manipulated within a sub-10-nm^2 area[13,45–48,52,53]. For example, the permeation of metal atoms into an oxidized h-BN

bilayer can enhance the local electric field, leading to a promoted ion hopping process and a lowered switching threshold[12]. Since 2017, Lanza et al. have engineered various defects in CVD-grown h-BN films for realizing rich ECM switching properties, ultralow switching energy and improved device yield[13,14,41,52]. Further feature size shrinkage was achieved by manipulating a single point defect in monolayer TMCs with a 2 nm footprint[19].

Important metrics of vdW memristors are summarized in Fig. 4d. In terms of scalability and energy consumption, vdW memristors show potential to outperform non-vdW memristors. Nevertheless, the endurance and retention of vdW memristors remain inferior to the state-of-the-art metal-oxide memristors, which is understandable considering that the research on vdW memristors is still at a rudimentary stage. On top of this, these important properties are not well characterized to the upper limit by the existing reports. Note that the retention of PCM memristors is particularly short because the metastable phase of TMCs is vulnerable to thermal noise and tends to spontaneously relax to the thermodynamic stable phase due to the low phase transition barrier.

Neuromorphic electronics

Implementing deep learning algorithms in conventional von Neumann computers encounters a critical technology challenge due to the overwhelmingly frequent data transportation between the physically separated processing and memory modules, incurring severe energy and time inefficiency[78]. This motivates the hardware innovation represented by neuromorphic electronics. The main idea of neuromorphic computing is to build artificial neural networks that not only compute in memory but also physically mimic the synapses and neurons in biological nervous systems, which can implement biological learning rules to fulfil complex learning and cognitive tasks, reduce power consumption and accelerate the learning process[79,80].

One crucial part of synapse emulation is to implement various modes of synaptic plasticities, such as short- and long-term plasticity, spike-timing-dependent plasticity and heterosynaptic plasticity. Short- and long-term plasticity have been demonstrated using MoS_2 or oxidized MoS_2 memristive devices on flexible substrates[37,81]. Spike-timing-dependent plasticity, which is a popular variant of the Hebbian learning rule, was achieved in a MoS_2 memristor via the formation and rupture of the metallic conductive pathway along the grain boundaries[53]. Heterosynaptic plasticity was then implemented in a single multigate MoS_2 memtransistor by tuning in-plane ion migration. The additional gate tunability enhances the modulation range of the switching threshold and zero-bias resistance, potentially enabling applications such as fault-tolerant neural networks (Fig. 5b)[20]. In terms of energy cost, most vdW synapses remain at a nanojoule to picojoule level, still far from the energy efficiency of their biological counterparts (Fig. 4b). Several recent studies revealed that this issue could be addressed by properly devising the switching operation protocols. For example, setting a low-level compliance current (CL) can achieve a 20 fJ switching by partially rupturing the conductive pathways in ECM switching devices[14]. However, the improved energy consumption obtained by this strategy necessitates a higher operational complexity (Fig. 5f).

An ideal artificial synapse is expected to meet many other merit requirements, including linear and symmetrical weight update, multiple well defined weight states, large dynamic range, low switching variation and high endurance. Supplementary Table 4 summarizes these metrics of reported synaptic devices based on vdW materials. The dynamic range and the endurance of these devices vary from case to case to a large degree, but they are overall outperformed by the state-of-the-art metal-oxide synaptic devices according to the data in the current literature. However, it is believed that these metrics may not have been pushed to their upper limit in the measurement design of previous reports. In particular, the nonlinearity of conductance change is a common issue of ECM and VCM switching devices, because the physical process (ion drift or diffusion) that dominates the evolution of the conduction channels varies at different stages of switching[82]. Several approaches have been developed to improve the programming linearity of vdW memristors. Chen et al. employed low-level CL in operating few-layer h-BN ECM memristors to achieve 25 linearly increasing conductance states[14].

More complicated functionalities such as information processing and recognition in human brains require dynamic interactions between numerous neurons, dendrites and synapses in neural networks. However, there have been a relatively limited number of studies on artificial neurons and even fewer on artificial dendrites[83]. The pioneering works on vdW-based artificial neurons focus on taking advantage of their volatile switching mechanisms[84,85]. For example, a 1T-TaS_2 memristor based on charge-density-wave phase transition realized tunable stochastic spiking characteristics, similar to the case of biological neurons. The stochasticity originates from the microscopic random reconfiguration of charge-density-wave domains (Fig. 5g).

Radiofrequency switches

A radiofrequency switch is a crucial reconfigurable component of radiofrequency circuits, which play a core role in high-frequency communication and Internet of Things technologies. A high-performance radiofrequency switch is expected to have low on-state resistance (R_{on}) and low off-state capacitance (C_{off}) to afford low insertion loss, high isolation and high cutoff frequency $f_c = 1/2\pi R_{on}C_{off}$. Low power consumption and scalability also become more critical for 5G and 6G applications.

For complementary metal–oxide–semiconductor transistor (CMOS)-based radiofrequency switches, static energy dissipation is the knottiest problem, as they are volatile and require a constant non-zero hold bias. This inspires the development of emerging non-volatile devices. Early attempts to develop memristive non-volatile switches used planar switching media such as a solid-state electrolyte (for example, $GeSe_2$) or an air nanogap (Supplementary Fig. 3)[86]. However, technical difficulties mainly related to silicon-based thermal budget barriers impede their industrial application. The emergence of vdW memristors provides a possible solution[1,87]. Taking an ECM switching-based h-BN atomristor as an example, its non-volatile nature results in zero static power dissipation, and the low R_{on} (Fig. 5c) guarantees a high cutoff frequency to cover the entire 5G spectrum (100 GHz)[87]. Given that C_{off} decreases proportionally with a smaller switching area, the area-independent R_{on} of vdW switches helps circumvent the trade-off between performance and device scalability. On the basis of this advantage, downscaled MoS_2 switches (0.04 μm^2) demonstrate the data transmission ability to satisfy 6G communication requirements[88]. However, the endurance of ECM atomristors is problematic due to the low structural robustness against the high operating current.

Challenges facing vdW memristor applications

Despite the substantial research progress made in defect physics, switching mechanisms and device benchmarking of vdW memristors over the last decade, some key issues still prevent their practical commercialization. To fully exploit the advantages of vdW memristive materials, further research on imperfection engineering is needed for optimized device design and characterization, variation control and system-level integration.

Imperfection engineering of vdW memristors aims to customize the imperfection types, distributions or tunability in vdW materials to achieve desirable memristive characteristics. From the viewpoint of physics, the imperfection-mediated switching mechanisms of vdW memristors are similar to those of metal-oxide memristors, especially for ECM and VCM[7]. However, imperfections in vdW materials provide a larger engineering space for more precisely tuning switching behaviours. First, a vdW system possesses more imperfection

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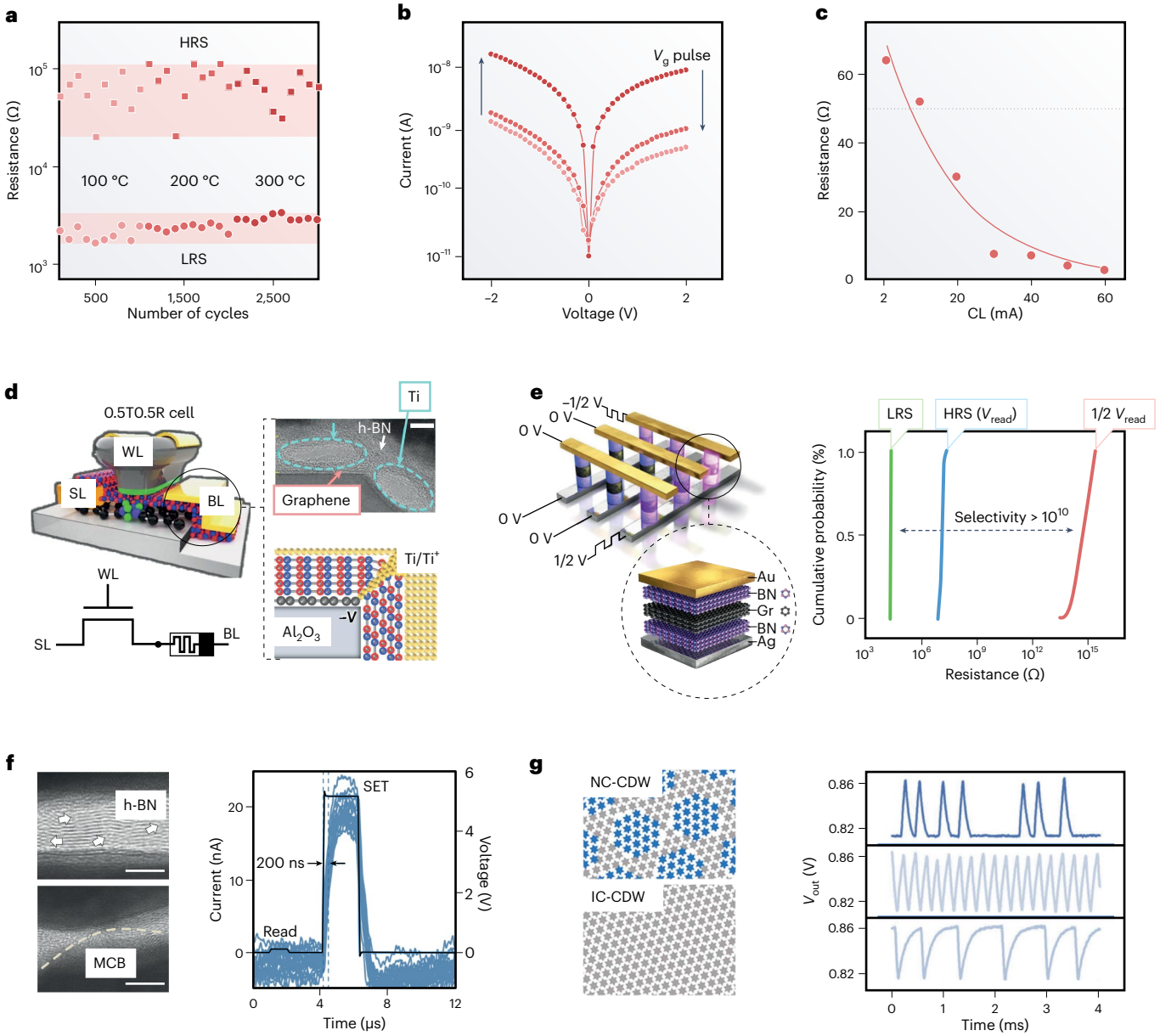

Fig. 5 | Selected special characteristics of vdW memristors. a, A $MoS_{2-x}O_x$/graphene memristor that can tolerate high operation temperatures. The switching between LRS and HRS remains robust as the temperature increases[24]. **b**, Gate voltage (V_g)-tunable current–voltage characteristics of a polycrystalline MoS_2 memtransistor[20]. **c**, LRS resistance of a monolayer h-BN memristor as a function of CL[87]. The low resistance (below 50 Ω) is critical for radiofrequency applications. **d**, Left: schematics of a vdW heterostructure 0.5T0.5R cell[49]. The key design features of this ultracompact 0.5T0.5R cell are the dielectric layer and edge contact shared by the transistor and the memristor. WL, word-line; SL, source-line; BL, bit-line. Right: cross-sectional TEM image of the h-BN memristor with a Ti conductive filament and simulated switching mechanism of the SET process. The scale bar in the TEM image is 5 nm. **e**, Left: schematics of a memristor array with self-selectivity and a zoomed-in single device structure (Au/h-BN/Gr/h-BN/Ag)[45]. Right: resistance variation of the selected cell at LRS, HRS and half-selected states. **f**, Left: cross-sectional TEM images of a Ag/h-BN/Au device after applying a current–voltage sweep with different values of CL. The small conductive islands at CL = 10 nA (top) and the well developed conductive filament at CL = 2 mA (bottom) indicate the threshold switching behaviour of the h-BN device[13]. Both scale bars are 4 nm. The arrows in the top panel mark the local defect paths in h-BN switching medium. The dashed line in the bottom panel describes the developed metallic conductive bridge (MCB) Right: the *I*–*t* curve (blue) of the Ag/h-BN/Ag memristor under a fast voltage pulse measurement (black curve) reveals the energy-efficient switching[14]. **g**, Schematics of the atomic structure of two different phases of 1T-TaS_2. NC-CDW and IC-CDW represent the nearly commensurate and incommensurate charge-density-wave phases, respectively. Output voltage waveforms of a 1T-TaS_2 neuron show different oscillation behaviours at various bias conditions, including stochastic oscillation (top and bottom) and regular oscillation (middle). Panels adapted with permission from: **a**, ref. 24, Springer Nature Limited; **b**, ref. 20, Springer Nature Limited; **c**, ref. 87, Springer Nature Limited; **d**, ref. 49, IEEE; **e**, ref. 45 under a Creative Commons licence CC BY 4.0; **f**, Left: ref. 13, Springer Nature Limited; **f**, Right: ref. 14, Springer Nature Limited; **g**, ref. 85, American Chemical Society.

types. The diverse anion types that dominate the VCM switching in TMCs and phase boundaries between regions of semiconductor and metal states are unique imperfections in vdW memristors. Second, more controllability over the distribution of imperfections can be realized in vdW systems. The well defined grain boundaries obtained via post-treatments can lower the ion-migration barrier and thus the energy consumption, and also reduce switching variation[13,16]. Similarly, if the vacancy density can be precisely controlled, a single-defect

memristor crossbar array with the smallest footprint can be expected for highly dense memory chips[19]. Moreover, a vdW system provides more tunability of switching features in lateral devices. For instance, the conductance of a vdW memtransistor can be tuned by a gate voltage, which is not effective for the traditional metal-oxide lateral memristors because they typically feature a large bandgap[20]. In addition, we can use intercalation ions to define the phase boundaries and the intercalation ion drift can be controlled via multiple electrode pairs in different directions, which enables the emulation of biological synaptic interactions[22].

Design and characterization

The uncovered memristive behaviours in many vdW materials are still far from being fully understood. The diversity of defects in vdW materials implies the coexistence of multiple switching mechanisms in a single system, for instance, the coexistence of ECM and VCM switching in oxidized MoS_2 (ref. 55). This incurs technical difficulties in precisely probing the dynamics of a specific type of imperfection and evaluating its contribution to the overall switching process. In addition, new physical phenomena and properties emerge with new materials, such as the charge-density-wave phase transition in 1T-TaS_2 (ref. 85). Expansion of the vdW family inevitably complicates the material selection for an optimized device design[39,85]. To overcome these problems, device modelling analysis and in situ characterizations should be combined to understand the underlying mechanisms and seek optimal device designs.

Advanced physical modelling via machine learning and first-principles calculation is proposed to efficiently predict the role of critical imperfections in shaping resistive characteristics. Taking ECM switching as an example, the optimization includes identifying promising switching media, training defective structure models by introducing metal atoms, and predicting ideal metal electrode candidates via evaluation of the binding energy barriers (Fig. 6a)[54]. Different barrier heights lead to different memristive switching behaviours in the corresponding ECM memristors, as the formation and motion of the defects are regulated by the energy profile (Fig. 6b)[21,47]. Regarding the host materials, h-BN provides higher energy barriers than the TMC group. For PCM switching, tellurides and their alloys serve as a thermodynamically more favourable platform for phase transition[36,67].

As to mechanism exploration, in situ microscopic techniques have been employed to uncover the resistive switching process in an all-surface 2D switching system (Supplementary Table 1). Commonly used in situ techniques include conductive atomic force microscopy, transmission electron microscopy (TEM) and scanning transmission X-ray microscopy. They are mainly used to visualize critical physical processes, such as a single-defect evolution, grain boundary migration and localized phase transformation[16,19,22,72]. These observations provide crucial inputs for constructing the physical models of switching.

Variation control

From the engineering perspective, the variability of the resistive switching process is one of the most critical issues impeding commercialization[89]. For ECM and VCM switching, an effective optimization method to reduce switching variation is to control the imperfection distribution by modifying the growth process or applying a post-treatment.

During material growth, imperfections such as grain boundaries and dopants can be predesigned to suppress switching variation. Efforts have been made to introduce prefabricated precursors or threading dislocations to control the channel formation/rupture in conventional oxides[90]. However, these methods still face non-uniformity problems for large-scale applications. In vdW systems, this issue can be further addressed since the grain-boundary distribution can be engineered via adjusting large-area CVD fabrication[91]. For example, predeposited metal nanoparticles (NPs) (such as Au NPs) can act as the growth nuclei of TMCs. The density of metal NPs defines the size of TMC domains (Fig. 6c(i))[25]. Therefore, the average distance between grain boundaries can be constrained below 5 nm by depositing high-density metal NPs. The vdW switching layer with dense grain boundaries makes the scalable fabrication of memristive devices possible. Predepositing metal nanoclusters (for example, Ag or Cu) serving as seeding materials can provide another approach to predesign the conductive channels for reducing device variation of vdW memristors but still needs more experimental attempts[92].

Post-treatment techniques such as surface plasma, electron-beam exposure or ion bombardment are used to introduce vacancies, grain boundaries or nanopores to confine the conductive channels and optimize switching uniformity. Electron-beam irradiation with nearly atomic-scale spatial resolution can create defective regions and precisely alter the grain-boundary morphology (Fig. 6c(ii))[93]. As a typical example, the properties of the formed conductive channels in $PdSe_2$ flakes were controlled by tuning the applied electron-beam dosage. The partially reset filaments along the created grain boundaries substantially improve the switching uniformity (sixfold) when compared with the totally reset ones[48]. Other researchers used ion bombardment to generate defective nanopores in vdW materials as a new way to regulate ion motion. Pristine graphene films are ion impermeable, but the precreated nanopores allow the ions to pass through[42,94]. By employing vdW films with nanoscale holes as ion sieves, researchers can define the size, distribution and density of the conductive channels (Fig. 6d)[43,50,95]. Furthermore, narrowing the nanopores can restrict the ion species allowed to pass, which can mitigate the high operation current and stuck-ON issues. Even though the proposed post-treatment solutions are theoretically effective for device downscaling, their high dependence on the precision of the equipment employed should be considered.

Integration

The integration of vdW memristors is critical for more practical applications. It has two aspects: integrating vdW memristors with current technology and realizing their scaling potential for ultradense memory arrays.

CMOS components are necessary in the hardware implementation of computing systems based on vdW memristors. While vdW memristor arrays can naturally serve as neural networks, CMOS components are still the best choice for the peripheral circuits[96,97]. Fortunately, vdW memristors are CMOS technology compatible due to the low-temperature synthesis and transfer capability[98]. They can be post-fabricated on a silicon chip through layer-by-layer stacking. A vdW memristor fabricated elsewhere can even be directly embedded in a silicon chip by a precise transfer process. Beyond silicon CMOS technology, it is worth to note that attempts have also been made to demonstrate an all-vdW computing system: for example, by integrating h-BN memristors with WS_2 transistors[49].

Though individual vdW memristors are reported to possess many advantages, system-level demonstrations of vdW memristor crossbars remain rare. This issue mainly originates from the relatively immature synthesis and fabrication techniques of large-area vdW materials. For example, cracks and wrinkles can easily emerge over the transfer process. Several large-scale transfer techniques or transfer-free fabrication methods, such as layer-resolved splitting or adhesive wafer bonding methods, have been developed to address this challenge[99]. Moreover, more area-efficient architectures and advanced integration technology are still needed to take full advantages of vdW memristors at a system level.

VdW memristors have two notable merits in 2D planar integration. From the point of view of the technology node, single-defect atomristors possibly have the smallest switching footprint thanks to the one-atom-thick switching layer. The theoretical device density can reach 160 Tbit $in.^{-2}$ at a 2 nm pitch, comparable to a TiO_x/HfO_2 crossbar array of 2 nm feature size, although the practical realization is still facing technical difficulties[19,100]. Also, the unique properties of vdW materials enable more integration architectures. The traditional 1T1R

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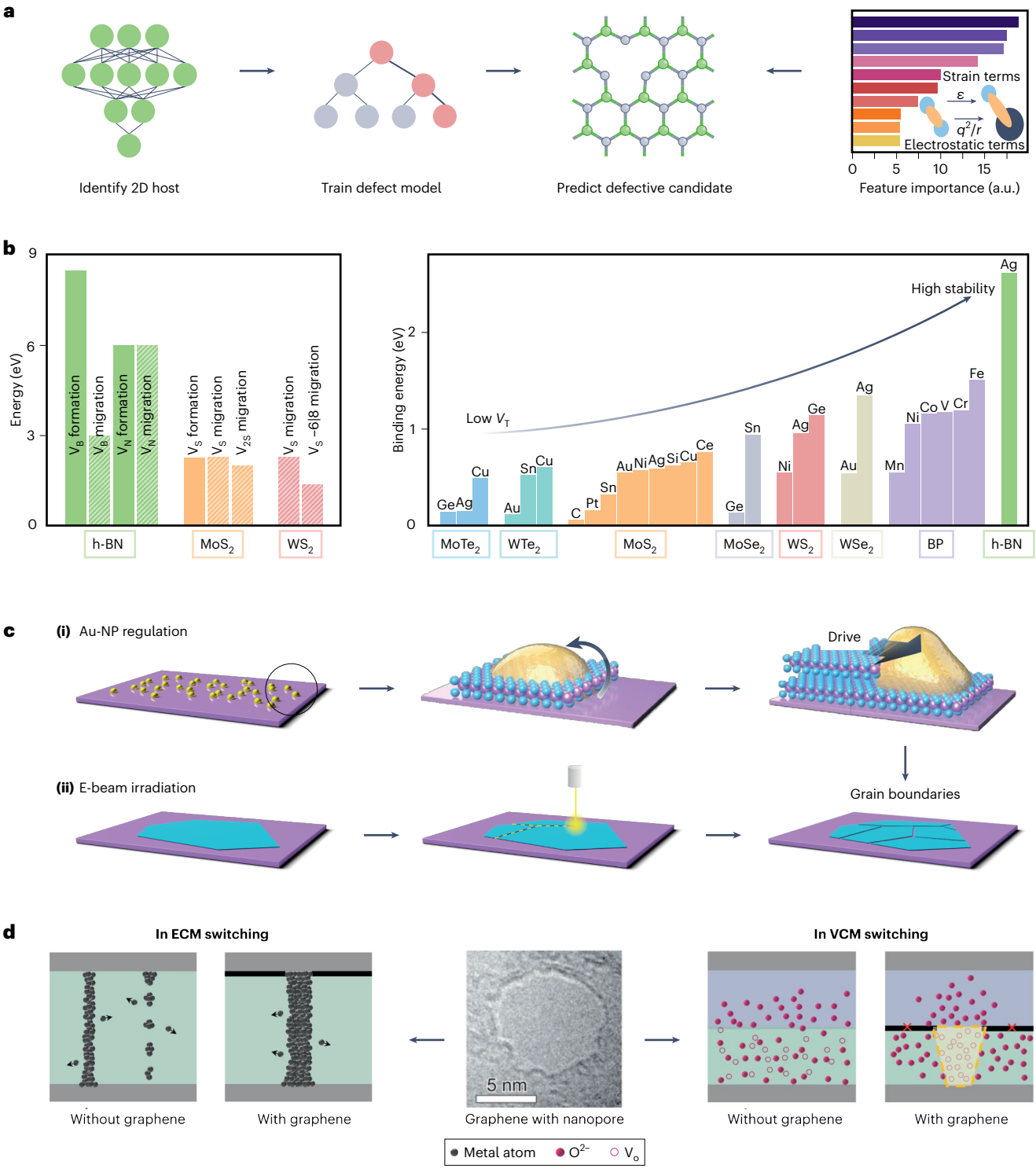

Fig. 6 | Imperfection engineering to improve the performance of vdW memristors. a, A workflow schematic of a deep learning method for predicting point-defect-enabled ECM switching in vdW materials. It involves identifying promising 2D host materials, training defective structure models and predicting ideal defect candidates. The rightmost panel shows various features in computing the defect formation energy. Top to bottom: mean number of *p* valence electrons, defect species chemical potential, electronegativity, mean number of *p* valence electrons[a], energy of highest occupied molecular orbital, mean atomic weight[a], number of valence electrons, mean atomic weight, chemical fingerprint, vdW radius. [a]The absolute value of a pristine or defective structure, and the others are the differences between the two systems[54]. **b**, Left: the calculated energy barriers of the defect formation and migration in various vdW materials. Right: calculated binding energies of various vacancies and metal atoms. In theory, a lower binding energy leads to smaller threshold voltages (V_T) for resistive switching, while a higher binding energy results in higher switching stability. **c**, Engineering the grain boundaries in vdW materials via (i) modifying material preparation or (ii) a post-treatment process[25,48]. Predeposition of metal NPs is a typical method to control grain size. A common method to tailor grain-boundary topologies is electron-beam irradiation. **d**, Engineering the defective nanopores in 2D films to define the size and distribution of conductive filaments. The middle TEM image shows the morphology of a graphene film with an 8 nm nanopore. Left: in ECM memristors, a defective graphene film between the active electrode and switching medium leads to a better-defined filament than found in a device without a graphene film. Right: in VCM switching, defective graphene as an ion-blocking layer confines the overinjection of oxygen vacancies[43,50,95]. Panels adapted with permission from: **a**, ref. 54, American Chemical Society; **c**, ref. 25 under a Creative Commons licence CC BY 4.0; **d**, ref. 42, Springer Nature Limited.

(one transistor and one resistor) design has been commonly used due to the anti-interference capability; however, the addition of the transistor compromises the scaling advantage of memristors. A 0.5T0.5R memory cell based on stackable vdW layers was recently proposed as a possible solution (Fig. 5d)[49]. It features a shared resistively switchable insulator (h-BN) and an edge contact (graphene) between the transistor and the memristor, achieving a more area-efficient memory unit. However, such a scenario can only reduce the cell area if the transistor and the memristor are assumed to be fabricated in the same plane, and show no clear advantage compared with the state-of-the-art 3D stacking 1T1R arrays[3]. Another strategy to achieve simplified system integration is to build memristive devices with self-selectivity. For example, in a vertical Ag/h-BN/graphene/h-BN/Au heterostructure, the graphene film with ion impermeability and h-BN films with defective vacancies enables the formation of a volatile Ag filament and a non-volatile boron filament in two h-BN regions, respectively. Such a design integrates both volatile and non-volatile kinetics in a single cell and leads to a 10^{10} self-selectivity (Fig. 5e)[45].

3D integration architectures of vdW systems exhibit several advantages over bulk materials due to their atomically thin bodies and low-temperature fabrication. Compared with traditional silicon technology with thermal budget incompatibility issues, low-temperature fabrication for vdW devices (below 400 °C) facilitates the back-end-of-line integration process. In addition, vertically stacked vdW crossbar cells are supposed to be promising in reducing the integration thickness when compared with a 3D oxide system[101]. However, the fabrication requires more lithography steps, probably compromising the low cost and high yield. To overcome this difficulty, the recently reported vertically constructed 3D oxide memristors, which use rolled switching media and metal pillow electrodes, can provide some inspiration to reduce the lithography need[102].

Outlook

The compositional or structural imperfections in vdW materials lead to rich memristive switching mechanisms and offer several opportunities to engineer and tune their switching properties. There are three key types of memristive mechanism, each of which is associated with a specific group of imperfections. Such switching mechanisms provide vdW memristive devices with unique characteristics, including ultrasmall switching dimensions, multidirectional tunability and high-temperature robustness, leading to various applications, including but not limited to memory devices, neuromorphic electronics and radiofrequency switches.

Research on vdW memristors is still at an early stage of development and the path to commercialization will involve addressing numerous challenges related to mechanism exploration, device design, variation control and system-level integration. To further improve material selection and processing, device fabrication, circuit integration and algorithm implementation of vdW memristive systems, more systematic research on imperfection engineering through device–circuit–algorithm co-design and co-optimization is required.

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J.J.Y., Y.-F.L. and H.W. conceived the concepts and perspectives. M.L., H.L. and R.Z. worked on literature analysis and data collection. M.L., H.L. and J.J.Y. co-wrote the manuscript. All authors contributed to the discussion of content and reviewed and edited the manuscript. J.J.Y. supervised the project at all stages.

Competing interests
The authors declare no competing interests.

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