Architectural Radiation Hardening of CMOS Power Management Circuits through Bias Tuning

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2023 IEEE 41st VLSI Test Symposium (VTS) | 979-8-3503-4630-5/23/$31.00 ©2023 IEEE | DOI: 10.1109/VTS56346.2023.10140031

***Abstract*—Within the space electronics industry, several strategies have been implemented to mitigate heavy ion, neutron, and proton induced radiation effects in CMOS processes, including radiation through process technology alterations and through circuit design, layout, and architecture. In this work, a new method is proposed that adaptively calibrates integrated analog circuits in CMOS bulk technology through bias tuning to create a radiation hardened system. In this technique, the device parameters that vary due to total ionizing dose radiation are monitored using built-in-self-test circuitry. These monitored parameters are used to tune and calibrate circuit level performance parameters. This work analyzes the TID radiation induced performance shifts in three critical power management circuits and uses bias tune in each circuit to recover circuit performance. The three circuits include: a ring oscillator, a bandgap voltage reference, and a non-overlap (dead-time) clock generator.**

***Index Terms*—Calibration, CMOS, analog, power management, radiation hardened, space electronics**

I. Introduction

Recent years have seen significant growth in the space industry, hence an increasing need for space electronics [1]. Inefficient and unreliable power systems continue to be the bottlenecks in electronics for space missions that span anywhere form a few days to multiple decades. These power systems oftentimes comprise of several point-of-load converters (PoL) that convert and distribute power from the central spacecraft bus to numerous spacecraft functions like the engine control, communications, steering control, and exploratory sensors and systems. It is desirable for these PoL converters to maintain performance and efficiencies above 90% over the mission's lifetime. Furthermore, space missions require continuously decreasing design cycle times and increasingly aggressive performance specifications, and would therefore benefit from using commercial circuit design methodologies. Unfortunately, very few state-of-the-art commercial platforms have been deployed in space due to their high rate of expected failures under radiation and temperature fluctuations.

A. Radiation Effects in Electronics

Radiation effects in electronics can be categorized into three types [2]: total ionizing dose effects (TID), single event effects (SEEs) and displacement damage (DD). DDs may also be referred to as non-ionizing dose effects. TID is caused by heavy ions, protons, and gamma rays. TID has long term and cumulative effects that gradually degrade CMOS device parameters, such as transistor threshold voltage shifts, subthreshold currents, parasitic currents, and degradation in electron mobility and transconductance (g_m). SEEs can cause bit-flips within memory and current latch-up, which may result in device damage such as a single event burnout or gate rupture in power devices.

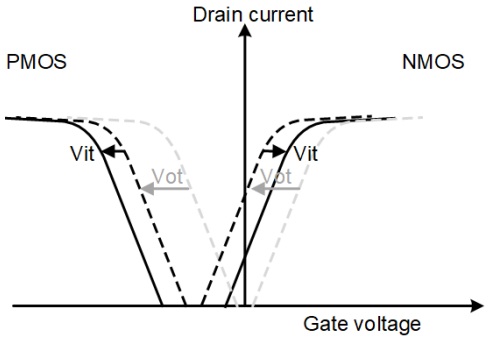


Fig. 1. TID induced threshold voltage shifts in MOSFETs

B. Radiation Hardening Techniques in Circuits

Several methods have been proposed to improve radiation performance in CMOS technologies [3], including reduction/elimination of mismatch causing elements, offset cancellation using averaging techniques in amplifiers [4], employing a combination of JFET-CMOS and BJT-CMOS structures [5] to overcome the mismatch in current mirrors due to TID, reduction of oxide thickness through process modification to mitigate TID, and triple modular redundancy [6] or error correcting codes [7] to mitigate SEE. For inaccessible electronics in harsh space environments, short repair times (if any) are preferred to reduce the cost of maintenance, which can only be achieved with highly reliable radiation-tolerant and self-calibrating electronics [8]. The most popular methods for ensuring reliable CMOS-based electronics pre-silicon fabrication is the prediction of radiation effects in semiconductors using time dependent analytical models [9] for deposition of charge due to ionizing radiation, and circuit synthesis using 6-sigma deviation with Monte-Carlo models provided by the foundry to estimate shifts due to radiation.

A great advantage of in-field integrated circuit parameter monitoring is that the cumulative radiation effects can be observed and recorded in continuous time. The cumulative radiation effects in CMOS circuits are observed through built in self test (BIST) circuits, and the relative changes in the parameters affected within the BIST circuits due to radiation are used to calibrate the PoL functional circuits. The adaptive

calibration of circuits is a three-step process: the first being the prediction of radiation effects at design time, the second is in-field monitoring of circuit/system parameters without affecting the circuit/system's normal operation, and lastly, the tuning of the functional circuit/system device parameters to recover circuit performance. This work analyzes the performance parameter shifts for three critical circuits of a typical power management system: a ring oscillator, a bandgap voltage reference circuit, and a non-overlapping clock (dead-time) generator. This paper also proposes low overhead monitoring circuits to track performance shifts due to TID.

Section II gives a brief overview of the TID induced MOSFET device parameter shifts in CMOS technology. These shifts are modeled in this work to study performance shifts in critical power management circuits. Section III gives detailed analysis of the performance shifts in a ring oscillator, band-gap reference, and dead-time generator due to TID. Bias tuning options are proposed in each circuit for recovering circuit performance. Additionally, two low-overhead BIST circuits are proposed in Section IV for in-field performance monitoring, and a complete system for bias tuning is presented in Section V.

II. TID Induced Device Parameter Shifts in CMOS Technology

Ionizing radiation on a MOSFET deposits energy creating electron-hole pairs, which leads to non-recombined trapped charges in the oxide and at the interface of the oxide and silicon [2] and causes parametric effects on the MOSFET like threshold voltage (V_{TH}) shift. The V_{TH} shift due to traps is negative when the charge is positive, as seen in Fig. 1. Interface traps in NMOS are negatively charged, leading to a positive shift in V_{TH} (designated Vit in Fig. 1), and interface traps in PMOS are positively charged, leading to a negative V_{TH} shift. PMOS V_{TH} shift is higher than NMOS V_{TH} shift over time [10], and the V_{TH} shifts are bias dependent.

Interface build-up is a slower phenomenon compared to oxide trapping, which means that a change in Vot (shift due to oxide trapping) is observed earlier than a change in Vit. This explains why n-channel threshold voltage first decreases as a function of tunneling and annealing time and later begins to increase as interface traps increase. This is called the 'rebound' effect. These shifts are commonly observed in today's larger than 110 nm node CMOS bulk technologies. Due to the power requirements of most power management integrated circuits, thicker oxide technologies like 180 nm, 350 nm and 0.5 μm are still being used. Hence, TID still poses an issue in current CMOS technologies used for power electronics in space missions.

PMOS and NMOS V_{TH} shifts due to TID have been modeled in prior works [2], [10] using simple gate voltage offsets in PMOS and NMOS devices, where the offset voltage trends are determined by the TID levels. For 0.18 μm CMOS bulk technology, TID induced gate offsets have been observed (measured) with gate voltage offsets up to 400mV in PMOS devices and 8mV in NMOS devices. This process technology is chosen for design because it is a popular technology node for implementing integrated power management solutions for space applications. This work uses the voltage offset models derived in [10] to analyze the performance via simulation of three critical power management circuits with total dose up to 1 Mrad (SiO_2).

III. Analysis and Bias Tuning of Performance Parameters in PM Circuits under TID

Three of the most critical circuits used in a PoL controller are a ring oscillator, a bandgap voltage reference, and a non-overlapping clock generator. This section analyzes the performance parameters of these three circuits under TID and proposes methods to recover performance under TID through bias tuning.

A. Ring Oscillator

A ring oscillator is generally used in a PoL system to set the switching frequency of the power converter. In some cases, it is also used to generate a clock for digital controllers in a switching power converter. A typical ring oscillator is shown in Fig. 2, whose frequency is set by the propagation delays of the inverters caused by the charging and discharging times of the equivalent capacitance at each node. This ring oscillator frequency can change due to TID induced threshold voltage shifts in the MOSFETs, which is an undesired phenomenon. Fig. 3(a) plots the shift in frequency with increasing TID for a 17-stage ring oscillator designed for a 20 MHz pre-radiation oscillation frequency in a 0.18 μm BCD-CMOS process technology with a 5.0 V supply voltage. The MOSFETs are modeled over TID using the gate offset models derived in [10] for this specific CMOS process.

In order to allow for flexibility in the oscillator's frequency, a 17-stage current starved ring oscillator topology shown in Fig. 4 is also implemented in the same process technology [11]. The current starved ring oscillator allows for bias tuning through $V_{control}$, which can be used to minimize undesired frequency shifts in the ring oscillator due to TID. $V_{control}$ changes the current bias (I_{bias}) values, where I_{bias} is set by the PMOS rail devices and determines the oscillation frequency. The simulated relative frequency shift for the current starved ring oscillator over TID is shown in Fig. 3(b) when the bias is kept constant over TID. The shift is plotted as the percentage frequency deviation from the pre-radiation oscillation frequency. As seen in Fig. 3(b), the frequency shifts by 3% at higher TID levels. When the control voltage ($V_{control}$) is ideally dynamically adjusted to tune the oscillator frequency with varying TID, the oscillator frequency can be maintained constant at the pre-radiation value. The required ideal voltage for $V_{control}$ required to maintain a constant (pre-radiation) oscillator output frequency with TID is also given in Fig. 3(b).

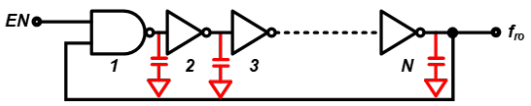
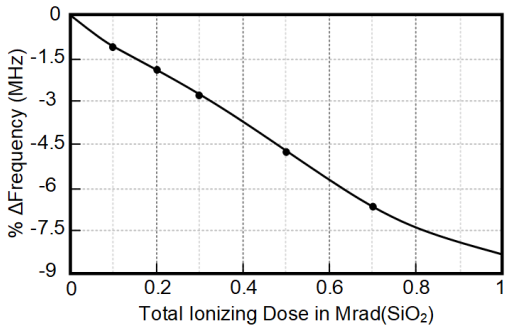
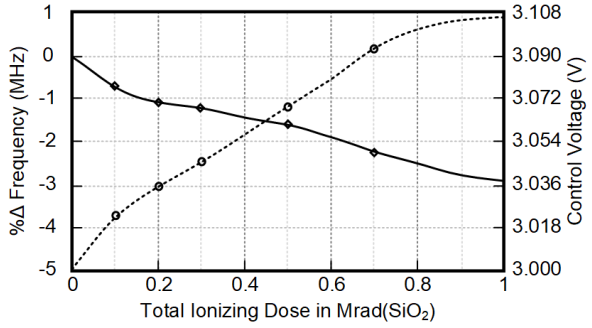


Fig. 2. A basic ring oscillator, where N=17 for the presented design



(a)



(b)

Fig. 3. (a) Percentage frequency shift in a 17-stage traditional ring oscillator versus TID, and (b) Percentage frequency shift in a 17-stage current starved ring oscillator with a fixed control voltage (solid line) and the control voltage value of $V_{control}$ required to tune the output frequency to the pre-radiation value (dotted line) versus TID

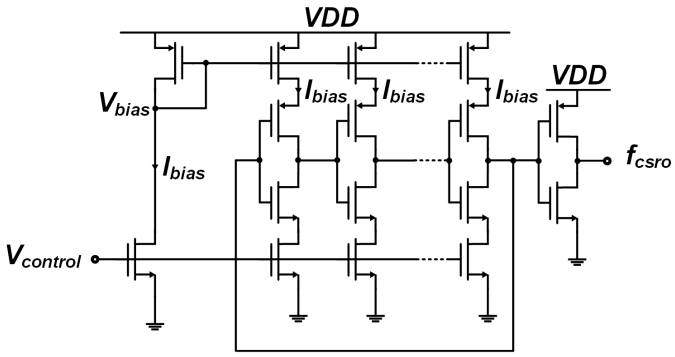


Fig. 4. Current starved ring oscillator with with bias tuning through $V_{control}$

The $V_{control}$ values are well within an acceptable range and resolution to support a simple DAC realization for system-level autonomous dynamic adjustment. Therefore, the $V_{control}$ bias tuning knob can be autonomously varied by employing in-field monitoring at the system level. Due to the reduced supply headroom, the frequency range for a 17-stage current starved ring oscillator is an order magnitude less than that of a 17-stage traditional ring oscillator and for this reason, the percentage change in oscillation frequency has been reported for both cases in order to clearly compare them. The NMOS rebound effect previously discussed in Section II can be seen at approximately 200 kRad (SiO_2) with the slight flattening of the curve, but this effect is not large since the NMOS

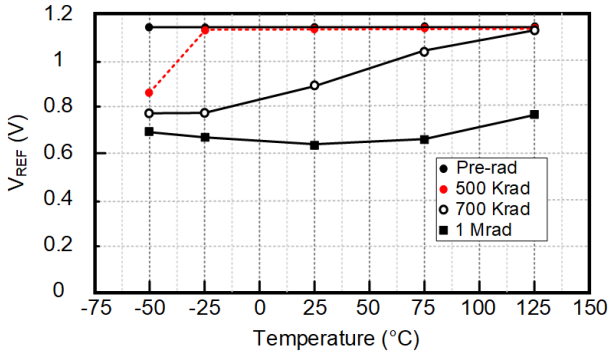


Fig. 5. Bandgap output reference voltage versus temperature at different TID levels

shifts are small compared to the PMOS V_{TH} shifts for device widths 10μm and larger [10]. The tuning of the current starved ring oscillator does not cause significant increase in power consumption, as the additional current for each inverter is only 3μA in the worst case.

B. Bandgap Voltage Reference Circuit

Bandgap voltage references (BGRs) provide an output reference voltage that is largely independent of process, voltage supply, and temperature (PVT) variations. For space electronics, the BGR should also provide a constant reference voltage under TID. If the reference voltage from the BGR shifts, this may compromise the performance of subsequent circuit blocks like error amplifiers in controller feedback loops, current biasing circuits, etc.

The expression in (1) describes the output reference voltage for the traditional bandgap that corresponds to Fig. 6, where V_{EB2} is the emitter-base voltage of Q_2, V_T is the thermal voltage of the pn junction, A_1 is the area of PNP Q_1, and A_2 is the area of PNP Q_2. This equation assumes that the currents I_1 and I_2 through the PNP devices are equal.

$$V_{REF} = V_{EB2} + \frac{R_2}{R_1} * V_T * ln(\frac{A_1}{A_2}) \quad (1)$$

In reality, the precision of the output voltage of the BGR is highly dependent on the accuracy of the current mirrors used in the bandgap core (seen as I_1 and I_2 in Fig. 6). TID can affect mismatch between I_1 and I_2, which affects the BGR's output voltage precision [12], [13]. The threshold voltage shift due to TID may affect the threshold voltage of each MOSFET in the circuit differently. For the presented analysis, the threshold is modeled for the BGR as a uniform effect on all of the PMOSFETs or NMOSFETs. Under TID, the PMOS V_{TH} (threshold voltage) will shift, resulting in the variation of I_1 and I_2, which causes an offset in the bandgap output voltage. The expression in (2) describes the output reference voltage for the bandgap that corresponds to Fig. 6 as a function of current and V_{EB2}, where M_1 and M_2 threshold voltages are assumed to shift simultaneously (and have the same (W/L) and therefore the same nominal currents), such that I_1 and I_2 are equal before and during irradiation. This means I_1 can replace I_2 in (2). If I_2 decreases, the V_{REF} will also decrease. As the

V_{TH} of the PMOS devices increase, they will lose current and the V_{REF} will subsequently decrease. The relationship between V_{TH} and I_2 is given in (4) as the standard saturation current equation.

$$V_{REF} = I_2 * R_2 + V_{EB2} \tag{2}$$

V_{EB2} is expressed as a function of I_B (base current of the PNP) in (3), where G_E is the emitter Gummel number, A_E is the area of the emitter, n_i is the electron concentration and the hole concentration in undoped semiconductor material, and q is the electronic charge.

$$V_{EB2} = V_T * ln(\frac{I_B}{A_E} * \frac{G_E}{q * n_i^2} + 1) \tag{3}$$

$$I_{1,2} = \frac{\mu_P * C_{OX}}{2} * \frac{W}{L} * (V_{GS} - V_{TH})^2 \tag{4}$$

Fig. 5 plots the simulated V_{REF} versus temperature under varying TID radiation doses. The BGR is simulated in a 180 nm technology that offers vertical PNPs, and the BGR is designed with 20 μm^2 area PNPs. The operational amplifier is a simple 5-transistor OTA architecture. The simulated BGR under TID only includes the threshold shifts in the MOSFETs that are modeled using data from [10]. It is important to note that there are other device parameters that shift over TID and significantly affect BGR performance, namely the PNP diodes and their effective emitter area and the input offset voltage of the operational amplifier. A big design uncertainty are the PNP bipolar devices, which are used for their pn junctions that act as diodes and create a CTAT (Complementary To Absolute Temperature) voltage. The effects of radiation on diodes can shift the output voltage of a bandgap output voltage by a few hundred millivolts [14]. Furthermore, the voltages at the amplifier's inputs should be equal to provide a more precise output voltage. Across TID, the input pair of the amplifier will have V_{TH} shift, which can be mitigated by using offset cancellation circuitry such as chopper stabilization techniques. This is a radiation hardening by circuit design technique to improve the output voltage precision. Although this work focuses on analyzing MOSFET threshold voltage shifts under TID, the concept of using bias tune to recover performance can also accommodate performance shifts due to these other device parameter shifts over TID.

Fig. 6 shows the simplified schematic of the BGR with added PMOS current source (trim) devices in red that may be switched in/out and used to dynamically tune the bias current of the bandgap under TID in order to mitigate BGR output voltage shift. The pre-radiation nominal currents can be independently reduced or increased in the bandgap core through this current tuning, thus counteracting much of the V_{TH} shift due to TID. Simply increasing the width of the nominal PMOS current sources would not provide hardening against TID since the threshold shift occurs dynamically and oftentimes differently amongst the MOSFETs. Thus, increasing the BGR's PMOS current source device widths would yield

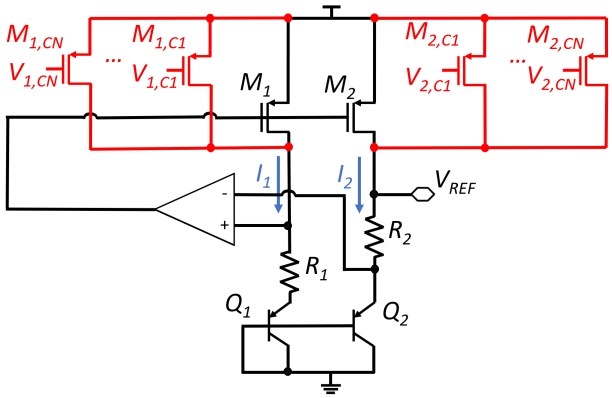


Fig. 6. Simplified schematic of the bandgap voltage reference core

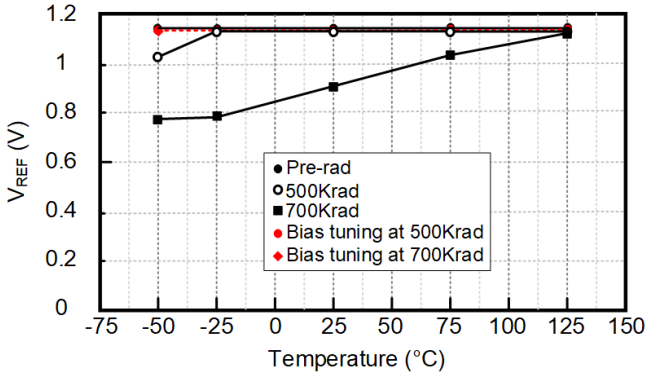


Fig. 7. Simulated V_{REF} versus temperature for 500 kRad and 700 kRad TID with and without bias tune

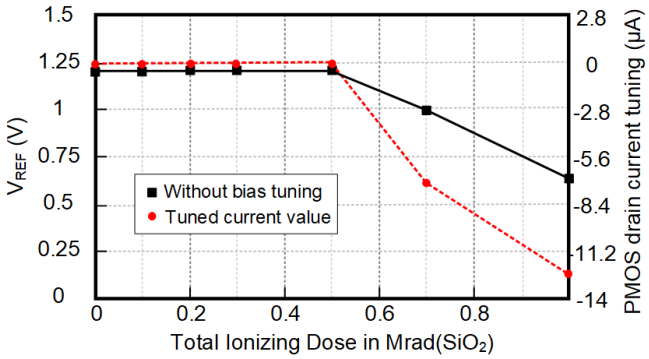


Fig. 8. Simulated Bandgap reference output voltage at 27 °C without tuning (black-solid) and drain current ($I_{1,2}$) of each BGR core branch after tuning (red-dashed) versus TID

the same result as an optimized BGR design with a non-width-increased current source, and bias tuning could again be used for hardening.

Fig. 7 plots V_{REF} versus temperature pre-radiation and under TID doses of 500 kRad (SiO_2) and 700 kRad (SiO_2). From Fig. 7, it is observed that ideally tuning the bias current by increasing the effective PMOS widths (M_1 and M_2) reduces the deviation of V_{REF} over temperature from the pre-radiation performance. This simulation shows that the 500 kRad (SiO_2) dose recovers well at -25 °C, while the 700 kRad (SiO_2) dose shows recovery throughout the temperature range of -25 °C to +125 °C.

Fig. 8 plots V_{REF} versus TID before bias tuning at a fixed

BGR temperature of 27 °C. V_{REF} varies from 1.207 V to 0.643 V over TID without bias tuning. When tuning the bias by varying the PMOS device widths (with ideally infinite width resolution) at each TID level, V_{REF} can be maintained at 1.207 V over TID. Fig. 8 also plots the PMOS drain (bias) current shift with respect to TID that is required to provide the V_{REF} performance with bias tuning. At 1 MRad (SiO_2), the current varies by 12.84 μA from its pre-radiation value, which is well within the range and resolution of the simple current bias trim illustrated in Fig. 6.

C. Non-overlapping Clock Generator

A non-overlapping clock is used to avoid shoot-through in the power stage of a switching power converter. This non-overlap period can vary due to parametric shifts from TID and must be recovered by employing tuning methods. A typical digital non-overlapping clock (also called a dead-time generator) is made up of digital NAND and NOT gates as shown in Fig. 9(a). The generated non-overlapping clock signals are ϕ_1 and ϕ_2. A simulation of the implemented non-overlapping clock generator in the 0.18 μm BCD process shows that the dead-time varies by 15% over the entire TID range for the untuned case in Fig. 9(a). This dead-time variation over TID is plotted in Fig. 10.

Several methods, such as that proposed in [15], and capacitor network tuning as illustrated in Fig. 9(b) have been explored in the past to tune the non-overlap period. Due to the on-chip area constraints from the capacitor network, the capacitor network tuning method poses limitations on the maximum tuning capability. In this work, the lowest overhead method of bias tuning is used to tune the non-overlapping clock. The bias tune for tuning the non-overlap employs the same technique for each inverter as the current starved ring oscillator discussed previously in Section III-A. The bias current is perfectly (ideally) tuned to maintain a constant pre-radiation dead-time (1.34 ns) over TID. The ideal control voltage ($V_{control}$) required to tune the bias current, and hence dead-time, to the pre-radiation value at each TID level is also plotted in Fig. 10. This control voltage varies significantly more than the tune for the ring oscillator because a 3-stage oscillator is used here. This control voltage range can be easily realized at a system level.

IV. BIST Circuitry for Low Overhead In-field Performance Monitoring under TID

A. Ring Oscillator with an Output Charge Pump

In Section III, the performance shifts in a ring oscillator due to V_{TH} shifts over TID is analyzed, and a bias tuning method to recover the pre-radiation frequency is proposed. In this section, a similar ring oscillator *without tuning* is used to monitor frequency shifts due to TID. This is a low overhead monitoring circuit that can be easily integrated within the system.

A ring oscillator is oftentimes used to characterize the performance of a new technology and also used during wafer testing to observe manufacturing process variations (process control monitor). The ring oscillator provides a straightforward method to measure supply and temperature changes

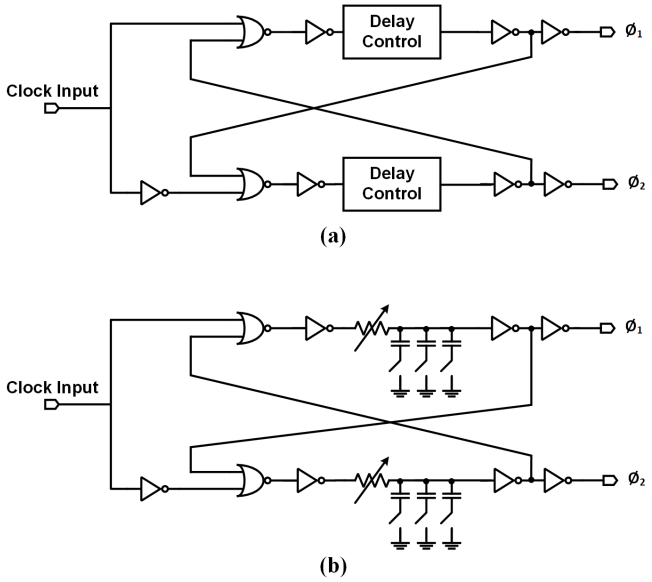


Fig. 9. Non-Overlapping clock generator with (a) delay control using basic bias tuning, and (b) digital implementation for tuning

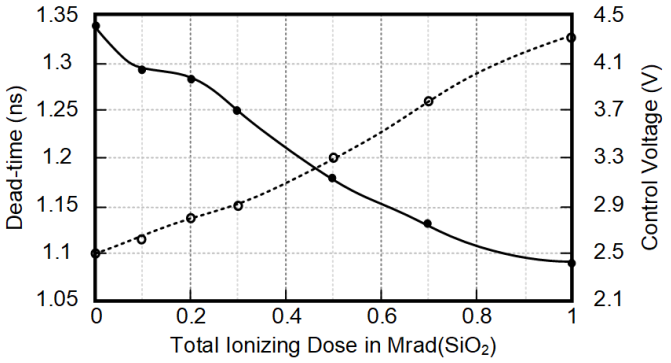


Fig. 10. Dead-time performance shift in a non-overlapping clock generator over TID (solid), and control voltage for tuning dead-time to the pre-radiation value over TID (dotted)

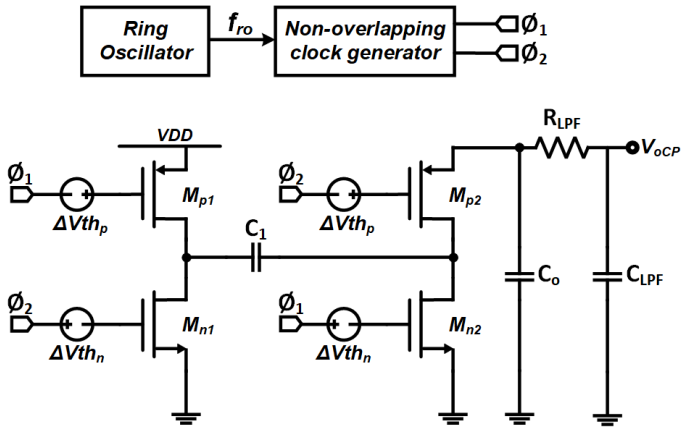


Fig. 11. Charge Pump used to convert dead-time to voltage for built-in performance monitoring over TID

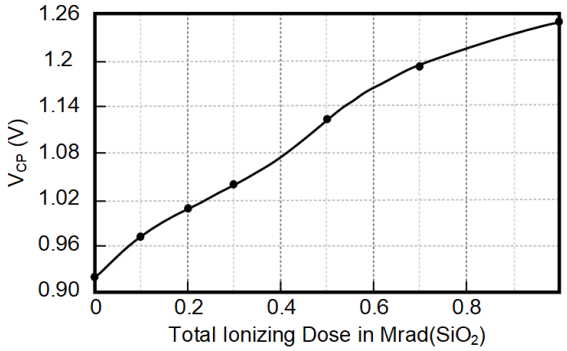


Fig. 12. Charge Pump DC output voltage versus TID

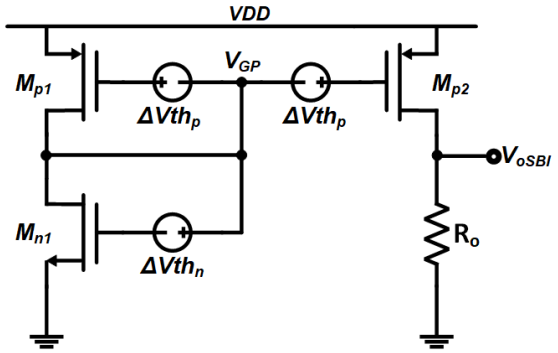


Fig. 13. Self-biased inverter BIST circuitry with modeled PMOS and NMOS V_{TH} shifts

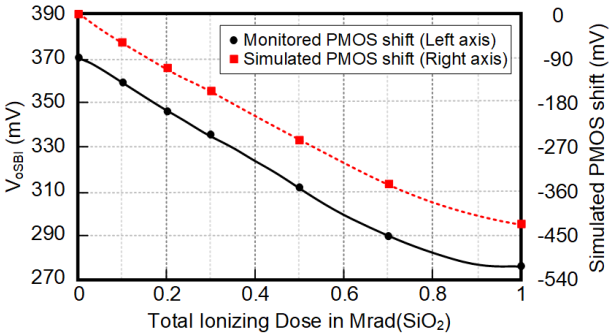


Fig. 14. Output voltage of the self-biased inverter that tracks V_{TH} shifts

on-chip. Oftentimes, it is costly to probe a high frequency signal (due to amplitude or bandwidth constraints) on chip. Thus, the oscillator's output signal is converted to a DC voltage on-chip. The DC voltage is then monitored off-chip. In this work, a charge pump is used to convert the oscillation frequency, which is typically in the higher MHz range for power management circuits, to a DC voltage that can be monitored off-chip. The simulation test bench for the proposed ring oscillator-based BIST circuit is shown in Fig. 11, where the ring oscillator is used to supply the input to the non-overlapping clock generator, which creates two non-overlapping clock signals $\phi 1$ and $\phi 2$. These signals are derived from the previously discussed non-overlapping clock generator circuit (also implemented on-chip). These clock signals are used as inputs to a charge pump that converts the frequency of the clock to a finite voltage V_{oCP}. A low pass filter is used to obtain a stable DC voltage that correlates to the ring oscillator's frequency. The TID-induced V_{TH} shifts in the NMOS and PMOS devices are modeled in simulation as a negative gate bias to observe a change in the frequency of the ring oscillator, as modeled by $\Delta\ Vth_p$ and $\Delta\ Vth_n$ in Fig. 11. All of the NMOS and PMOS devices are shifted simultaneously with TID. These V_{TH} shifts are modeled in all of the circuits, including the ring oscillator, non-overlapping clock generator and the charge pump, as the BIST circuitry's device parameters also shift with TID. The charge pump's output DC voltage curve correlating to parametric shifts in the frequency of the ring oscillator is plotted for varying TID level in Fig. 12.

This radiation monitoring circuitry can be used to control and tune critical functional PM circuits such as the current starved ring oscillator described in Section III-A.

B. Self-Biased Inverter

The self-biased inverter in Fig. 13 is made up of an inverter whose input is connected to the output. This configuration generates a gate voltage V_{GP} that is used to bias the PMOS M_{p2}. The drain current of M_{p2} is converted to a voltage V_{oSBI} with the help of resistor R_o. According to [6], if the width of the PMOS device is much greater than the width of the NMOS device in a self-biased inverter, then the gate voltage tracks V_{TH} shifts from PMOS devices only. Hence, the drain current derived from M_{p2} is a function of PMOS V_{TH} shifts alone. This is another low overhead method that can be easily integrated to monitor TID induced V_{TH} shifts in an integrated circuit.

TID induced threshold voltage shifts are modeled and added to all PMOS and NMOS devices of the self-biased inverter circuit, as shown in Fig. 13. The self-biased inverter's output voltage V_{oSBI} is plotted for various TID levels up to 1 Mrad (SiO_2) in Fig. 14. The PMOS V_{TH} shift is clearly tracked as shown by the graph, where the simulated PMOS shift is the actual PMOS V_{TH} shift modeled in the MOSFETs for each TID level. This self-biased inverter can be used in combination with other monitoring circuits to extract various parametric shifts.

The outputs of the ring oscillator with a charge pump and the self-biased inverter have different profiles over TID, thus allowing the designer flexibility to choose among the two radiation monitoring circuit implementations to match the bias tuning needs of the functional power management circuits.

V. Complete System for Bias Tuning

To correlate the radiation induced performance shifts in monitoring circuits to the bias tuning that is required to tune the circuits to pre-radiation performance, a look up table is generated using CAD based simulations at design time from Section III. The output of the radiation monitoring circuit is then scaled to match the bias tuning control value from the look up table. The complete system is shown in Fig. 15. A single radiation monitoring circuit can be used to control multiple functional circuits in order to reduce area and power

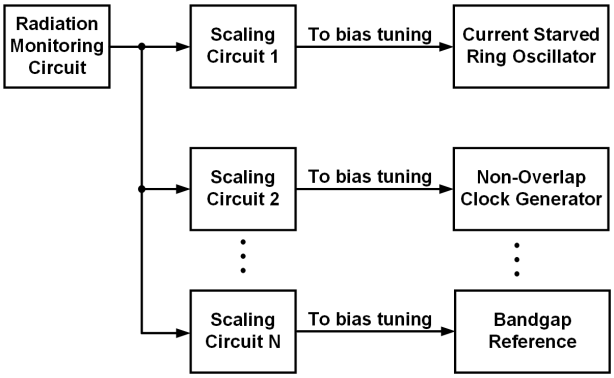


Fig. 15. A complete system for bias tuning using radiation monitoring circuits

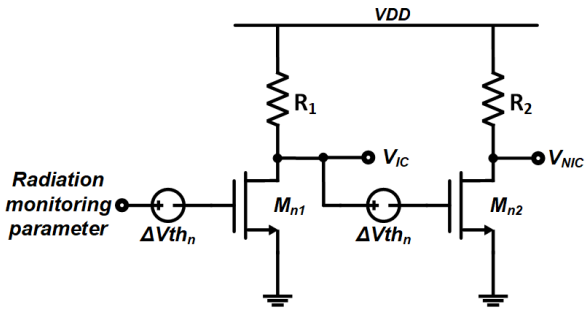


Fig. 16. An example of scaling circuit using minimum devices

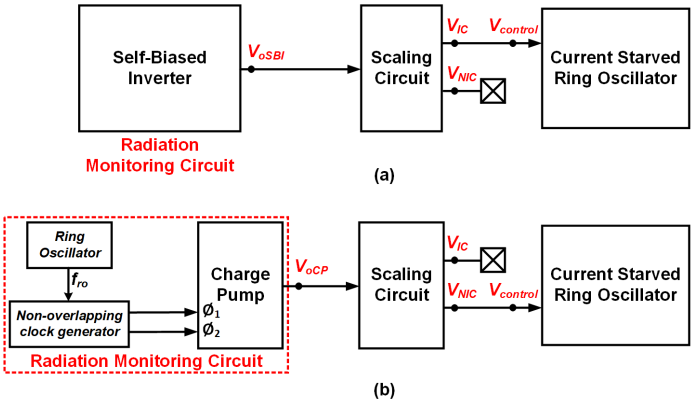


Fig. 17. Automatic bias-tuning system for TID induced parametric shifts with radiation monitoring circuit based on (a) self-biased inverter and (b) Ring oscillator with a charge pump

overhead. A separate scaling (interface) circuit is required for every PMIC circuit to match the bias tuning trend for that specific circuit design.

The scaling circuit can been realized by level shifting and tuning the slope of the radiation monitoring circuit's output. One such scaling circuit is illustrated in Fig. 16. The output V_{NIC} gives a level shifted voltage trend similar to Fig. 14 while the output V_{IC} gives an inverse voltage trend of the same plot. The performance of the scaling blocks is also affected by radiation induced threshold voltage shifts and these shifts have been taken into consideration for the simulations.

Two methods of automatically bias tuning the current starved ring oscillator have been implemented. In the first method shown in Fig. 17(a), the self-biased inverter is em-

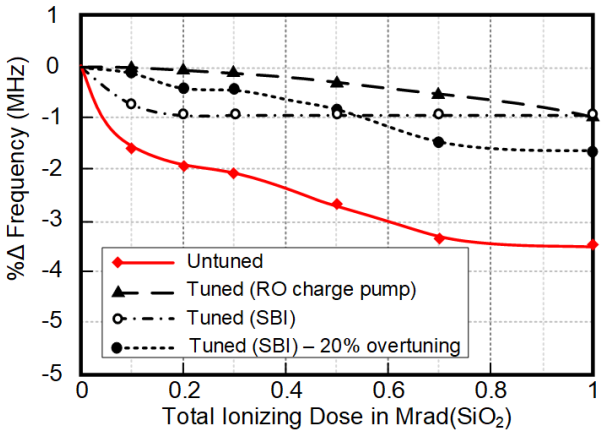


Fig. 18. Plot of un-tuned and bias-tuned ring oscillator frequency shift using the look up table method

ployed as the radiation monitoring circuit, the output of which is fed to the scaling circuit. The inverted output of the scaling circuit is used to tune the functional current starved ring oscillator. In the second method shown in Fig. 17(b), the ring oscillator based charge pump is used as the radiation monitoring circuit. The plots for the automatically tuned current starved ring oscillator frequency has been shown in Fig. 18 for both methods. The red solid curve shows the ring oscillator frequency without any bias tuning and the dotted curves show the output of the ring oscillators that take advantage of the autonomous bias tuning methods from Fig. 17(a) and Fig. 17(b). The plot also includes the tuned ring oscillator frequency using the Fig. 17(b) method, with 20% inaccuracy in the tuning value in order to demonstrate the robustness of the tuning method. Even with 20% inaccuracy in the tuning voltage, the shift in frequency is less than 1.8% of the pre-radiation value. Although 100% radiation hardening is not possible from this look-up table based method due to the small error margin from the non-linearity of the scaling and process variations, the presented methods of bias tuning are an essential step towards system radiation hardening by monitoring radiation induced parametric shifts in space technologies.

Conclusion

This paper analyzes the effects of MOSFET threshold voltage shifts due to TID on circuit performance parameters for critical analog PoL circuits. Three circuits are analyzed, and bias tuning is used in these three circuits to recover circuit performance over TID. Additionally, two radiation effects monitoring circuits are showcased that may be used to track TID-induced performance shifts in integrated power management circuits. Finally, two complete systems are demonstrated based on a look up table approach that automatically tunes a functional current starved oscillator to maintain performance over TID. One system uses the presented charge pump radiation monitoring circuit and the other system includes the self-biased inverter.

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