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FPGA-based burst-error performance analysis and optimization of regular and irregular SD-LDPC codes for 50G-PON and beyond

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Abstract: We evaluate the burst-error performance of the regular low-density parity-check (LDPC) code and the irregular LDPC code that has been considered for ITU-T's 50G-PON standard via experimental measurements in FPGA. By using intra codeword interleaving and parity-check matrix rearrangement, we demonstrate that the BER performance can be improved under ~44-ns-duration burst errors for 50-Gb/s upstream signals.

1. Introduction

The IEEE 802.3ca 25G-EPON [1] working group has chosen a high-performance hard-decision (HD) irregular LDPC coding-based forward error correction (FEC) scheme with a bit-error ratio (BER) threshold of about 10^{-2} and a code rate of 0.849 [2–4]. During the standard meeting, the use of soft-decision (SD) was proposed to improve the performance of the irregular LDPC mother code that has been specified by the IEEE working group in order to better support 50G-PON [5–7]. The SD-LDPC performance has been analyzed via real-time measurements with field programmable gate array (FPGA), showing that SD-LDPC outperforms HD-LDPC by over 1 dB in terms of the gross coding gain at an output BER of 10^{-12} [5–7]. More recently, the International Telecommunication Union (ITU) had consented ITU-T 50G-PON [8] standard to support disruptive application and services including the high-definition (HD) video streaming service, virtual/mixed reality, online video meeting, cloud storage and computing. The standard adopted the same LDPC mother code as IEEE 802.3ca with slightly different puncturing and shortening.

LDPC codes are widely used as one of FEC solutions in optical transmission systems to provide the error correction performance close to the channel capacity [9,10]. LDPC coding was introduced by Gallager in the early 60's [11] and employ iterative message-passing (MP) decoding algorithms. Such a decoding algorithm exchange the extrinsic information between coded bit nodes and parity-check nodes in which they participate in an iterative fashion. At each new iteration, new messages are computed in an extrinsic manner, which means that the message received by a coded bit node from a parity-check node does not depend on the message just sent to the other nodes in the previous round. Consequently, the collected belief information keeps propagating within each new decoding iteration, which provides a maximum *a posteriori* probability decoding of the transmitted codeword (when there are no cycles in corresponding bipartite representation of the parity-check matrix). There are various approaches to implement the MP algorithm. In this paper, we will focus on one of these approaches, scaled min-sum algorithm [12]. Irregular LDPC codes are proposed by Luby *et al.* that can approach capacity more closely than regular ones [13] by proper parity-check matrix construction. The density evolution theory is developed by Richardson *et al.* to analyze and synthesize optimal degree distributions in asymptotically large random bipartite graphs under a wide range of channel realizations [14].

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In time-division-multiplexed (TDM) PON, burst-mode (BM) operation is an essential feature for upstream communication. During the transmission, the optical performance at the beginning portion of each upstream signal burst is usually much worse than that of the rest of the burst, which can lead to burst errors during the beginning portion of the stream [15]. The performance degradation at the beginning of each upstream signal burst is typically introduced by several impairment sources, such as the electrical and optical turn-on transients of the transmitter and the receiver. It is important to evaluate the burst-error performance of FEC for upstream transmission in TDM-PON.

In this paper, we analyze the burst errors mode for the 50G-PON standard based on the non-uniformly distributed errors model. Then we implement and test a commercial irregular LDPC code studied in [3–5] and compare it against regular LDPC code performance under the burst mode errors. By using parity-check matrix rearrangement and different intra codeword interleaving, we observed that both regular LDPC code and irregular LDPC code performance would be improved under burst mode errors by using the proper optimization. For both regular LDPC code and irregular LDPC code, the intra codeword interleaving with the accurate knowledge of burst mode errors duration will provide the optimal correction performance. However, it will lead to the extra costs of latency and buffering resources. For the irregular LDPC code, the suboptimal option is to rearrange its parity-check matrix. In this method, we improved the coding performance around 0.3 dB without the extra cost of latency and buffering resources under burst mode errors. This method could provide an interesting approach to be considered for the next generation 100G-PON standard.

We organized the rest of this paper as follows. In Section 2, we describe our system model, including the FPGA architecture and the non-uniformly distributed errors model in the burst mode. In Section 3, we detailed our implemented regular LDPC code and analyzed its performance on different scaled burst mode errors with and without intra codeword interleaving. Sections 4 are devoted to the performance analysis of the implemented commercial standard irregular LDPC code performance under burst error mode by using parity matrix rearrangement and intra codeword interleaving. We conduct both modelling analysis and FPGA verification for different burst errors mode level. Finally, Section 5 summarizes and concludes the paper.

2. FPGA architecture and burst errors models

For the on-off keying (OOK) transmission over thermal or amplified spontaneous emission (ASE) noise dominated channel, which could be considered as an additive white Gaussian noise (AWGN) channel, let the log likelihood ratio (LLR) information of the i-th received symbol y_i be represented by δ_i and it is defined by:

$$\delta_i = \log\left(\frac{Pr(x_i = 0 \mid y_i)}{Pr(x_i = 1 \mid y_i)}\right), \tag{1}$$

where the prior probabilities of the transmitted bit of 0 and 1 are equal, x_i represents the i-th transmitted bit, and $Pr(x_i = 0 \mid y_i)$ represents the posterior probability of the i-th transmitted symbol x_i given the received symbol y_i. For LDPC decoder under the binary input AWGN channel, let σ^2 represents the noise variance. $\beta_v^{k,l}$ and $\alpha_c^{k,l}$ represent extrinsic information (message) at the variable v and the check c at k-th iteration and l-th layer message, $\beta_{cv}^{k,l}$ and $\alpha_{vc}^{k,l}$ represent the check c to variable v extrinsic information (message) and the variable v to check c at k-th iteration and l-th layer message; where $l = 1,\ldots,L$ and $k = 1,\ldots, I_{max}$. The parameters I_{max} and L denote the maximum iteration index and layer index, respectively. The FPGA emulation processors can be summarized through Eqs. (2),(5):

$$\delta_i = \frac{2}{\sigma^2} y_i \tag{2}$$

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$$\alpha_v^{k,l} = \delta_i + \sum_{l'} \beta_{cv}^{k,l'} \tag{3}$$

$$\alpha_{vc}^{k,l} = \delta_i + \sum_{l' \neq l} \beta_{cv}^{k,l'} \tag{4}$$

$$\beta_v^{k,l} = s \times \prod_{v' \neq v} \mathrm{sign}(\alpha_{v'c}^{k,l}) \min_{v' \neq v} |\alpha_{v'c}^{k,l}| \tag{5}$$

where s represents the scaling factor for the scaled min-sum algorithm [12]. Equation (1) is employed to calculate the bit LLR in OOK AWGN channel and Eqs. (2)-(5) are used in the layered decoding algorithm.

As illustrated in Fig. 1(a), we design and implement an FPGA based real-time LDPC emulator, and corresponding utilization of FPGA resources is provided in Fig. 1(b). The platform consists of following parts: a software configuration interface, an LDPC encoder; a modulation symbol mapper, a Gaussian noise generator, a burst error emulator, an LLR calculator, a rate-adaptive LLR processor based on layered scaled min-sum algorithm [9]; and an error counter circuit. The LDPC encoder produces a sequence of binary encoded codeword, which consists of information bits and parity-check bits. A read only memories (ROMs) based modulation mapper is responsible to generate signed symbols based on input binary codeword sequence and sent to a burst errors' emulator. The first 1/8 portion of each codeword were attenuated before transmitting over an AWGN channel to emulate the burst errors. A PC controls the attenuation factor through the software configuration interface. Based on the Box-Muller algorithm, the Gaussian noise generator generates samples of the white Gaussian noise by using two linear-feedback shift register (LFSR) based uniform generators. The generated sequence of samples is multiplied with standard deviation of noise σ to emulate the output signals from AWGN channel. The signal and the noise are both 32 bits with 25 bits fractional parts. Based on Eq. (1), the emulated output signals are sent to the LLR calculator to calculate the bit LLR. Then the quantized bit LLR is obtained based on Eq. (2) and fed to the LDPC decoder based on Eqs. (3)–(5). In LLR min-sum processor, we optimize the power and latency cost by compressing the input $\alpha_{v'c}^{k,l}$ into a smaller size after deleting the unnecessary nodes. In order to check whole variable nodes BER values within one layer, we delayed and inserted corresponding unnecessary nodes value to the output of the min module $\beta_{cv}^{k,l'}$ into the full size. The location of the unnecessary $\alpha_{v'c}^{k,l}$ and non-updated $\beta_{cv}^{k,l'}$ are controlled by a finite state machine. In the architecture, the noise variance, the number of iterations, the burst error attenuation factor, and the length of shortening are controlled by the Virtual I/O based software controlled interface. The software control interface also reports the number of errors and the number of codewords to calculate the BER. A full codeword monitoring result are depicted at the Fig. 2(b). The row of output signal is the binary signal under AWGN channel emulated at FPGA. The row of signal power is the binary signal transmitted before the AWGN channel. The first 1/8 portion of the codeword shows lower amplitude both in the row of output signal and the row of signal power.

In PON, each upstream burst usually experiences more burst errors at the beginning of the burst. Typically, it is desirable to limit the time duration of the burst-error region to <100 ns. In the burst-error region, the input BER to the FEC decoder at the upstream receiver may be much higher than the average input BER. In the burst mode upstream TDM PON, the burst transmission consists of a preamble used for synchronization and the data encoded with LDPC. By using different size of the preamble, the impact of the burst errors from the channel will also vary. Based on our previous study [10], the length of the preamble is normally short (~128bits) compared to the length of the burst duration (more than 2000 bits). Adding few bits to the preamble will significantly improve the performance of the signal synchronization, therefore, in this article, we will focus on the solution of the fixed length of the preamble solution for the burst errors case without considering of the impact of the burst noise on the signal frame synchronization. To

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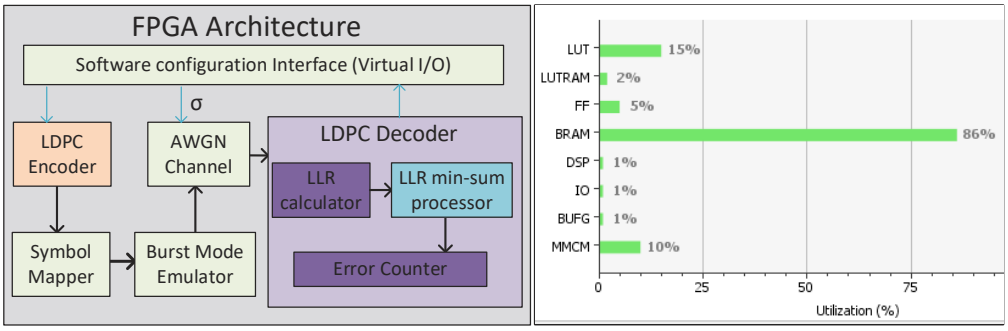

Fig. 1. FPGA architecture used for SD-LDPC coding studies.

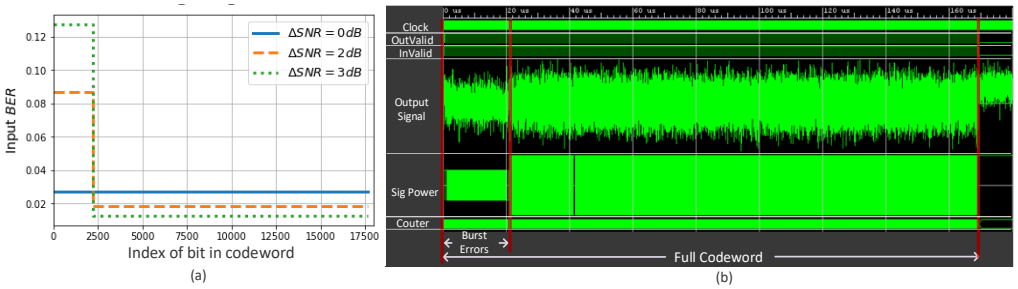

Fig. 2. (a) Different burst-error scenarios; (b) Simulated signal waveform showing a burst-mode errors with non-uniform signal levels.

emulate the non-uniform burst error behavior, the burst errors module intentionally introduces more errors in the first 1/8 portion of each LDPC codeword, which corresponds to about 44 ns for a 50-Gbps upstream signal, or 88 ns for a 25-Gbps upstream signal. To emulate different degrees of bit error non-uniformity, we introduce different signal-to-noise (SNR) degradations for the burst-error region w.r.t. the steady-power region. To generate the SNR degradation in the burst-error region, we reduce the power level. More specifically, we attenuate the power of the first 1/8 of each codeword frame by various amounts such as 0 dB, 2 dB, and 3 dB, respectively corresponding to the reduced power levels of 1.0, 0.63, and 0.5, which are normalized to the steady-state power level. The reduced power level of 1.0 indicates burst mode without errors. An illustrative example of the input BER distribution with the same average input BER and different attenuation values is provided in Fig. 2(a). These three cases of attenuation 0 dB, 2 dB, and 3 dB are labeled with ΔSNR = 0 dB, ΔSNR = 2 dB, and ΔSNR = 3 dB respectively. The first 1/8 bits of the 2dB- and 3dB-attenuation cases lead to the input BERs of 0.0868 and 0.1273, respectively. The following 7/8 bits of the 2dB- and 3dB-attenuation cases yield to the input BERs of 0.0185 and 0.0127. Considering the whole codeword, they all provide the overall input BER of 0.027 in average. At the decoder, we use the same variance to calculate the *LLR* since it is more practical in the real system. A more accurate variance, especially when used for calculate the *LLR* for the burst error region, will definitely improve the decoding performance; however, it will increase the variance estimation complexity and thus energy cost of the real-time system will increase as well. Clearly, the scenario in which the first 1/8 bits of a codeword get attenuated is expected to exhibit higher input BER at first 1/8 of codeword bits. However, in the non-uniform attenuation scenario the situation gets changed as follows. To achieve the same average input BER, the steady-state 7/8 codeword bits must have lower input BER so that overall average BER is the same as for the uniform case. Viewed from the decoder point of view, the first 1/8 of variable nodes will

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provide less belief information while the following 7/8 variable nodes will provide higher belief information. Emulated by Xilinx Vivado, the time-domain waveform of a representative output signals from AWGN channel is shown in Fig. 2(b). The *inValid* and *outValid signals* enable the input port and output port, respectively. *SigPower* describes the input signals affected by the burst errors. *Output Signal* waveform illustrates the attenuated output signal in the presence of AWGN.

When the noise is uniformly distributed in the transmission channel, the variable nodes with higher column weight in a well-designed irregular LDPC codes will collect more belief information in one iteration since the corresponding variable nodes are connected to more check nodes. Therefore, the irregular LDPC codes will provide higher coding gain since the irregular LDPC codes would converge faster than regular LDPC codes. However, in the burst mode, the errors are distributed non-uniformly. The non-uniformly distributed errors lead to the different convergence speed in the regular LDPC codes. There naturally arises the question, whether the performance of the regular LDPC codes will be still better in this case? Can the performance of the irregular LDPC codes be optimized based on the error distribution? Based on our FPGA system, we will answer the first question in the Section 3 and the second one in the Section 4.

3. Regular LDPC performance under burst mode errors

Based on the FPGA system in Fig. 1(a), we implemented a regular LDPC code constructed based on the same method but different from [16,17] with the codeword length of 16935, information bits length of 13550, code rate of 0.8, column weight of 3, row weight of 15, and the girth of 8. The burst errors are concentrated at the first 1/8 of each codeword (due to a SNR degradation of up to 3 dB), corresponding to ~44 ns (~88 ns) for a 50-Gbps (25-Gbps) upstream signals. The employed decoder has three layers and employs 24 iterations. The purpose is to study the suitability of the regular LDPC code for the burst-mode upstream reception operation in the 50G-PON. We use the Xilinx Kintex UltraScale FGPA KCU105 with 530 logic cells and 1920 DSP slices, 21.1 Mb block RAM as the hardware platform for the implementation. To evaluate the regular LDPC performance, we also employ the AD9680 with the sampling wide bandwidth analogy signals of up to 2 GHz to sample the analog signal and perform the quantization, and the AD9144 with more than 1 GHz bandwidth to perform the digital-to-analog conversion.

Using the three layered and 24 iterations decoder with 8 bits $\alpha_{v'_c}^{k,l}$ and $\beta_{cv}^{k,l'}$ with 5 integer bits, 2 fraction bits and 1 bit for sign, the performance of the code is depicted at Fig. 3(a) with the label of RE_o ΔSNR = m dB, where m represents the value of SNR difference (and RE stands for regular). We found that although the performance of the regular LDPC code is slightly improved before the output BER of 10^{-5} under the non-uniformly distributed burst mode errors, the performance is much worse and even exhibit an error floor when we set the output BER threshold to 10^{-10}. For high SNR condition, the continuous errors in the first 1/8 variable nodes impact the coding performance heavily. This does not represent a surprise, given that from coding theory we know that in burst mode the interleaving is required. We also test the performance of the regular LDPC code after using intra codeword interleaving of 8 pieces, with corresponding results provided in Fig. 3(b), where the label is denoted by RE_i ΔSNR = m dB. In this case, the codeword $\boldsymbol{x} = [x_0 x_1 x_2 \ldots x_{n-1}]$, where n is the codeword length, will be interleaved as $x_0 x_8 x_{16} \ldots x_1 x_9 x_{17} \ldots x_{8*q+r-1}$, where q is the integer floored quotient of n divided by 8, r is the remainder, $n = 8*q + r$. Instead of only first 1/8 codeword bits suffering heavier noise, only one from every eight bits in a codeword suffer heavier noise. For an LDPC output BER of 10^{-9}, RE_i ΔSNR = 3 dB, RE_i ΔSNR = 2 dB, and RE_i ΔSNR = 0 dB require the input BER to be 3.07×10^{-2} (corresponding to a Q-factor value of 5.44 dB), 3.01×10^{-2} (5.48 dB), and 2.97×10^{-2} (5.51 dB), respectively. We also implemented and tested the case of intra codeword interleaving of two pieces whose results are summarized in Fig. 3(c) with the label of RE_ii ΔSNR = m dB. In the case of interleaving of two pieces, each codeword is sliced into 2 pieces first and interleaved with each other. Only one from every two bits at the 1/4 beginning of each

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codeword suffers heavier noise. The results indicate that the performance of the regular LDPC codes can be improved under non-uniformly distributed burst mode errors, which is a positive answer to the first question. However, based on the results of interleaving of two pieces, the optimal improvement requires the accurate knowledge of the duration of the burst mode errors.

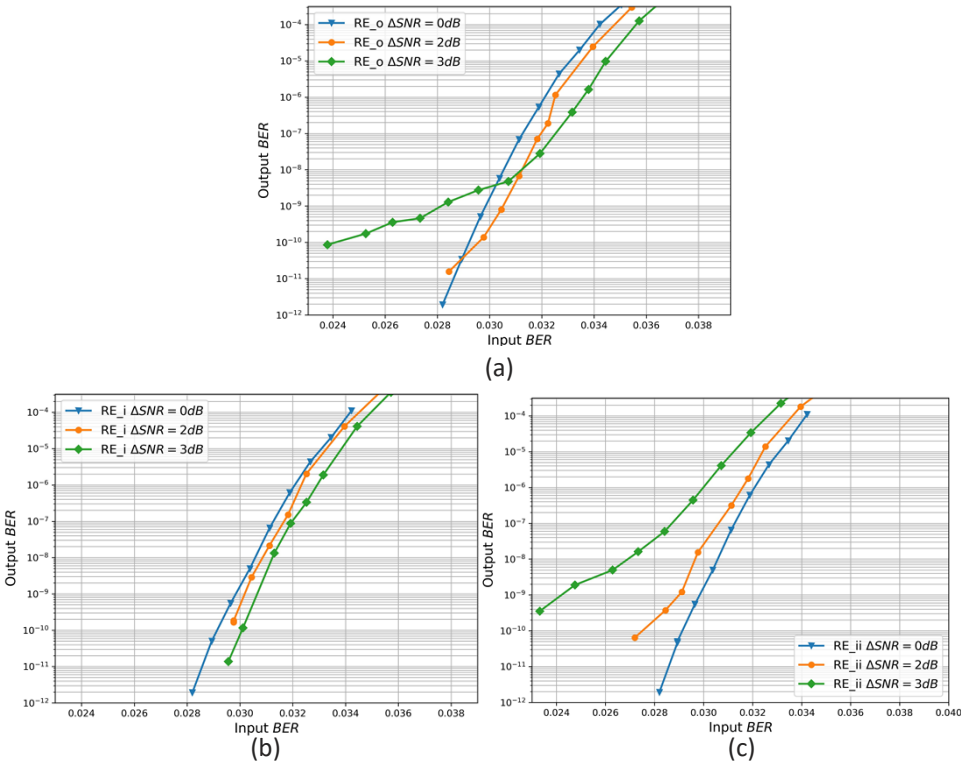

Fig. 3. The regular LDPC codes performance with different degradations: (a) without intra codeword interleaving, (b) with intra codeword interleaving of 8 pieces, and (c) with intra codeword interleaving of 2 pieces.

By analyzing the LDPC code performance as a function of the input of pre-FEC BER, and the output of post-FEC BER, we compared the FGPA performance results from the regular LDPC code with or without different interleaving strategies under the burst error channel. The results indicate that 12.5% (1/8) of the codeword are in the burst mode channel. Smaller LLRs magnitudes on average bring less belief information compared to the rest of codeword in burst mode free sub-channel. The 87.5% bits in codeword in burst error free sub-channel have higher belief information, and these variable reliabilities help decoding process. Besides, based on the performance of the RE_o ΔSNR = 3 dB, the error floor location will increase as suffering the non-uniformly distributed errors. By using the interleaving, which will reallocate the errors distribution in a uniformly method, the error floor will decrease and the coding performance will improve again.

4. Irregular LDPC codes' performance

To study the irregular LDPC code performance in non-uniformly distributed errors, an irregular LDPC code mother matrix studied in [2–6] and then adopted in ITU-T's 50G-PON standard is implemented on the FPGA platform. Figure 4(a) illustrates the mother code parity-check matrix H_a structure of the irregular LDPC used in [4–8], where the colored-box denotes the permutation

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matrix. It consists of 17664 codeword bits, 14592 information bits, and the code rate is 0.846. The H_a matrix consists of three kinds of column blocks with different column weights of 3, 6, 11, and 12. The information bits contain the column of column weight of 3 and 6. The parity check bits contains the column of column weight of 3 and 11 or 12. Since the performance of the irregular codes is impacted by different column weights, we rearrange the H_a such that the columns with the lowest weight (3) appear first in order for the code to become more tolerant to burst errors occurring at the beginning of the codeword. The rearranged matrix is organized as follows: $H_b(1{:}69) = [H_a(18{:}57), H_a(1{:}17), H_a(58{:}69)]$, and it is depicted in Fig. 4(b). The original 12 columns of parity checks are unchanged to make the decoding complexity unaffected. To explore the worst-case burst-mode performance, another H-matrix (H_c) is rearranged in the opposite way where $H_c(1{:}69) = [H_a(68{:}69), H_a(1{:}67)]$, and it is depicted in Fig. 4(c).

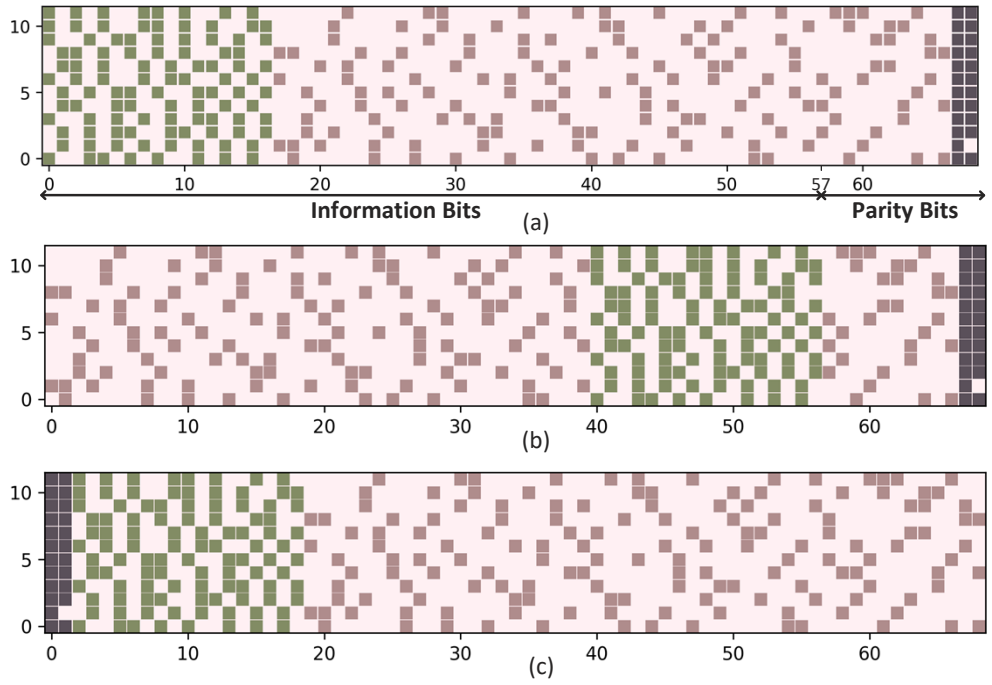

Fig. 4. Three parity-check matrix column arrangements of the same LDPC mother code: (a) H_a, (b) H_b, and (c) H_c.

Based on the FPGA system in Fig. 1(a), using the 8 bits $\alpha_{v'c}^{k,l}$ and $\beta_{cv}^{k,l'}$ with 5 integer bits, 2 fraction bits and 1 bit for sign, we implemented LDPC codes with these three parity-check matrices and test their coding performance by employing a decoder with 12 layered and 15 iterations. To compare with the interleaving case, we also test the performance of same two interleaving methods with the ones we use for regular LDPC code in Section 3 based on the H_b only. The performance improvement of the interleaving method with the H_a and H_c will be a similar trend as the case of H_b. The results are labeled with IR_n ΔSNR = m dB, where n = a for the performance of H_a, b for the performance of H_b, c for the performance of H_c, n = i for the performance of interleaved case of 8 pieces, and n = ii for the performance of interleaved case of 2 pieces respectively. In Fig. 5(a), corresponding to an LDPC decoder output BER of 10^{-9}, IR_a ΔSNR = 3 dB, IR_a ΔSNR = 2 dB, and IR_a ΔSNR = 0 dB require the input BERs to be 2.42×10^{-2} (corresponding to a Q-factor value of 5.91 dB), 2.51×10^{-2} (5.84 dB), and 2.60×10^{-2} (5.77 dB), respectively. Compared to the regular LDPC code without interleaving we tested in Section 3, the irregular LDPC code matrix H_a performances are well maintained

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(within ~0.2 dB) for non-uniform input bit error distributions where the errors are concentrated at the first 1/8 of each codeword due to an SNR (or power) reduction of up to 3 dB. The water fall shape is also well maintained for different burst mode errors scales. The performance of regular LDPC code is slightly better than irregular LDPC code due to its lower code rate, when interleaving is used. The irregular structure of the quasi-cyclic (QC) code helps us to effectively combat the burst errors by belief propagation variation. With layered decoding, the *a posteriori* probability for those affected bits by upstream burst can be improved layer-by-layer from check-node-to-variable-node and variable-node-to-check-node information exchange in the iteration process. Therefore, the 1/8 of affected bits in one codeword can be corrected with very little penalty. However, unfortunately, the performance of the H_a decrease when suffering higher burst mode errors. Based on the result from Section 3, we know that it is possible to have higher coding performance for the non-uniformly distributed burst errors channel model. By comparing the Figs. 5(a)–(e), the interleaving of 8 pieces method provides the best performance. For an LDPC output BER of 10^{-9}, IR_i ΔSNR = 3 dB, IR_i ΔSNR = 2 dB, and IR_i ΔSNR = 0 dB requires the input BERs to be 2.95×10^{-2} (corresponding to a Q-factor value of 5.52 dB), 2.78×10^{-2} (5.64 dB), and 2.60×10^{-2} (5.77 dB), respectively. Compared to the case of IR_i ΔSNR = 0 dB, the case of IR_i ΔSNR = 3 dB improves the Q-factor by ~0.25 dB after suffering the non-uniformly distributed errors with 3 dB SNR (or power) reduction. Compared to the case of IR_a ΔSNR = 3 dB, the improvement from the case of IR_i ΔSNR = 3 dB is around 0.45 dB. However, the method of interleaving of 8 pieces requires the exact knowledge of the burst mode errors duration and rearranging bits instead of blocks. The results of the interleaving case of 2 pieces, depicted at Fig. 5(e), indicate the little improvement, thus supporting this observation. Rearranging or interleaving bits will not maintain the cyclic shift block structure of the parity check matrix. It leads to extra energy and latency cost at encoder and also increases the complexity of the decoder design. The second best performance comes from the rearranged matrix H_b. For the output BER threshold of 10^{-9}, IR_b ΔSNR = 3 dB, IR_b ΔSNR = 2 dB, and IR_b ΔSNR = 0 dB require the input BERs to be 2.72×10^{-2} (corresponding to a Q-factor value of 5.68 dB), 2.67×10^{-2} (5.72 dB), and 2.60×10^{-2} (5.77 dB), respectively. Compared to the case of IR_b ΔSNR = 0 dB, the performance of the matrix H_b improves the Q-factor by ~0.1 dB after suffering the non-uniformly distributed errors with 3 dB SNR (or power) reduction. Compared to the case of IR_a ΔSNR = 3 dB, the improvement from the case of IR_b ΔSNR = 3 dB is around 0.3 dB. Compared to the parity-check matrix H_a, the parity-check matrix H_b is derived by cyclic shift of the columns in information bits of the H_a-matrix. It will not cost extra latency and complexity when implementing in FPGA/ASIC. The reason of the improvement coming from H_b-matrix is that the lower column weight at beginning of the codeword that suffers more impairments get involved in smaller number of check nodes in decoding process and vice versa for the higher column weights at the ending portion of the H-matrix. The FPGA emulations corresponding to the H_c-matrix, depicted at Fig. 5(c), indicate the worst BER performance, thus supporting this observation. There are many combinations for arranging the parity-check matrix to get a better burst error performance. Reversing the information related columns is another choice. Also, because the burst mode is a well-defined, as long as we move some low weight columns to the left, we will get some benefit. Therefore, the answer for the second question would be: by rearranging the parity-check matrix of the irregular LDP code by matching the lower column weight to the bits in burst mode it is possible to get better coding performance under the burst error channel model introducing the non-uniformly distributed errors, without extra cost for interleaving codewords.

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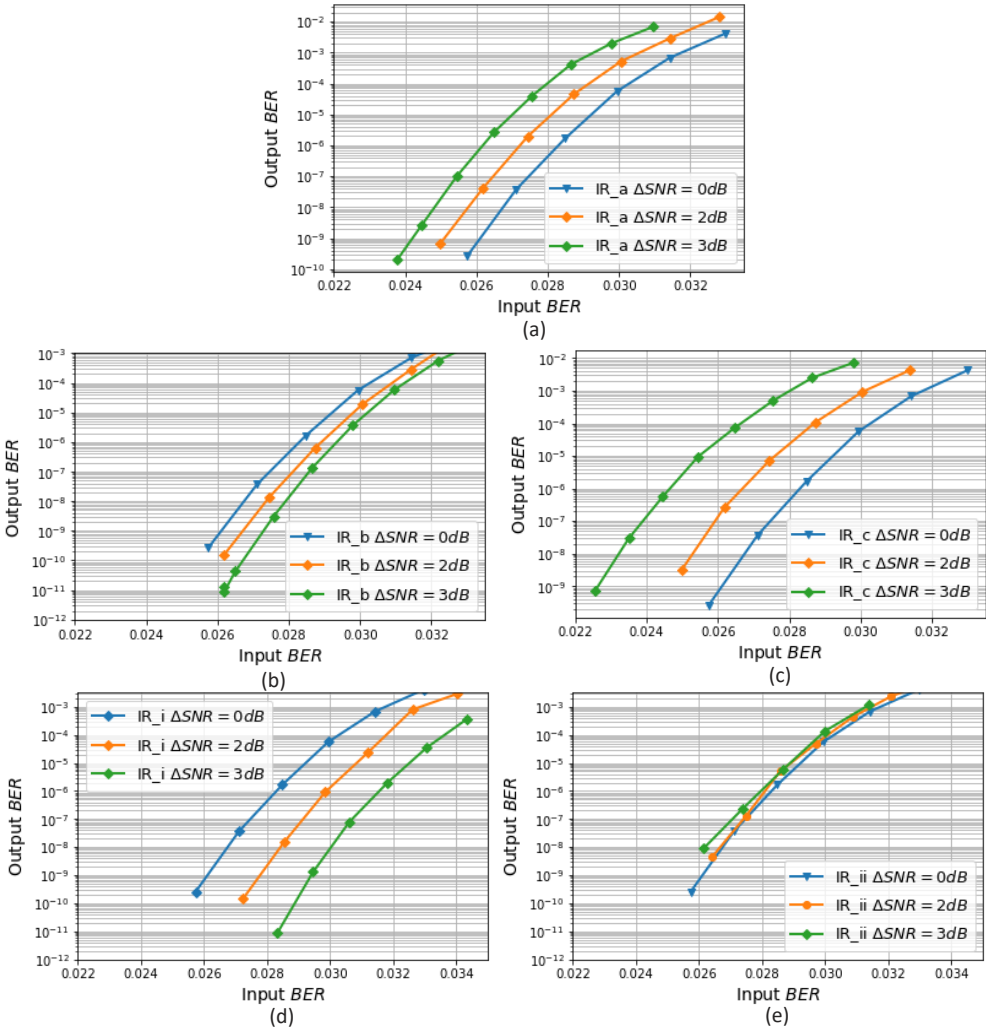

Fig. 5. Error correction performance for different parity-check matrices: (a) H_{a}, (b) H_{b}, (c) H_{c}, (d) intra codeword interleaved case of 8 pieces based on H_b, and (e) intra codeword interleaved case of 2 pieces based on H_b

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5. Concluding remarks

We have evaluated the error-correction performance of the regular LDPC code under the burst mode errors with and without interleaving in PON scenario. We also evaluated the performance of the rearranged and interleaved irregular LDPC code that was under study by ITU-T's 50G-PON group for burst mode upstream reception operation. Real-time measurements have been done by using the Ultrascale FPGA. It has been found that without using interleaving, the regular LDPC code performance get affected tremendously for non-uniform input bit error distributions, where the errors have been concentrated at the first 1/8 of each codeword (due to a SNR degradation of up to 3 dB), corresponding to ~44 ns (~88 ns) for a 50-Gbps (25-Gbps) upstream signals. In the same condition, the irregular LDPC code performance has been well maintained and can be noticeably improved by properly rearranging the columns of its parity-check matrix such that the beginning parity-check matrix columns have the smallest weight (of 3). Although properly interleaved regular LDPC code and irregular LDPC code both provide excellent performance, this approach brings extra energy and latency cost and require the knowledge of accurate burst mode errors duration in advance. Compared to the interleaving, the rearrangement design improvement can be obtained without affecting the complexity or latency of the LDPC encoder and decoder, making it beneficial for 50G-PON (and possibly 100G-PON) burst-mode upstream transmission for the next-generation optical access networks. Thus, the LDPC design described in [4–8] can be potentially improved by rearrangement for both downstream and upstream transmissions in TDM-PON, and may find valuable applications in future broadband fiber access networks such as 50G-PON and beyond.

Disclosures. The authors declare no conflicts of interest.

Data Availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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