A ±0.5 dB, 6 nW RSSI Circuit With RF Power-to-Digital Conversion Technique for Ultra-Low Power IoT Radio Applications

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***Abstract*— This paper presents a new technique of radio frequency (RF) signal strength detection with a received signal strength indicator (RSSI) circuit which can be deployed in an internet-of-things (IoT) network. The proposed RSSI circuit is based on a direct conversion of RF to digital code indicating the signal strength. The direct conversion is achieved by the repeated switching of a rectifier's output voltage using an ultra-low power comparator. A 5-bit programmable feedback circuit is used to correct detection inaccuracies. The RSSI circuit is implemented in a 65-nm CMOS process and consumes 6nW power. It has a linear dynamic range of 26dB and exhibits an error of ±0.5dB with a wide bandwidth of 750MHz. A detailed analysis of the RSSI circuit is presented and verified with simulation and measurement results. The high detection accuracy with ultra-low power consumption of our RSSI circuit is favourable for IoT applications including localization, beamforming, hardware security and other low-power applications.**

***Index Terms*— Received signal strength indicator (RSSI), Internet of Things (IoT), wireless networks, radio frequency (RF), hardware security.**

I. Introduction

THE growth of internet-of-things (IoT) network is unleashing a new era of low-power connected devices with an anticipated 75 billion IoT devices being expected to be connected in the network by the year 2025 [1]. Enabling wireless technologies such as Bluetooth, ZigBee, LoRaWAN, and SigFox have technologically advanced wireless communication in the IoT landscape. However, a reliable communication in a densely deployed network of IoT devices with shared spectrum is becoming increasingly challenging.

The reliability of wireless communication is challenged by several issues on account of "hostility" of the wireless channels. The spatio-temporal fluctuations in the wireless channel which include shadowing, multipath propagation, propagation loss, and inter symbol interference (ISI) affect the transmitted signal by introducing random variations in the signal strength to cause variations of orders of magnitude.

The high variation in the received radio frequency (RF) signal, requires a wide dynamic range detection circuit for the RF receivers to be robust and adaptive to fluctuations. RF receivers must be sensitive to low magnitude signal while also ensuring that a higher magnitude input signal does not lead to internal saturation.

Various magnitude control architectures including limiting amplifier (LA) [2]–[7] and automatic gain controller (AGC) [8]–[10] have been used to control the magnitude of the received signal to prevent the RF receivers from saturating. Fundamentally, these architectures are based on power detection of the received signal, where input power level is used to control the gain. The strength of the incoming signal in these magnitude control architectures is conventionally detected by the received signal strength indicator (RSSI) amplifier. Conventional RSSI circuit is a logarithmic amplifier that provides an output DC voltage to the corresponding input RF power. It can be used for monitoring and signal processing to control the gain in the RF signal chain. The logarithmic characteristic of the RSSI circuit is used to map a wide dynamic range of the signal on to a relatively limited output voltage range.

To assess and use the "best" communication channel, RSSI circuit is deployed as a signal quality measurement tool in the RF receivers [11]–[13]. Other applications in the IoT realm include localization [14], smart storage systems [15], biomedical applications like human body communication [2], wireless beamforming [14] and seizure detection [16] among others. The mandatory requirement of RSSI in the physical layer (PHY) of IEEE 802.15.4 protocol stack makes RSSI an indispensable part of the RF receivers [17].

With such a critical and integral role of the RSSI circuit in RF receivers, optimizing its key parameters such as power consumption, dynamic range, and detection accuracy is critical to the optimization of the entire RF receiver. RSSI designs in the

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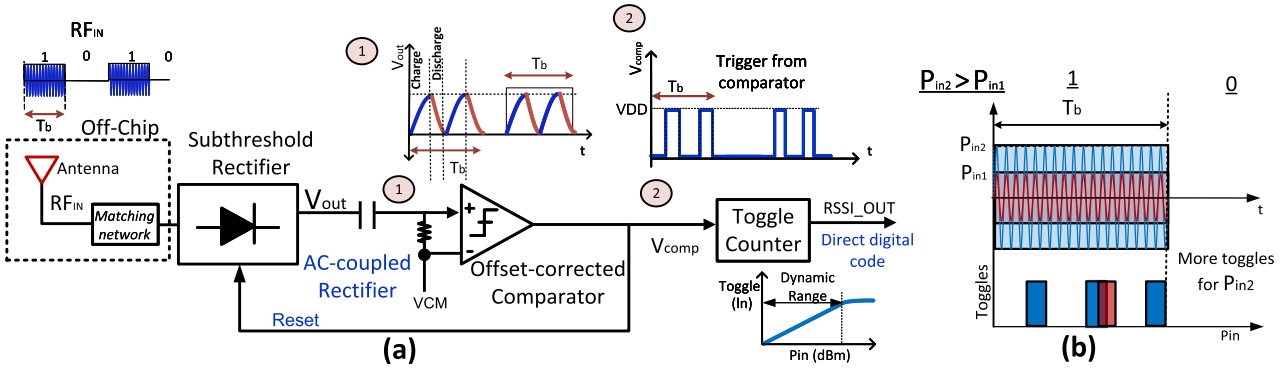

Fig. 1. (a) The RSSI circuit directly converts the input signal power to a digital code where the number of toggles (N) vary with the incoming signal strength (dBm). (b) The strength incoming RF signal is detected by the unique signature generated in the RSSI circuit.

literature for various applications have reported dynamic range >50dB with detection accuracy ranging from ±1 to ±2dB and power consumption in the range of few mWs [2], [3], [5], [6]. The higher dynamic range at the cost of such high power consumption is not a feasible scenario considering IoT devices are operated using small batteries. While ultra-low power RSSI circuits have recently been reported [18], these RSSI circuits cater to only low frequency (in kHz) biomedical EEG applications. With ultra-low power (ULP) consumption, IoT devices can potentially thrive on a self-sustained energy system with energy harvesting, overcoming limitations of battery-based systems [19].

In this paper, an ultra-low power RSSI circuit is designed in 65-nm CMOS technology which directly converts the input RF power to a digital signal, indicating the strength of the incoming signal. The RSSI design has a sensitivity of −55dBm. It has a dynamic range of 26dB, power consumption of 6nW, and detection accuracy of ±0.5dB with the highest reported figure of merit (FOM) among the state-of-the-art designs. The rest of the paper is organized as follows. Section II discusses conventional architecture and the architecture of this RSSI circuit. Section III provides the details of the circuit design. In Section IV, we provide an analysis of the design. Measurement results are presented in Section V. Finally, conclusions are presented in Section VI.

II. RSSI Architecture

Successive detection architecture (SDA), is the conventionally used RSSI architecture. SDA architecture consists of cascaded limiting amplifiers (LA) and full wave rectifiers (FWR) in each stage and generates an output which is proportional to the logarithm of the input signal. It has a relatively lower power consumption compared to the other reported architectures [6].

Based on the equations of dynamic range and accuracy, which are the critical parameters of the RSSI circuit [3], it is observed that increasing the number of stages (n) and the gain per stage of the limiting amplifier improves the dynamic range and the accuracy of detection.

Optimization of these parameters would lead to an increased overall power consumption for detection in addition to the area overhead. In addition to detection, magnitude control of the incoming signal with architectures like AGC using digital signal processing step would also incur extra power consumption. In this work, a different RSSI design architecture is presented over the conventional SDA-based signal detection. Through a direct conversion of RF signal to a digital code, the detection and processing steps are combined at ultra-low power consumption with a lower area overhead.

A. Design Architecture

Fig. 1(a) shows the architecture of the RSSI circuit. It is based on the envelope detection of the incoming signal RF_{IN}, which is implemented using a multi-stage passive rectifier. RF_{IN} is rectified and the output V_{out} is AC-coupled to an ultra-low power comparator. This output voltage of the rectifier triggers the comparator to generate a '0' or a '1'. The output of the comparator is fed back to the multi-stage passive rectifier. Each stage of the rectifier consists of a discharge switch which effectively discharges the output of the rectifier by discharging each stage of the rectifier. Based on the control signal from the comparator, discharge event happens for a $0 \rightarrow 1$ transition. In the symbol duration T_b, the incoming signal initiates another cycle, charging the rectifier output node. This again triggers the comparator and leads to another cycle of the discharge. The repeated cycle of charging-discharging (toggle) of the rectifier output in the duration T_b of the incoming signal RF_{IN}, triggers the comparator output to '1/0' respectively and creates a unique digital signature indicating the strength of incoming signal. Thus, a higher strength signal leads to multiple charge−discharge events at the output of the comparator.

Fig. 1(b) shows that for two different incoming signal strength P_{in1} and P_{in2}, the strength of the incoming RF signal is uniquely identified by the different toggling output of the RSSI circuit. A higher power signal P_{in2} charges the rectifier output faster than the lower power signal P_{in2} in the period T_b and hence leads to a higher number of output toggles. The number of toggles at the RSSI output increases with the input signal strength. It enables input power detection with a high accuracy. The direct conversion of the input signal to a digital word provides several advantages:

1) Direct Digitization of the RF Signal: The direct conversion of the signal strength to a digital code can be used to indicate and control the magnitude of the incoming signal, eliminating the need for further post processing like code word generation in AGC based architecture [10]. The direct conversion eliminates the need of analog to digital converter (ADC), which would otherwise require a higher dynamic range leading to a higher area and power overhead [20], [21].

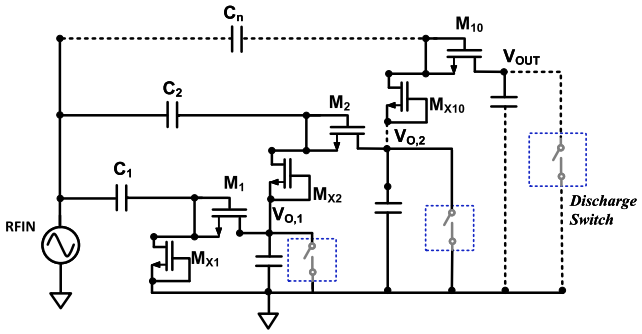

Fig. 2. Modified 10–Stage Dickson based passive rectifier with the discharge switch for energy detection of the incoming RF signal.

2) Noise Resilience: To assess the accuracy of the link quality, it is important to characterise the in-band interference and the ambient channel noise. This RSSI circuit can characterize the in-band interference and the ambient channel noise, which can be used to set the threshold before the actual channel estimation [22].

3) Higher Accuracy: In this RSSI design, a high accuracy in the signal strength detection is achieved. This is advantageous for applications like localization, where the detection accuracy is a critical specification [23].

4) Diverse Applications: In addition to enhancing the viability of novel wireless techniques like beamforming [14] on account of better accuracy, the ultra low power consumption of the RSSI circuit is favourable for the low power IoT applications like link quality assessment, RF energy harvesting, backscatter communication, and secure wireless communication among others.

III. Circuit Implementation

A. Rectifier

Fig. 2 shows a modified Dickson charge pump with a 10-stage rectifier which is used to perform power detection of the incoming RF signal. The output of the rectifier is a DC signal with small ripples. The input to successive stages swings on top of the DC level of the previous stage, which results in a higher output voltage. The rectifier must exhibit high voltage conversion across a wide range of the input powers in order to achieve the desired dynamic range for the RSSI-based detection. Fig. 2 shows multiple half wave rectifiers cascaded to provide a higher output voltage. For the incoming signal of amplitude V_A, with a large dynamic range, the transistors in the diode configuration may operate either in the subthreshold or in the saturation region. For low strength signal, the transistors primarily operate in the subthreshold region. In Table I, device implementation details for the rectifier design are presented.

1) Sensitivity: For the RSSI circuit, sensitivity is defined as the minimum input power (dBm) for which the circuit consistently generates at least one toggle at the output. This minimum detectable signal sets the lower limit of the dynamic range of detection. The rectifier is followed by the comparator, and hence the rectifier output voltage must reach the threshold voltage of the comparator (V_{sw}) within the duration of the incoming RF signal. Fig. 3(a) shows the simulation results of the output voltage of the rectifier for different power levels marked with the switching threshold (V_{sw}). Although the use of passive rectifiers limits the sensitivity when compared to active rectifiers, they are instrumental in enabling the ultra-low power operation. The 10-stage rectifier can detect signals at −55dBm (with matching network).

TABLE I
Device Implementation for Rectifier

Device	Type	Property
M_{1-10}	NCH_LVT	W/L=200n/60n
$M_{x(1-10)}$	NCH_LVT	W/L=200n/60n
C_{1-10}	MIM	200 fF

2) Timing Analysis of the Rectifier: The time for the rectifier output voltage to reach to V_{sw} depends on several factors and a detailed analysis is presented below for the half wave rectifier and is extended to an n-stage rectifier.

In the sub-threshold region of operation, the transistor drain current is given by,

$$I_D = I_S e^{(V_{GS}-V_{TH})/\eta V_t}(1 - e^{-V_{DS}/V_t}) \tag{1}$$

where I_S is the sub-threshold saturation current, η is the sub-threshold ideality factor, V_t is the thermal voltage given by kT/q, V_{TH} is the threshold voltage, and V_{GS} is the gate-source voltage. $V_{GS} = V_O - V_A cos\omega t$ where V_O is the output of each stage. The DC output or average current from the rectifier can be calculated by

$$I_O = \frac{1}{T} \cdot \int_0^T I_D \cdot dt \tag{2}$$

To simplify an otherwise involved equation [24], the sinusoidal input of an amplitude V_A is approximated with a square wave of amplitude $k \cdot V_A$ as shown in Fig. 3(b), assuming that the scaling factor k for the square wave provides the same output power as the sinusoidal wave input. As the transistors are connected in the diode configuration, V_{GS}=V_{DS}, the resulting equation, assuming a square wave input, is given by,

$$I_O \cong \frac{I_{ST}}{T} \cdot \int_0^{T/2} e^{(k\cdot V_A - V_O)/\eta V_t}(1 - e^{(-k\cdot V_A + V_O)/V_t}) \cdot dt - \frac{I_{ST}}{T} \cdot \int_{T/2}^{T} e^{(0)/\eta V_t}(1 - e^{-(k\cdot V_A + V_O)/V_t}) \cdot dt$$

where $I_{ST} = I_S \cdot e^{-V_{TH}/\eta V_t}$, and $V_{GS} = 0$ during the reverse bias phase.

For $kV_A \gg V_0$, the equation resolves to

$$I_O = \frac{I_{ST}}{2}(e^{k\cdot V_A/\eta V_t} - 1) \tag{3}$$

At lower input powers with $k < 1$ and $\eta > 1.2$, $kV_A \ll \eta V_t$. I_O using Taylor's expansion can be written as

$$I_O \cong \frac{I_{ST}}{2} \cdot (\frac{k \cdot V_A}{\eta V_t}) \tag{4}$$

Time required (t_{stage}) for the rectifier output (single stage) to reach the switching voltage of comparator V_{sw},

$$\int_0^{V_{sw}} C \cdot dV = \int_0^{t_{stage}} I \cdot dt$$

$$t_{stage} = (\frac{2 \cdot C \cdot V_{sw} \cdot \eta \cdot V_t}{I_{ST} \cdot k}) \cdot (V_A)^{-1}$$

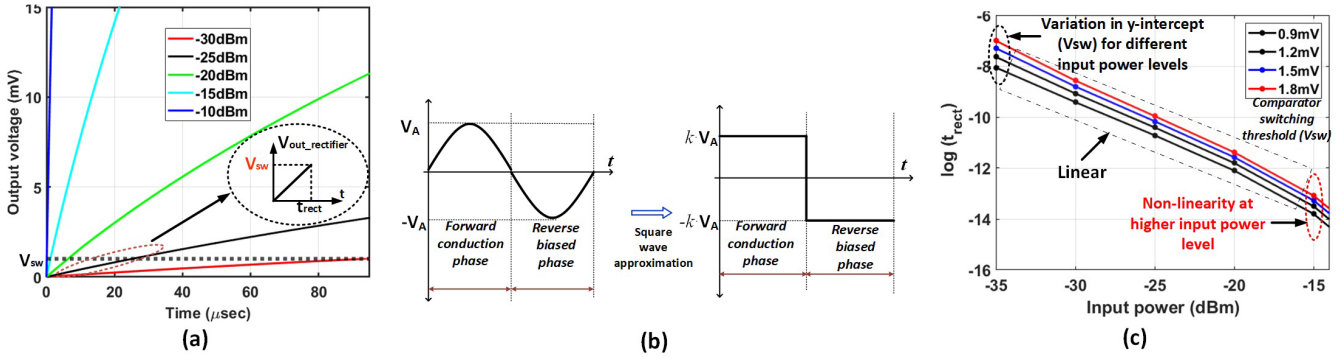

Fig. 3. (a) Output of the 10-stage Dickson charge pump for different input power levels of the RF signal, (b) Square wave approximation for analysis, (c) Simulation results of the rectifier timing response for different switching voltage of the comparator.

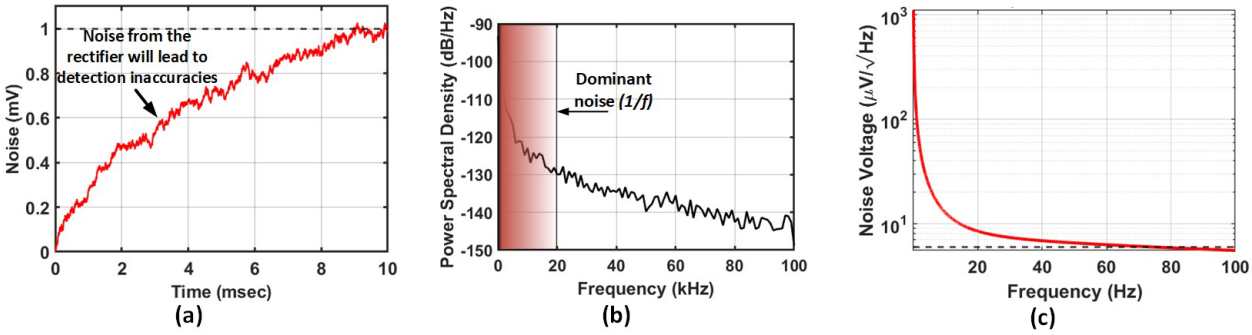

Fig. 4. (a) Transient noise analysis of the rectifier, a high value can trigger the comparator, (b) Power spectral density (PSD) plot of the noise, (c) The noise is dominant in the low frequency region.

For $n-stage$ rectifier,

$$t_{rect} \cong \left(\frac{2 \cdot C \cdot V_{sw} \cdot \eta \cdot V_t}{I_{ST} \cdot k \cdot k'}\right) \cdot (V_A)^{-1} \tag{5}$$

where k' represents the scaling factor of the n-stage rectifier.

For the conventional n-stage Dickson charge pump, $k' \approx n$, when the rectifier output reaches the maximum open circuit voltage. In the modified rectifier, the output charges only upto V_{sw} as it enables the discharge switch in each stage, effectively discharging the rectifier output before it settles to the open circuit voltage implying $k' < n$.

Taking natural logarithm on both sides in Eq. 5 and based on the conversion of V_A to P_{in}(dBm) by the relation,

$$P_{in}(dBm) = 10 \cdot \log_{10}\left(\frac{V_A^2}{2R_{in} \cdot 10^{-3}}\right)$$

where R_{in} in the input impedance of the rectifier, t_{rect} (after conversion of $\log_{10}$ to natural logarithm, $\log_e$ scale) can be finally written as,

$$\ln(t_{rect}) = -(A \cdot P_{in} + B) + \left[\ln\left(\frac{2 \cdot C \cdot V_{sw} \cdot \eta V_t}{I_S \cdot k \cdot k'}\right) + \frac{V_{TH}}{\eta V_t}\right] \tag{6}$$

where A and B are constants with $A = \frac{\ln(10)}{20}$ and $B = \frac{1}{2}\ln(2R_{in} \cdot 10^{-3})$.

Several important conclusions can be drawn from Eq. 6 that give an insight on the design of rectifiers operating in the sub-threshold region. First, $(\ln(t_{rect}))$ is a linear function of P_{in}, which is an important result, as a linear relation between the number of toggles $(\ln N)$ and the input power (expressed in dBm) is derived later. The negative slope is an anticipated result as rectifier time (t_{rect}) must decrease with increasing input voltage. Second, based on the above analysis from Eq. 6, the threshold voltage variation does not affect the slope of the curve and it can be corrected in the initial calibration along with the temperature dependant term $(V_{TH}/\eta V_t)$. To confirm the above analysis, simulations of the rectifier response time at different input power levels are presented in Fig. 3(c). The variation in the switching voltages changes the y-intercept while the slope of the curve remains the same in accordance with Eq. 6. At higher input power levels, the transistors shift from sub-threshold to saturation region of operation which imparts a non-linear characteristic and limits the dynamic range of detection. Under this constraint, techniques to extend the dynamic range are discussed in Section V.

3) Noise Analysis of the Rectifier: Sensitivity of the rectifier can be limited by the noise from the rectifier. If the noise of the rectifier exceeds the minimum detectable signal level of the rectifier, it will affect the overall sensitivity which limits the dynamic range of input signal power detection. The noise simulation shown in Fig. 4(a) reveals that the noise from the rectifier alone is high enough to trigger the comparator which may lead to detection inaccuracies from the undesired toggling of the output node of the RSSI circuit. From Fig. 4(b), it is observed that the noise from the rectifier is dominant in the lower frequency range (hundreds of Hz). From Fig. 4(c), the magnitude of noise reaches to 1mV in the lower frequency range $(1-10Hz)$. To mitigate the effects of this low frequency noise, a low frequency noise cancellation

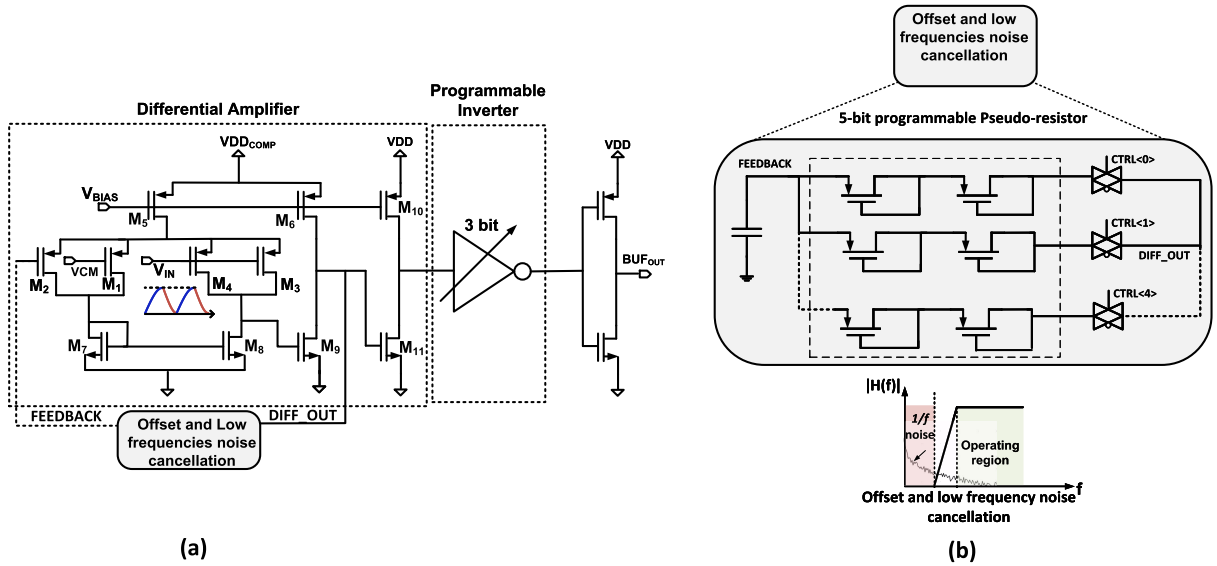

Fig. 5. (a) Ultra-low power comparator schematic composed of amplifiers and digitizing inverters, (b) DC offset and low frequencies noise cancellation circuit.

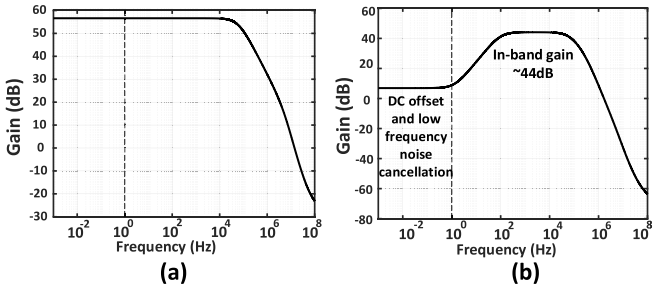

Fig. 6. Simulation results for (a) Open-loop response of the comparator (b) Closed loop response with offset-noise correction feedback loop.

circuit is implemented in the feedback loop of the comparator. The design details of noise cancellation are discussed in Section III-B

B. Comparator

Fig. 5(a) presents the schematic of the comparator which is a differential amplifier followed by a common source stage. Transistors $M_3 - M_4$ are used to sense the output voltage of the rectifier (V_{IN}) and transistor M_1 is held at the common−mode level. The bias current of the comparator is 4nA which includes bias for diff-amp stage and programmable inverter. In Table II, device implementation details for the comparator design are presented. The comparator is triggered by the output of the rectifier, with switching threshold as labelled in Fig. 3(a). A tunable switching threshold for the comparator is implemented with a 3-bit programmable inverter which can also aid in dynamic range enhancement. To improve the precision of the detection, a configurable negative feedback circuit is implemented in the comparator which alleviates the sources of error.

1) Feedback Circuit: The device mismatch in the comparator generates non-ideal effects resulting in an input referred offset voltage. This input referred offset voltage can lead to significant accuracy errors in the detection of signal strength. Another source of error is the noise from the rectifier (dominant at low frequencies) which was discussed in Section III-A.

TABLE II
DEVICE IMPLEMENTATION FOR COMPARATOR

Device	Type	Property
M_1,M_2, M_3,M_4	PCH	W/L=500n/500n
M_5,M_6	PCH	W/L=200n/60n
M_7,M_8	NCH_LVT	W/L=1μ/500n
M_9	NCH_LVT	W/L=2μ/500n
M_{10}	PCH	W/L=800n/200n
M_{11}	NCH_HVT	W/L=200n/1μ

From Fig. 4(a), it is observed that the integrated noise is sufficiently high (1mV) at lower frequency to trigger the comparator even in the absence of an incoming signal. This would lead to an incorrect toggle from the comparator, introducing inaccuracies in the detection. By using a first order low pass filter in the feedback loop of comparator as shown in Fig. 5(b), both DC offset and the dominant *1/f* noise from the rectifier can be corrected. The offset in the design is corrected by removing the offset of the first stage amplifier while the succeeding inverter helps in achieving the digitizing functionality as expected from a comparator.

The closed loop frequency response of comparator is given by,

$$A(s) = \frac{V_0(s)}{V_{in}(s)} = A_0 \cdot \frac{(s\tau_z + 1)}{(s\tau_{p1} + 1) \cdot (s\tau_{p2} + 1)} \tag{7}$$

where A_0 represents the small signal gain and τ_{p1}^{-1} and τ_{p2}^{-1} represent the output poles of the differential amplifier and the CS stage respectively. The feedback network introduces a zero τ_{z1}^{-1} in the frequency response. This zero (τ_{z1}^{-1}), cancels the sources of errors limited to low frequencies and also improves the stability of the circuit. This attenuates both the DC and low frequency signal.

Fig. 6(a) shows the simulation result for the open loop frequency response of the comparator. In Fig. 6(b), the simulation result for the response of the comparator with the feedback loop is presented. The comparator with the feedback loop

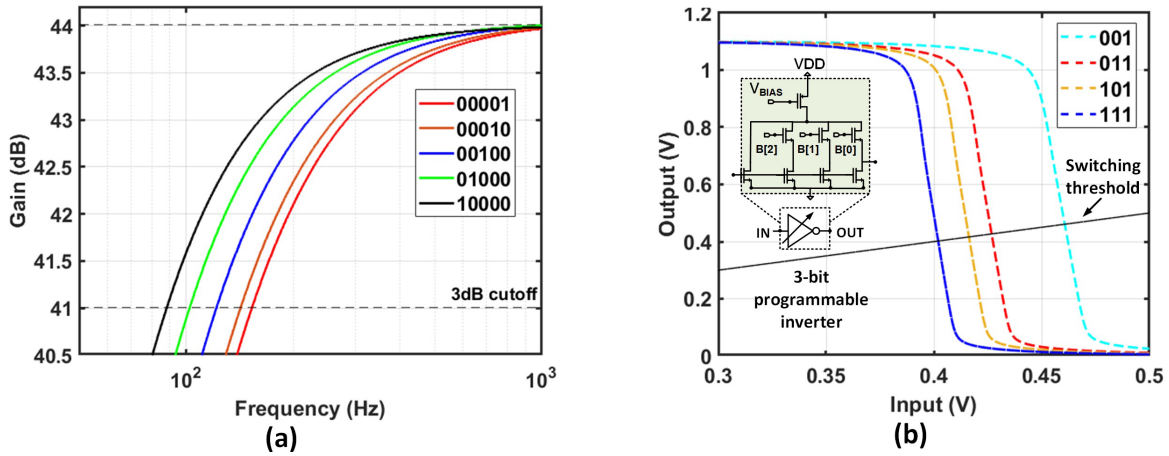

Fig. 7. Simulation results for (a) 5-bit programmable pseudo-resistor based feedback network, (b) 3-bit programmable inverter.

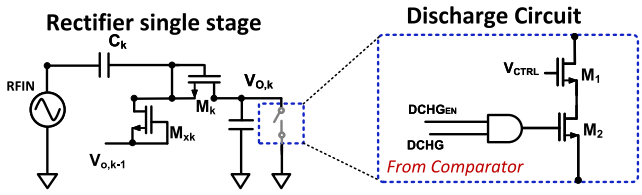

Fig. 8. Discharge switch triggered by the comparator output included in each stage of the rectifier for a faster discharge of the rectifier output.

shows a flat band gain of 44dB, 3dB bandwidth of 60kHz, and 0dB bandwidth of 1MHz. The attenuating behavior of the comparator at low frequencies removes the effects of the DC offset and *1/f* noise from the rectifier. It should be noted that the feedback loop does not attenuate the incoming signal in the range of interest (a few kHz to MHz).

To cancel the low frequency signals in the order of hundreds of Hz would require a significantly high value of resistor in the low pass filter based feedback network. With a capacitance of 10pF realized using an on-chip metal-insulator-metal (MIM) capacitor, a resistance of 1-10GΩs would be required. The requirement of such a high resistance is practically infeasible if realized on-chip with a poly-silicon based resistor. Pseudo-resistor [25], which is essentially a MOS transistor connected in the diode topology can present a high resistance and is an alternate way to realize high on-chip resistors. Although, pseudo-resistor as a simple topology can achieve such values of resistance, process variation affects its resistance value significantly. To account for the process variability of the pseudo-resistor based topology, a 5-bit tunable pseudo-resistor network is implemented achieving different cut-off frequencies as shown in Fig. 7(a). This one time setting of the cut-off frequency is a part of the initial calibration setup of the RSSI circuit. Using this tunable setup, a variation of more than 2× in the value of the pseudo-resistor can be controlled.

2) Programmable Inverter: Device mismatch related offset is removed from the comparator because it can cause a large variation in the comparator's switching threshold. However, a 0-offset comparator can start toggling due to noise. The switching threshold of the comparator therefore is made tunable with the following 3-bit programmable stage inverter to keep it above noise. Fig. 5(a) shows the inverter which can have a small influence on the comparator's switching threshold. From Fig. 7(b), a tunability range of up to 100mV in the switching threshold of the inverter can be achieved with different settings of the programmable inverter. This translates to a tunable switching threshold control of up to 0.5mV at the comparator input. Along with the offset and low frequencies noise correction in the comparator, the programmable inverter in different settings can be used to control switching threshold of the comparator to correct for any additional noise. This additional correction is part of the initial calibration process.

3) Timing Analysis: The output of the rectifier ($V_{out,rect}$) is AC-coupled to the input of the comparator ($V_{in,comp}$) and can be approximated as a ramp function as shown in Fig. 3(a) (inset)

$$V_{in,comp}(t) = V_{out,rect}(t) = \frac{V_{sw}}{t_{rect}} \cdot t \tag{8}$$

where t_{rect} is the time to reach the switching voltage V_{sw} of the comparator and is calculated from Eq. 5.

Using Eq. 7 and 8, a detailed analysis if undertaken, shows an exponential relation between t_p and input power (dBm), and $t_p \ll t_{rect}$. For the sake of brevity, simulation results are directly presented in Fig. 9(a), to demonstrate that the magnitude of the comparator delay does not have a significant impact on the toggling rate of the RSSI output as overall delay is dominated by the rectifier.

C. Discharge Circuit

To discharge the output of the rectifier based on the trigger from the comparator, a discharge switch as shown in Fig. 8, is incorporated in all stages of the 10-stage rectifier.

The discharge switch has transistors M_1 and M_2 in the cascode configuration where voltage V_{CTRL} is the gate voltage of M_1, M_2 and is controlled by the gated signal $DCHG$ and external signal $DCHG_{EN}$. $DCHG_{EN}$ is the output of the comparator, intentionally slewed to prevent charge-feedthrough issues from quick successive transitions of the comparator output. $DCHG_{EN}$ is asserted when RSSI based detection is performed. To enable a faster discharge of the multi-stage rectifier, this discharge switch is included in each stage of the rectifier to discharge the rectifier completely without any residual charge.

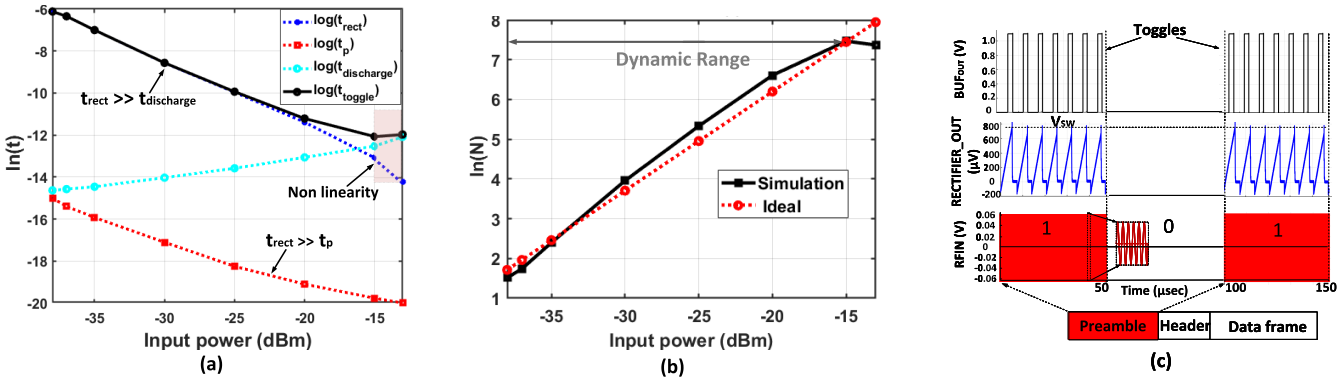

Fig. 9. (a) Simulation results of relation of different timing arcs with the input power for the RSSI circuit. Overall timing t_{toggle} mainly depends on t_{rect}, (b) Simulation result of the number of toggles at the RSSI output for different input powers, (c) Simulation results of a simplified scenario of signal estimation for the RSSI circuit with an input power of -20dBm. The output toggles correspond to the input signal strength.

1) Timing Analysis: In Fig. 9(a), simulation result of rectifier discharge time, $t_{discharge}$ with input power is presented. The comparator is triggered once the rectifier voltage reaches V_{sw} (Fig. 3(a)). The discharge circuit has to discharge the rectifier output (V_{sw}) irrespective of the input power level implying a constant discharge time. In Fig. 9(a), it is observed that the discharge time is a nearly constant timing arc for lower input powers.

D. Toggle Counter

The toggle counter presented in Fig. 10, indicates the digital word corresponding to the power of the incoming signal. Each charge-discharge cycle of the rectifier in a given symbol, in the bit period T_b (Fig. 1) results into a toggle at the output of the comparator which is counted by the toggle counter. The programmable reset block in the toggle counter is a standard 3-bit counter which resets the 10-bit counter. For the incoming RF signal, the toggle counter counts each toggle at the RSSI output. In the absence of the RF signal (symbol '0'), the programmable reset block then resets the 10-bit counter for the next counting period. The absence of RF signal is detected once the $RESET\_OUT = 111$ based on the counting of clock (CL) pulses. The clock signal (CL) driving the programmable reset block is a 32kHz real time clock (RTC) commonly available in various IoT application.

While this RSSI circuit consists of 10-bit counter, a higher bit counter (11 or 12-bit) will have better coverage of the entire dynamic range of signal detection. The post layout power consumption of the toggle counter is 0.5nW from 0.6V supply. ULP RTC clock will add an additional few nWs to the overall power consumption [26], [27].

IV. Analysis

A. Toggle Rate Calculation

The toggling rate is calculated based on the timing delay of the entire path i.e. charge-discharge path of the rectifier output. In Fig. 9(a), different logarithmic relation between the different timing arcs and the input power is presented.

The total time for a single toggle is given by t_{toggle}

$$t_{toggle} = t_{rect} + t_p + t_{discharge}$$

Based on the results in Eq. (6) and simulation results in Fig. 9(a), it is observed that for lower powers,

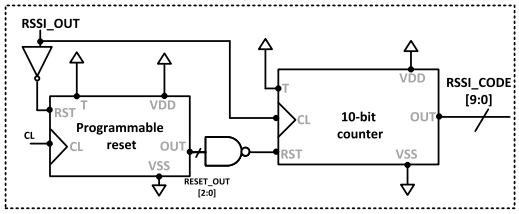

Fig. 10. Toggle counter design to indicate the digital code corresponding to the power level of the incoming RF signal.

$t_{rectifier} \gg (t_p + t_{discharge})$. This simplifies the number of toggles of the RSSI output as,

$$N = \frac{T_b}{t_{rect} + t_p + t_{discharge}} \approx \frac{T_b}{t_{rect}}$$

Substituting the value of t_{rect} from Eq. 5 and taking natural log on both sides,

$$\ln(N) = (AP_{in} + B) + \left[\ln\left(\frac{T_b I_S k' k}{2CV_{sw}\eta V_t}\right) - \frac{V_{TH}}{\eta V_t}\right] \quad (9)$$

This can be further simplified as,

$$\ln(N) = \alpha P_{in} + \beta \quad (10)$$

where α and β represent the slope and the y-intercept of the line respectively. Thus, the RSSI circuit presents a linear characteristics of $\ln(N)$ with the input power (dBm). The simulation results presented in Fig. 9(b) confirm the analysis.

B. RSSI Protocol

According to 802.15.4 standard [17], the PHY layer of the radio must provide an estimate of the received signal power indicated by an integer value. The signal strength is generally observed between PCLP (Physical Layer Convergence Protocol) preamble and PLCP header.

Considering channel state estimation, the transmitter sends the packets, and the RSS sensor collects and monitors the RSSI value at a low data rate like 100 packets per second [11], [28]. The process of transmission, collection, and monitoring is repeated for different transmission powers accordingly.

In Fig. 9(c), simulation results of a simplified scenario of signal estimation are presented, wherein RSSI detection is

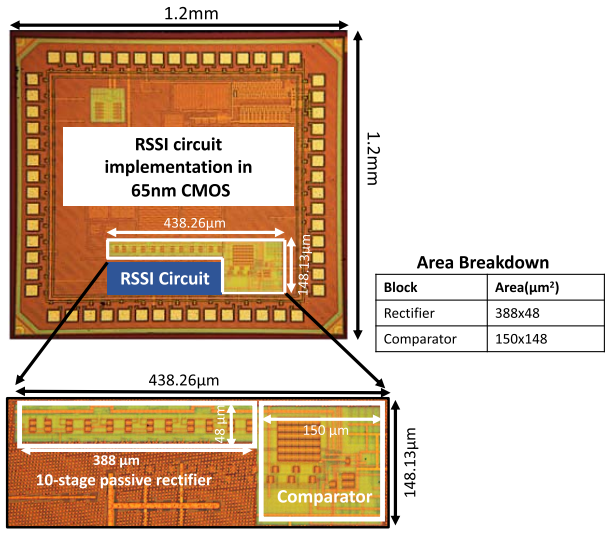

Fig. 11. Die Micrograph of the RSSI circuit implementation in 65-nm CMOS process.

performed during the preamble state of packet transmission at a transmit power of −20dBm using on-off keying (OOK) based modulation at 900MHz. Based on the magnitude of the incoming signal, the RSSI circuit generates a toggling pattern as the output, which is directly correlated with the signal strength. Based on the toggle value, the RSSI value can be reported directly in dBm.

Even though RSSI based detection is generally performed with low bit rates, the RSSI circuit supports a bit rate of 0.1kbps-100kbps, and hence can implement even a faster channel state estimation.

V. Measurement Results

A. Measurement Setup

The RSSI circuit is designed in a 65-nm CMOS process. Fig. 11 shows the die micrograph with an area breakdown of different blocks. The die is encapsulated in a Quad Flat No-Leads (QFN) package. This RSSI circuit is energy detection based and performs detection in amplitude modulation schemes like OOK, which is a more commonly used modulation to assess the link quality in applications like ULP wake up receivers (WRX) [29]. Measurements on the RSSI circuit were performed to characterize its sensitivity, dynamic range, noise performance, modulation speed, and power consumption. The measurement setup to characterize the performance of the RSSI circuit is presented in Fig. 12. RF signal source (*Tektronix TSG4106A*) was used to generate the incoming RF signal and noise signal (for noise measurements). Pattern generator (*Link instruments: IO3200*) was used to generate one-time calibration signals. For the noise measurements, power combiner (*ZFSC-2-2500-S+*) was used to combine the incoming RF signal and noise signal. RSSI test board was placed in a thermal chamber (*Tenney-TJR*) for temperature measurements.

The setup and results for these measurements are discussed below.

1) Sensitivity Measurements: To characterize the overall sensitivity of the proposed circuit, we measured the sensitivity of the RSSI circuit with an off-chip matching network [30].

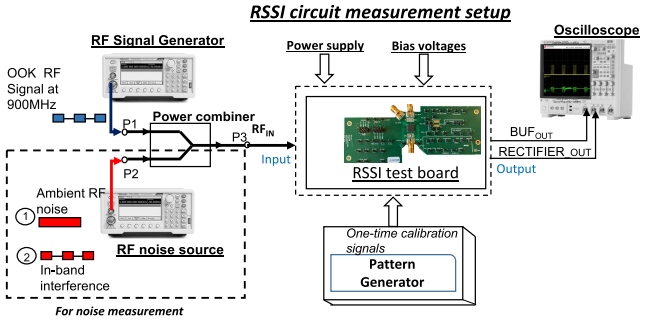

Fig. 12. Measurement setup to characterize sensitivity, dynamic range, power consumption, modulation speed and noise performance of the RSSI circuit.

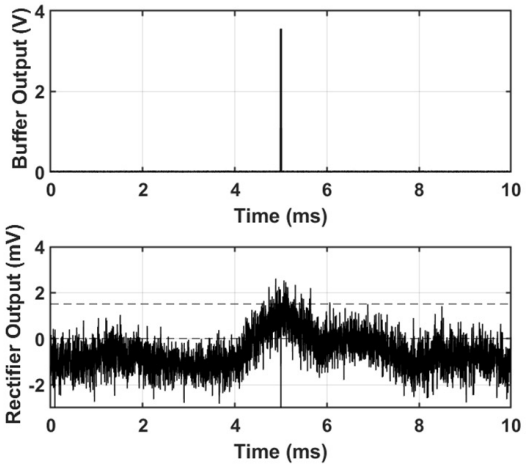

Fig. 13. Measurement result showing single toggle of the comparator when rectifier output charges to 1mV for −38dBm input power OOK modulated at 900MHz.

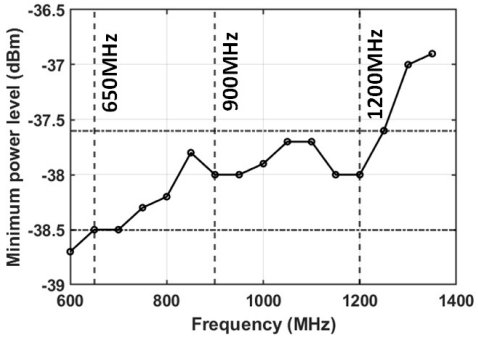

Fig. 14. Measurement of sensitivity of the RSSI circuit from 600MHz to 1.35GHz. The sensitivity of the circuit at 900MHz is −38dBm.

The off-chip matching network (co-design of antenna and MEMS resonator) provided a boost in the voltage gain by 17dB at 820MHz. The single toggle at the output results in a sensitivity of −55dBm at 820MHz with a OOK modulated signal at 0.1kbps (10% duty cycle). To further characterize the RSSI circuit at different frequencies and at different power, rest of the measurements were carried without the off-chip matching network.

Fig. 13 shows the basic measured transient output of the RSSI circuit. It shows a single toggle response to a slowly rising rectifier output with −38dBm input power, OOK modulated at 900MHz. The comparator toggles when the rectifier output reaches 1mV. This result also validates

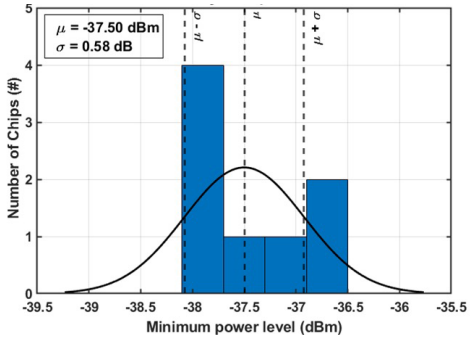

Fig. 15. Measurement of sensitivity of the RSSI circuit across 8-different chips.

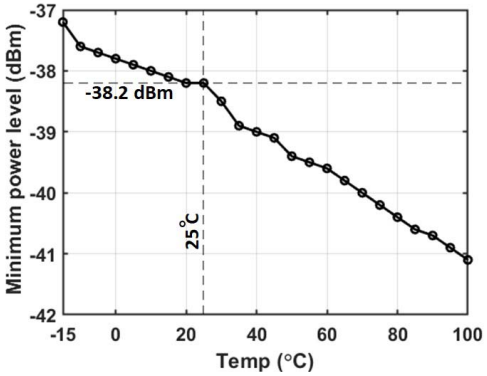

Fig. 16. Measurement results showing the sensitivity variation across a temperature range of −15° C to 100° C.

the offset-correction method used in the design. An uncompensated comparator would not respond to the 1mV input voltage due to inherent offset. Fig. 14 shows the sensitivity measurement result for a broad range of frequencies (600MHz-1.35GHz). The sensitivity of the RSSI circuit varies from −39dBm at 600MHz to −37dBm at 1.3GHz. The circuit achieves a sensitivity of −38dBm from 900MHz to 1.2GHz.

Sensitivity of the RSSI circuit across 8-different chips was also characterized. Fig. 15 shows this measurement. A mean (μ) sensitivity of −37.5dBm is achieved with a standard deviation (σ) of 0.58dB.

To characterize the variation of sensitivity with temperature, sensitivity of the circuit for a temperature range of −15° C to 100° C was measured. Fig. 16 shows the variation in the sensitivity across this temperature range. The sensitivity of the RSSI circuit is −38dBm at room temperature.

2) Dynamic Range Measurement: The measurement is done for a symbol duration of 10ms (at 10% duty cycle, i.e., high for 1ms) during which the toggle at the RSSI output is recorded and the measurement is repeated for different power levels at 900MHz. Although this RSSI circuit works for a broad frequency spectrum (Fig. 14), in Fig. 17(a) measurement results for the dynamic range at 900MHz [31], [32] are presented. The measurement data is plotted on the natural log scale ($\log_e$) represented as ln (N). From the measurement plot, the RSSI circuit has a dynamic range of 26dB with an accuracy of ±0.5dB.

Fig. 17(b) shows the comparison between the simulated and measured results for the dynamic range. The reported slope from the measurements matches with the simulated results and an error of ±0.5dB between the measurement and simulation results highlights the overall accuracy of the entire setup. The difference of 3dB between simulation and measurement is on account of the insertion loss which was not considered in the simulation setup.

Dynamic Range Enhancement To improve the dynamic range at higher input power, different techniques like capacitor attenuation array [7], [33], selective stage control of limiting amplifier [34], power selection control bits [35], multiple RSSI circuits [36] are generally used. It should be noted that the RSSI circuit is fully monolithic and no external off-chip components have been used for dynamic range extension. Off-chip components like capacitor attenuation array which effectively prevents saturation at higher input power levels, would prove advantageous in increasing the dynamic range.

3) Noise Resilience Measurements: Experiments were done to measure the noise performance of the RSSI circuit. Fig. 13 shows the ability of the comparator to detect a low signal at 1mV output voltage of the rectifier. It shows higher resilience to DC-offset and low frequency noise. The trip point of the comparator can be further raised by controlling the switching threshold of the programmable inverter (Fig. 5-a). Fig. 18 shows the measurement results of the RSSI output toggle with a 900MHz OOK signal sent at −38dBm input power. The 3-bit control signal B is used to control the inverter threshold (Fig. 7-b). B=<111>, which sets the lowest trip point for the comparator, shows 3 toggles at −38dBm. In all the measurements, B=<110> is used which sets the comparator threshold to 1mV shows a single toggle. B=<000> sets the highest threshold and no comparator toggling is seen at this power level.

The performance of the RSSI circuit in the presence of ambient RF noise and in-band blocker was also characterized. Fig. 19 presents the measurement results for the ambient noise and in-band blocker.

a) Ambient noise: In one experiment, a continuous wave (CW) in-band blocker was applied at 902MHz (2MHz offset) with its power varying from −30 to −10dBm. The input signal was OOK modulated signal at 900MHz. RSSI output toggle count was observed at −36dBm and −27dBm input power. In addition to this, out-of-band CW blockers were also applied at 800MHz and 1GHz. Fig. 19-(a) shows the measurement result for the CW blocker. In the presence of the CW blocker or ambient noise, the rectifier output settles to its corresponding DC voltage level. Thus, the RSSI circuit with the DC-offset correction only responds to the primary input signal and number of toggles remain same even in the presence of CW blocker or ambient noise. This feature of the RSSI circuit can have advantage in providing defense against constant jamming attacks [37].

b) In-band interference: For the in-band blocker, a 0.1kbps (10% duty cycle) OOK modulated in-band blocker was applied at 902MHz (2MHz offset) with a power level of −33dBm and varied the input power level from −55 to −13dBm. Fig. 19-(b) shows the measurement results. Three regions are highlighted to see the effect of in-band blocker on the number of output toggles.

For low input power level (<−38dBm), the toggling at the output is dominated by in-band blocker. This toggle count can be used to characterize the (OOK modulated) in-band blocker (*Blocker power characterization* in Fig. 19-(b)). At higher

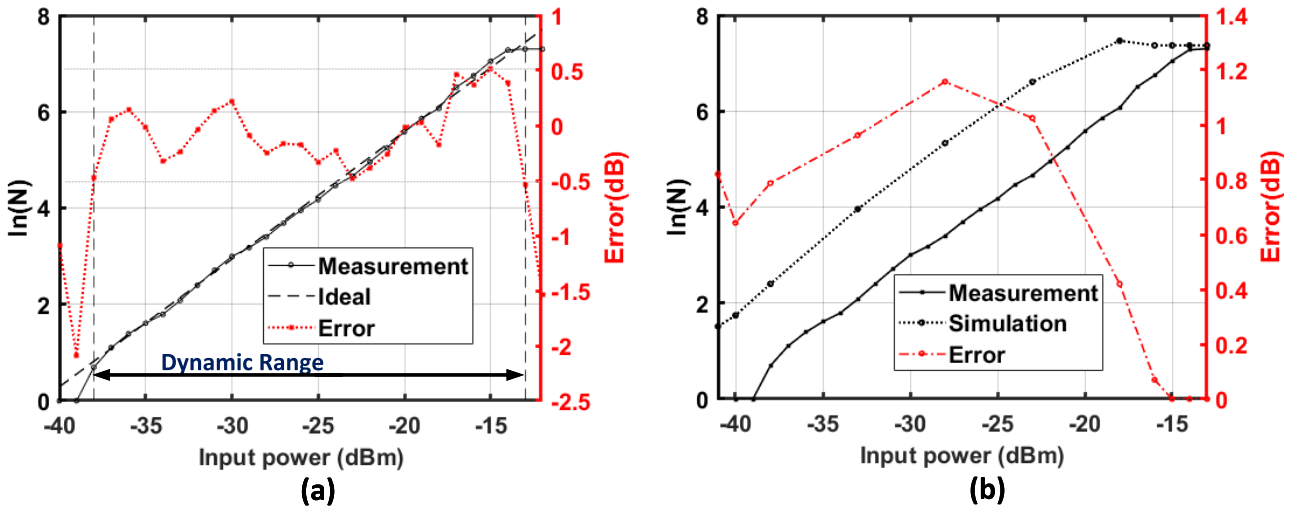

Fig. 17. (a) Measurement result of the dynamic range of the RSSI circuit. The RSSI circuit has a detection accuracy of ±0.5dB over a 26dB dynamic range (b) Comparison between the simulated and measurement result of the dynamic range of the RSSI circuit.

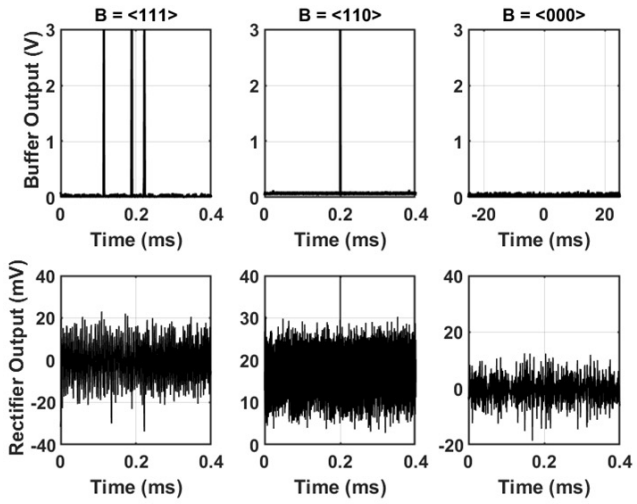

Fig. 18. Measurement results showing how programming of the inverter threshold controls the trip point of the comparator with input power at −38dBm at 900MHz. (a) B=<111> sets the minimum threshold for the comparator and results in multiple switching, (b) B=<110> sets the next higher threshold and consequently results in one toggle at −38dBm, and (c) B=<000> sets the highest threshold and no toggling is measured.

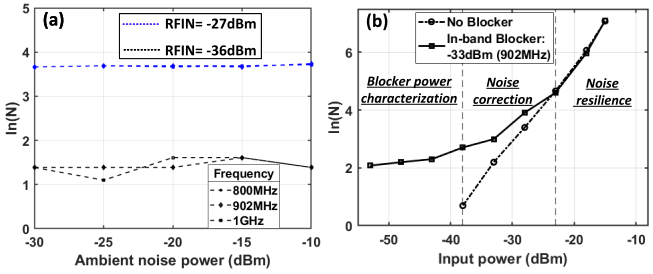

Fig. 19. Performance measurement of the RSSI circuit in the presence of ambient RF noise. (a) RSSI output measured for a 900MHz signal at −36dBm and −27dBm with a continuous wave in-band blocker at different power levels and at different frequencies, (b) RSSI output measured with OOK modulated −33dBm, 902 MHz in-band blocker.

input power levels, the output toggles represent the combined effect of the in-band blocker with the input signal. This deviation of the toggle count can be compensated from the *Blocker power characterization* mode which can be used to improve

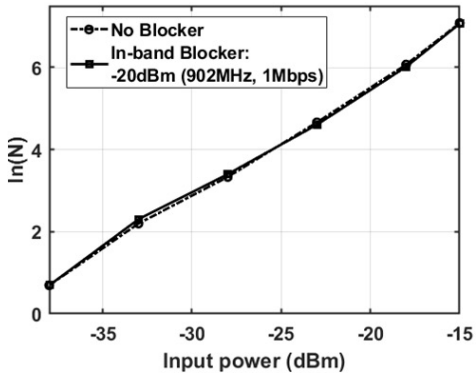

Fig. 20. Performance measurement of the RSSI circuit in the presence of in-band blocker of −20dBm at 902MHz OOK modulated at 1Mbps.

the accuracy of detection (*Noise correction* in Fig. 19-(b)). When the input power level is further increased, the number of toggles is dominated by the input power, minimizing the effect of in-band blocker in the detection accuracy (*Noise resilience* in Fig. 19-(b)).

The performance of the RSSI circuit in presence of an in-band blocker OOK modulated at high data rate was also measured. In Fig. 20, measurement results when a 1Mbps OOK modulated in-band blocker at 902MHz (2MHz offset) with a power level of −20dBm was applied and varied the input power level from −40 to −13dBm are presented. The number of toggles remain unaffected owing to the band-pass characteristics of the comparator in the RSSI circuit (Fig. 6(b)).

The effect of external interference noise is briefly discussed below:

c) Electrostatic discharge (ESD): In the this RSSI design, rectifier output is AC-coupled to the comparator. Any slow or fast transients will be attenuated by the band-pass response of the comparator Fig. 6(b). In addition to this, ESD protection circuits at RF_{IN} pad are used to suppress ESD effects.

d) Radiation-based noise: Electromagnetic radiation interference is more dominant at higher frequencies, particularly in the 2.4GHz band [38], [39]. The RSSI circuit with out-of-band blocker rejection feature will filter out these elec-

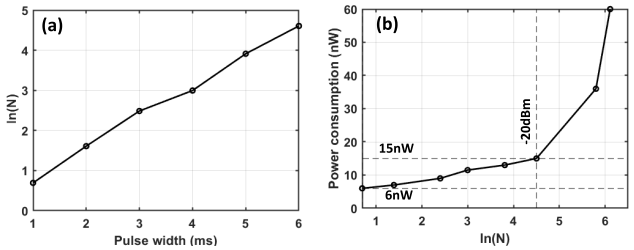

Fig. 21. (a) Measurement results showing the toggle count for different symbol pulse width with input RF signal at 900MHz and −37dBm power (b) Measurement results showing power consumption of the RSSI circuit for different number of output toggles. .

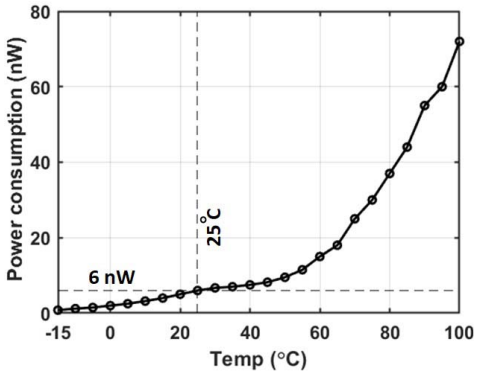

Fig. 22. Measurement results showing the variation in the power consumption across a temperature range of −15° C to 100° C for the minimum detectable power.

tromagnetic radiation interference which exist at frequencies above the range of interest.

4) Modulation Speed Measurement: The response of the circuit to different modulation speed was also measured. Fig. 21-(a) shows the measurement results of the output toggles for an input power of −37dBm input power at 900MHz OOK modulated at different modulation speeds. The modulation speed was varied by changing the pulse width from 1ms to 6ms over a 10ms time period. As expected, the toggle count increases with increase in the symbol duration (Eq.9)

5) Power Consumption Measurements: In Fig. 21-(b) measurement results for the power consumption of the RSSI circuit for different number of output toggles are presented. As the number of toggles increase, the overall power consumption increases on account of higher switching in the circuit. The circuit consumes 6nW for the minimum detectable power of −38dBm. For −20dBm input power, the RSSI circuit consumes 15nW power. The power consumption of the circuit across temperature variation for a OOK modulated signal at 900MHz when the circuit generates single toggle at the output was also measured. A proportional to absolute current reference (PTAT) was used to bias the comparator across the temperature range for a constant transconductance [40]. In Fig. 22, the measurement result of the power consumption across the range of temperature from −15° C to 100° C for the minimum detectable power are presented.

The power consumption varies with the input signal strength as higher strength signal generates more toggles and hence higher switching power. Within the dynamic range of detection (26dB), the power consumption varies from $6nW$ (−38dBm) to $90nW$ (−13dBm). This RSSI circuit consumes higher power only during the incoming RF signal. Considering IoT applications like link quality assessment, secure wireless communication, the RSSI circuit has to actively monitor the wireless link for signal detection. While the signal detection may happen in short pulses, in the absence of RF signal, the standby power of the RSSI circuit becomes dominant for continuous monitoring. The standby power of SDA-based RSSI design in few milli-watts may be prohibitively large considering IoT applications. However for this RSSI circuit, power goes down to a few nano-watts in the absence of RF signal.

B. Figure of Merit

Table III compares this work with some of the other reported works for RSSI circuit or ULP radios which include RSSI circuit. The measured sensitivity of this RSSI circuit is −38dBm at 900MHz. The sensitivity is further improved to −55dBm at 820MHz by using an off-chip matching network. This work reports the lowest power consumption of 6nW and a high detection accuracy ±0.5dB when compared to the other works. The active area of the RSSI circuit is 0.04 mm^2. It also reports the highest Figure of Merit (FOM) among other works where FOM defined as [44],

$$FOM(10^{12}) = \frac{10^{(DR/20)} \cdot f_{max}}{P}$$

where DR is the dynamic range, f_{max} is the maximum frequency of operation and P is the power consumption.

The ultra-low power consumption of the RSSI circuit with 26dB dynamic range can be useful in ULP IoT applications which include link quality monitoring [29], RF energy harvesting monitoring [45], backscatter communication [12], security against jamming attacks [37], among others.

C. Target Applications

The ultra low power consumption of this RSSI circuit (standby power of 6nW) with a dynamic range of 26dB and a sensitivity of −55dBm (when using off-chip matching network) is favourable for the following low power applications.

a) Link quality assessment: RSSI circuit is crucial to continuously monitor the link quality for wireless communication [13]. In [29], authors report a RSSI circuit with a dynamic range of 25dB to support RSSI and CCA for link quality measurements for ULP WRX. This RSSI circuit as a link quality indicator (LQI) tool with 6nW power consumption would reduce the power consumption of the entire ULP radio.

b) RF energy harvesting monitoring: In RF energy harvesting based systems, RSSI is deployed to monitor the strength of the incoming signal. In [45], RSSI circuit used to monitor the incoming RF signal for a RF-DC energy harvester. This RSSI circuit with ultra-low power consumption can be deployed as the monitoring systems for energy harvesters. It can potentially enable a simultaneous RF monitoring and storage of harvested energy otherwise prohibitive due to a high power consumption of the RSSI circuit [45].

c) Backscatter communication: Recently, backscatter communication as a replacement to conventional high power transceivers in the IoT systems, has been implemented in [12]. Transmitter-tag link is characterized with the RSSI circuit for a <40m communication range in an office environment with

TABLE III
COMPARISON OF THIS RSSI DESIGN WITH OTHER REPORTED WORKS ON RSSI CIRCUIT

Ref	TCAS-II'22 [18]	TMTT'21 [41]	ISSCC'21 [29]	IEEE Access'20 [42]	MWCL'19 [7]	TMTT'16 [35]	TCAS-I'15 [43]	TCAS-I'14 [3]	JSSC'12 [44]	This work
Technology	$65nm$	$180nm$	$65nm$	$65nm$	$0.18\mu m$	$28nm$	$65nm$	$0.18\mu m$	$0.18\mu m$	$65nm$
Supply Voltage	1	1.8	-	1.2	3.3	1.8	1.2	1.8	1.8	1
Dynamic Range(dB)	45	128.8	25	20	45	40	15	55	64	26
Power Consumption (mW)	$3.2\text{x}10^{-5}$	89.2	$3.2\text{x}10^{-3}$	2.04	0.78	11.8	0.96	4.68	$1.08\text{x}10^{-3}$	$0.6\text{x}10^{-5}$
f_{max}(GHz)	$1\text{x}10^{-6}$	0.87	2.4	5	5	4	0.108	-	$2\text{x}10^{-5}$	1.35
Number of stages	6	2	$2\text{x}16^{\oplus}$	1	7	4	3	6	1	$10^{\oplus}$
Accuracy (dB)	±1	-	±3	±0.5	±1	±0.8	±1.5	±1	<1	±0.5
Sensitivity(dBm)	-40	-18.6	-67.5	5	-10	-35	-40	-55	-61	**-55$^{\#}$ | -38***
Silicon Area (mm^2)	0.123	3.56	0.33	0.014	0.085	0.15	0.75	0.6	0.019	0.04
Bandwidth (GHz)	$1\text{x}10^{-6}$	0.4	-	2	4.6	3.3	0.02	0.03	$2\text{x}10^{-5}$	0.75
BW/Area (GHz/mm^2)	$8.13\text{x}10^{-6}$	0.11	-	142.86	54.12	22.02	0.03	0.05	$1.05\text{x}10^{-3}$	18.38
Measurement time (ms)	-	8.1	-	-	-	-	-	-	-	1
Energy/Conversion (J)	-	$7.23\text{x}10^{-4}$	-	-	-	-	-	-	-	$6\text{x}10^{-12}$
FOM (GHz/mW)	5.6	$2.69\text{x}10^{4}$	$1.33\text{x}10^{4}$	24.5	1140	33.9	0.6	-	29.3	**$4.5\text{x}10^{6}$**

$^{\oplus}$*Number of rectifier stages*, $^{\#}$*Measured at* $820MHz$ *using off-chip matching network*, **Measured at* $900MHz$ *without off-chip matching network*

25dB dynamic range. The dynamic range of the RSSI circuit (26dB) can meet range characterization in such backscatter communication based ULP IoT transceivers.

d) Secure wireless communication: In addition to the link quality assessment for low power radio, an enhanced security in the ULP IoT network has been gaining traction [46], [47]. Physical layer attacks like jamming attacks, energy depletion attacks can lead to a disruption in the communication leading to Denial of Service (DoS) in the IoT network [48]–[50]. RSSI circuit as a energy-detection based solution along with packet delivery ratio (PDR) have been used to detect such physical layer attacks [37]. In Fig. 19(a) measurement results demonstrating the resilience of this RSSI circuit to the in-band and out-of-band CW blockers are presented. In addition to this, the ability of this circuit to characterize the in-band OOK modulated blocker is presented in Fig. 19(b). RSSI circuit as an energy efficient *lightweight* solution can be used to detect and provide defense against such physical layer attacks like constant jammer, deceptive jammer among others.

VI. CONCLUSION

This paper presented an ultra-low power RSSI circuit implemented in a 65-nm CMOS process with a 1V supply. The novel technique of direct conversion of the RF signal to a digital code presents several advantages over the conventional successive detection architecture. The direct RF to digital code converter RSSI circuit consumes a power of 6nW and achieves a sensitivity of −55dBm (with off-chip matching network) and a dynamic range of 26dB. With noise and offset correction and digital implementation of the detection, an accuracy of ±0.5dB is achieved. The mathematical analysis of the toggling rate of the RSSI circuit is in strong agreement with the simulation and measurement results. Measurement results of the sensitivity of the RSSI circuit across a broad range of frequencies (600MHz to 1.35GHz), temperature range (−15° C to 100° C) and process variation were presented. The measurement results of the noise performance of the RSSI circuit under ambient noise and in-band blockers and the corrective measures to achieve noise resilience were also presented. The RSSI circuit also has the highest FOM among the other reported works for the RSSI-based detection. Finally, some target ULP IoT applications where this work can be advantageous were discussed.

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