30.4 A 3.7V-to-1kV Chip-Cascaded Switched-Capacitor Converter with Auxiliary Boost Achieving >96% Reactive Power Efficiency for Electrostatic Drive Applications

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This work presents a high voltage drive system for electrostatic and piezoelectric (PZT) actuators used for small-scale electromechanical applications, e.g. microrobotics and haptics. Such systems are notoriously challenging due to the need for extreme conversion ratios to reach 100s of volts to kV from system batteries, often with stringent size (<<1cm^3) and weight (<<1g) restrictions [1–3]. As typical electrostatic/PZT actuators require significant reactive power (CV^2f_{sw}) to drive a bulk dielectric medium, past work [3, 4] has shown a need to efficiently deliver and recover reactive energy to minimize system power loss, significantly improving on hard-switching drivers [1] or uni-directional boost circuits [2].

Shown in Fig. 30.4.1, this work implements a modular/scalable switched capacitor (SC) converter allowing nominally 16-stage reconfigurable series-parallel (SP) chips to be stacked in series voltage domains with low-voltage control signals relayed up the stack to operate as a single high-voltage driver. Each SP stage reconfigures the state of 15 off-chip flying capacitors sequentially from parallel to series, increasing V_{OUT} in integer steps of ~$V_{IN,SC}$ during actuator charge. While hard charging loss occurs in each step, overall it is reduced by ~N (the number of steps in the drive sequence) compared to conventional full-swing hard charging [1]. During the mirrored step-down process, the flying capacitors recharge and recover an ideal fraction (N-1)/N of reactive energy stored in the actuator. Due to predominantly reactive power flow, this can be described as a pseudo-resonant process [4], here we use metrics: (1) effective quality factor Q_X to capture reactive over real power loss and (2) reactive power efficiency η_x to quantify delivery and recovery of reactive power.

Compared to the related concept in [4], this work is the first to show modular multi-chip stacking which significantly improves scalability and *extends voltage conversion beyond the SOI buried-oxide BOX voltage limit* (here 400V) using only 5V and 32V-rated trench-isolated devices. Switching cell and chip-chip control uses only low-voltage level shifters and finite-state machine FSM logic, allowing a simple 1b+CLK differential input signal to control arbitrary high-voltage chip-stacks. Compared to [4] which used an unregulated 16-20V benchtop power supply, this design uses an integrated auxiliary boost converter to operate with low-voltage 3-3.7V battery inputs. The boost operates in discontinuous burst-mode operation with feedback to provide voltage regulation with low quiescent power. With typical output V_{OB}=$V_{IN,SC}$=20–30V (6 to 8× step up), the boost remains efficient with a physically small inductor. Quantitative improvements include >5× higher conversion ratio per chip (>15× for three chips stacked), >3× higher output power (up to 1.5W/chip), >10× higher switching frequency, and higher efficiency and quality factor than past work.

Figure 30.4.2 shows the chip stacking and daisy chain control process and circuitry. Four differential digital signals are processed through chip-boundary I/O: CLK (triggers FSM), UD (indicates whether in step up or down mode), SP (whether the next cell is in series or parallel) and MC (whether the current chip is connected to the load). At the chip input, only UD and CLK are needed to control switching. At initial step-up, all parallel (blue) switches are on (V_{OUT} = 0V); signals UD and CLK are forwarded up the stack. With UD=1, when the CLK edge propagates to the last parallel cell in the stack, it switches to series (red switch on); this cell sets SP=1 which is passed to the previous cell. At the next CLK edge, the previous cell switches to series; thus with UD=1, at each CLK edge the parallel-series state transition ripples down from last cell to first cell. During step down (UD=0), UD and CLK only pass through parallel cells. Thus, at CLK events, the series-parallel transition ripples up from first cell to last cell. The interface cell (Fig. 30.4.1) is only used in the last chip to connect to the load; for other chips it is bypassed/unused. To inform chips of their position in the stack, signal MC is hardwired (PCB jumper to V_{REGN} or V_N of the last cell in middle and last chips respectively).

Figure 30.4.3 shows local circuitry within each switching cell including FSM logic, local level shifters, gate drivers, power switches, and a local linear regulator (LDO). The LDO is needed for low-side and high-side supplies V_{REGN} (~4V above V_N) and V_{REGP} (~4V below V_P). It uses a MOS-degenerated 5V depletion device to form a pseudo-PTAT current reference (~250nA); when passed through a weak inversion diode MOS stack, it forms a pseudo-bandgap reference for the class-B LDO output. A 32V depletion cascode shields the reference from $V_{IN,SC}$ = V_P –V_N, nominally 20V to 30V. A power OK (POK) circuit generates logical FSM reset and monitors the $V_{IN,SC}$ voltage level (resetting FSM state to parallel if low voltage detected). Measurement shows POK triggers when $V_{IN,SC}$ reaches ~6V; a 500mV hysteresis window prevents POK chatter. Level shifters use a floating latch with 32V cascodes to block voltage domain differences. A NAND-latch is used to lock state and reject common mode transients (charge on parasitic BOX cap C_{tub}) during step up/down. High-side PMOS $M_{APa,b}$ is pulse-triggered during switching to accelerate latching (charge C_{tub} and other parasitics). Chip-boundary level shifters are differential latching to overcome V_{REGN} mismatch across chips and use logical blanking to reject common mode errors.

Figure 30.4.4 shows time-domain measurements for a scenario with 3 chips cascaded, operating with the auxiliary boost for 3.7V-to-1kV conversion. The boost runs in discontinuous conduction mode (DCM) with hysteretic burst-mode control. When the boost output voltage V_{OB} is below a provided reference, it switches with fixed duty cycle and frequency of 1MHz (constant peak inductor current ~30mA). This provides charge and increases voltage $V_{IN,SC,1}$ of the first chip in the stack. When the SC stage is stepping up, providing charge to the load, $V_{IN,SC,1}$ decreases, thus the boost converter mainly operates during step up. When boost output V_{OB} reaches the reference + hysteresis, it stops switching (standby mode). During step-down, charge from the dominantly capacitive load is recovered (to the flying capacitors) such that the boost remains idle. Energy recovery in the SC stage can be seen in that during step down, flying capacitor voltage(s) are increasing. More energy is transferred and recovered in capacitors close to the load as seen in their larger voltage swing. Peak efficiency η_{boost} is ~89% and is above 80% for most of the useful range. However, boost efficiency only marginally impacts overall converter metrics due to the benefit of the associated SC stage. For example it can be shown that $Q_{X,tot} = Q_{X,SC} \cdot \eta_{boost}$, which leads to only a modest impact on efficiency $\eta_{X,tot}$ as long as $Q_{X,SC} \propto$#steps, N is high. Effectiveness of the daisy-chain relay is also highlighted in Fig. 30.4.4 which shows measured CLK signals as they are propagated across three stacked chips. At the rising/falling edge, total propagation delay through 16 cells from Chip 1 to 2 and 2 to 3 is roughly 60ns. This includes 16 level shifters and FSM logic blocks per chip, indicating fast switching of the daisy-chain-relay.

Figure 30.4.5 shows measured $V_{OUT,PP}$ versus $V_{IN,SC}$ for both single chip and 3-chip cascaded operation when driving calibrated class-I COG capacitor loads from 20pF to 15nF. The foundry-defined BOX and MOSFET voltage rating (400V/chip and 32V resp.) and measured breakdown limits (550V/chip and 40V resp.) are shown to highlight the reasonable operating range. Note that while the converter was able to drive output voltage exceeding the rated BOX and device limits without measurable leakage at room temperature (>500V for single chip and >1.5kV for 3-stacked), here we only quote performance up to rated limits. For detailed testing and characterization, respective derated limits of 300V and 1kV were used, regulated with $V_{IN,SC}$ or V_{OB}, while switching frequency was swept to adjust output power. Reliable switching frequencies extended well over 30kHz for single chip and 10kHz for 3-chip operation (depending on load cap and fast-switching limit FSL). Driving C_L = 2nF, the single-chip SC with aux. boost achieves Q_X ~12 or efficiency η_X = 92.3% at roughly 1W reactive power. At peak power of ~1.5W, it achieves η_X ~ 91%. With 3-chips cascaded, C_L = 2nF, roughly 1W, the SC with aux. boost achieves Q_X = 31.8 ($\eta_{X,peak}$ = 96.9%). At peak power of ~4.5W it achieves η_X ~ 96%. Efficiencies are higher with 3-stages as the SC is providing and recycling a larger fraction of energy.

Figure 30.4.7 shows a die photo and component breakdown. Total die area is 1.7mm^2 including 15 switching cells, interface cell, aux. boost (used only on first chip), I/O and ESD. Figure 30.4.6 provides a comparison table. This work achieves higher performance metrics Q_X and η_X than past work. Importantly, for an efficient pseudo-resonant design, it achieves VCR = V_{OUT}/V_{IN} > 80 per chip, with highest output power and switching frequency. While additional components are needed (higher volume) for the boost stage, compared to [4] this work achieves ~2 to 3× higher volumetric and gravimetric power density. Importantly, the design provides a modular/scalable pathway to achieve high drive voltages efficiently for a variety of electrostatic/PZT actuator devices.

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This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) under award number HR001119C0040 and the National Science Foundation (NSF) award number 2216552.

References:

[1] J. S. Rentmeister et al., "A 120–330V, Sub-µA, 4-Channel Driver for Microrobotic Actuators with Wireless-Optical Power Delivery and over 99% Current Efficiency," *IEEE Symp. VLSI Circuits*, pp. 1–2, Jun. 2020.
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[3] S. Chaput et al., "21.5 A 3-to-5V input 100Vpp output 57.7mW 0.42% THD+N highly integrated piezoelectric actuator driver," *ISSCC*, pp. 360–361, Feb. 2017/.
[4] Y. Li et al., "33.8 A Decentralized Daisy-Chain-Controlled Switched-Capacitor Driver for Microrobotic Actuators with 10× Power-Reduction Factor and Over 300V Drive Voltage," *ISSCC*, pp. 474–476, Feb. 2021.

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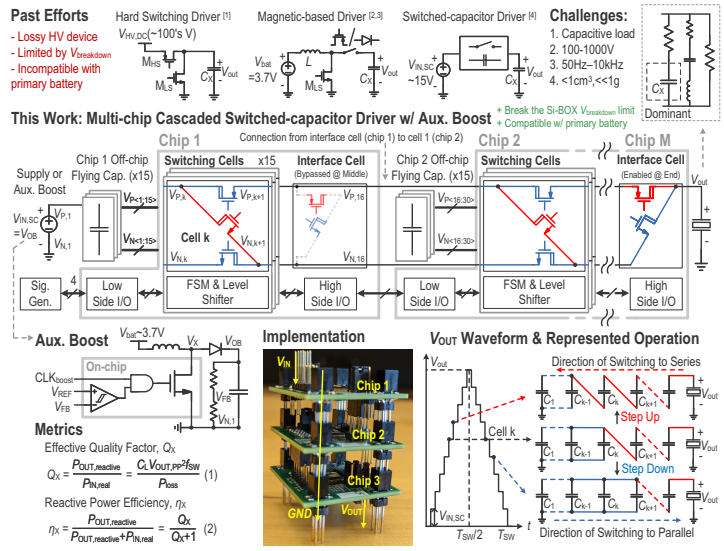


Figure 30.4.1: High level architecture and application background.

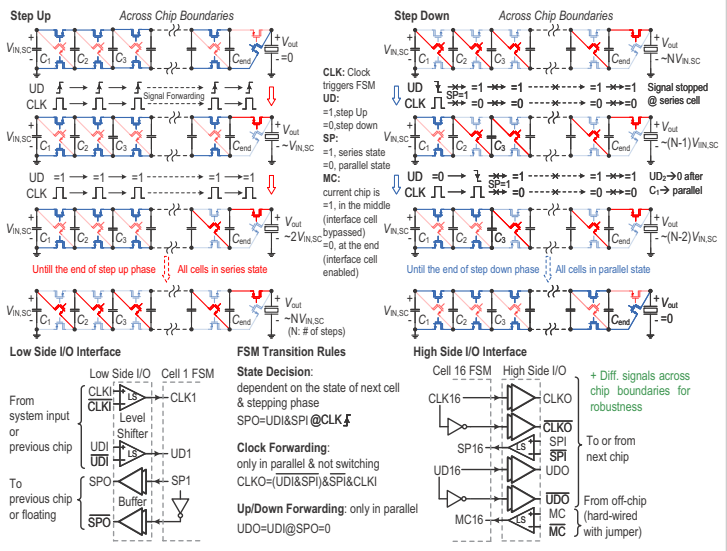


Figure 30.4.2: Converter operation, finite state machine and chip I/O interface.

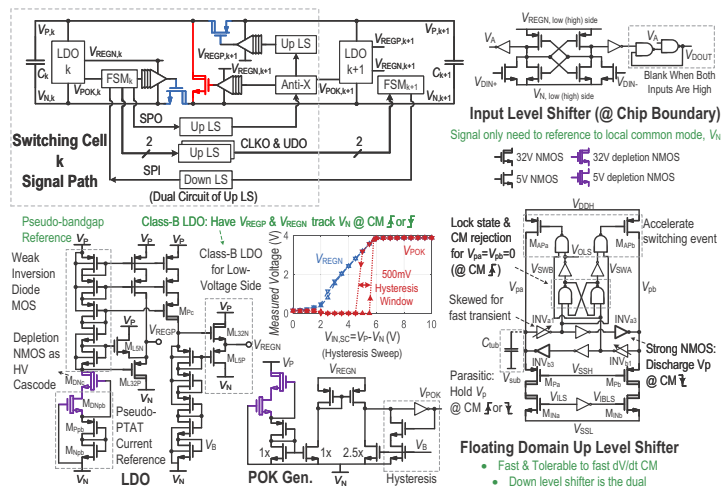


Figure 30.4.3: Key circuit blocks including switching cell, LDO, and level shifters.

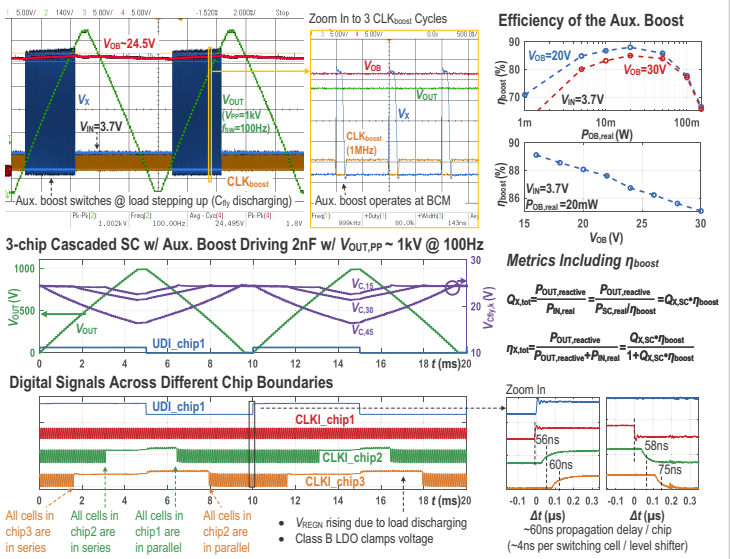


Figure 30.4.4: Measured time domain waveforms @1kVpp output and boost converter efficiency.

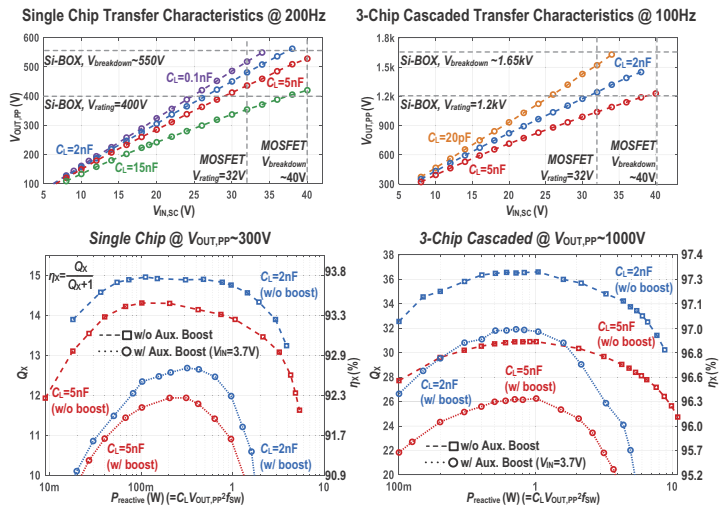
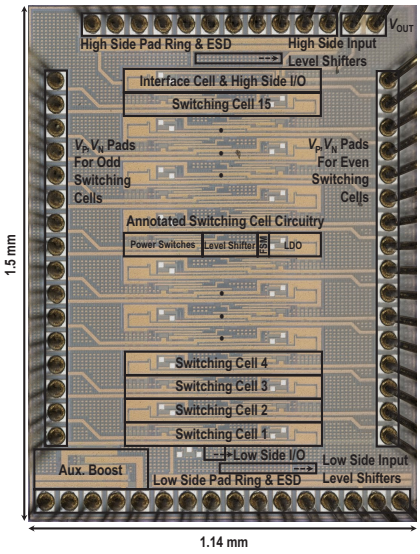


Figure 30.4.5: Measured peak-to-peak output voltage compared to rated and breakdown limits; effective quality factor and reactive power efficiency.

	Rentmeister VLSI20 [1]	Park ECCE [2]	Chaput ISSCC17 [3]	Li ISSCC21 [4]	This work	
Topology	Hard Switching	Unidirectional Boost	Bidirectional buck-boost	Switched Capacitor (SC)	Single chip SC w/ Aux. Boost	3-chip cascaded SC w/ Aux. Boost
Process	1μm SOI BCD	Discrete	0.18μm HV SOI	1μm SOI BCD	0.18μm SOI BCD	
V_{IN} (V)	310	3.7	3.6	16 - 20	3.7	3.7
$V_{OUT,PP,max}$ (V)	310	2700	100	300	300	1000
VCR	1	730	27.8	15	80	270
C_L (nF)	0.04 - 1	N/A(2)	100 – 330	0.1 - 10	0.1 - 15	0.02 - 5
$f_{SW,max}$ (kHz)	1	0.04	0.2	1	>30	>10
Passive components	1206 cap	1:11 Transformer + 4.7μF + 0603 cap x10 + 0201 cap x109	100μH + 10nF	0402 cap x16	100μH + 27μF(5) + 0402 cap x16	100μH + 27μF(4) + 0402 cap x48
Weight(1) (mg)	38	178.6(3)	105.7(3)	49.6	76	175
Volume(1) (mm^3)	8.5	35.5(3)	29.1(3)	9.4	15	35
$P_{OUT,max}$ (mW)	80	162(2)	495	400	1500	4500
Power Density (mW/mg) (1)	2.1	0.9(2)	4.7(2)	8.1	19.7	25.7
Power Density (mW/mm^3) (1)	9.4	4.6(2)	17.0	42.6	100	130
$\eta_{X,peak}$ (%)	49.8	34(2)	83.7	91.2	92.7	96.9
$Q_{X,peak}$	0.99	N/A(2)	5.1	10.3	12.7	31.8

(1) Metrics are based on passive component weight & volume only (chip weight/volume is generally negligible, PCB package/assembly size is difficult to quantify and depends on PCB/assembly technology, therefore misleading to compare)
(2) Design in [2] was tested with a resistive (40MΩ) load; thus reactive power metrics are not applicable; real power & efficiency are reported here.
(3) Does not include size/weight of active components and/or bypass capacitors (although these may be significant)
(4) Derated to 3.7V

Figure 30.4.6: Performance summary and comparison to prior art.



Process		0.18µm SOI BCD
Active Devices	Power Switches	32V NMOS 32V PMOS
	Reference Gen. Devices	32V depletion NMOS 5V depletion NMOS
	Digital Core	5V NMOS 5V PMOS
	Off-chip Diode	BAS40L-G3-08
Passive Devices	Off-chip Flying Capacitors	GRM155R61E225KE11D (0402, 207nF[1])
	Off-chip Inductor	XPL2010-104ML (100µH, 8.5Ω, I_{sat}=180mA)
	Off-chip Bypass Capacitor	06036D476MAT2A (0603, 27µF[2])
	Off-chip Resistors	300 kΩ (0402) + 3 MΩ (0402)
Die area	Total Area	1.7 mm^2
	Used Area [3]	1.2 mm^2

(1) Derated to 25V
(2) Derated to 3.7V
(3) Design is pad limited; some die area unused

Figure 30.4.7: Annotated die photo and implementation breakdown.

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