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ABSTRACT

Understanding the thermal stability and degradation mechanism of β-Ga_2O_3 metal-oxide-semiconductor field-effect transistors (MOSFETs) is crucial for their high-power electronics applications. This work examines the high temperature performance of the junctionless lateral β-Ga_2O_3 FinFET grown on a native β-Ga_2O_3 substrate, fabricated by metal-assisted chemical etching with Al_2O_3 gate oxide and Ti/Au gate metal. The thermal exposure effect on threshold voltage (V_{th}), subthreshold swing (*SS*), hysteresis, and specific on-resistance ($R_{on,sp}$), as a function of temperature up to 298 °C, is measured and analyzed. *SS* and $R_{on,sp}$ increased with increasing temperatures, similar to the planar MOSFETs, while a more severe negative shift of V_{th} was observed for the high aspect-ratio FinFETs here. Despite employing a much thicker epilayer (~2 μm) for the channel, the high temperature performance of I_{on}/I_{off} ratios and *SS* of the FinFET in this work remains comparable to that of the planar β-Ga_2O_3 MOSFETs reported using epilayers ~10–30× thinner. This work paves the way for further investigation into the stability and promise of β-Ga_2O_3 FinFETs compared to their planar counterparts.

High temperature power electronic devices have a wide range of applications in automotive electronics, industrial control, and oil/gas extraction. For instance, one notable application of high temperature high voltage electronics is in the electric charging system, which is essential for all-electric vehicles. Additionally, sensors utilized in aerospace under extreme environments require the understanding and control of their behaviors under high temperatures. However, conventional Si-based devices cannot work for the above-200 °C regime due to its intrinsic limitation of their electronic properties. Therefore, wide bandgap (WBG) materials, such as SiC and GaN, have been actively investigated for applications in next-generation high power high temperature electronics. The emergence of β-Ga_2O_3, an ultra-wide bandgap (~4.8 eV) semiconductor material with an extremely high Baliga's figure of merit (FOM) compared to SiC/GaN, provides yet another highly promising platform.[1,2] Various high performance β-Ga_2O_3 devices have already been demonstrated, including Schottky barrier diodes (SBDs), metal-oxide-semiconductor field-effect transistors (MOSFETs), and metal-semiconductor field-effect transistors (MESFETs).[2] As a high temperature operation is essential for power electronics, studies have been conducted to explore the thermal effects associated with β-Ga_2O_3 based devices.[3–7] The β-Ga_2O_3 epilayers can be bonded to alternative substrates that have superior thermal conductivity, such as SiC, by thermal thinning and annealing, achieving a relatively low thermal boundary resistance.[8] Consequently, the thermal impact on the β-Ga_2O_3 MOSFETs was mitigated,[7] leading to the reduction of I_{ds} and on-resistance (R_{on}) degradation at elevated temperatures up to 200 °C. However, the high temperature operation of homoepitaxial β-Ga_2O_3 transistors, which is more favorable for mass production considering the availability of native substrates, poses a challenge due to the inherently low thermal conductivity of β-Ga_2O_3.[9,10] Therefore, it is imperative to investigate the degradation behavior and mechanism of homoepitaxial β-Ga_2O_3 transistors.

Among all the unipolar β-Ga_2O_3 MOSFETs, the FinFETs are among the most promising structures for lower specific on-resistance

($R_{on,sp}$), less power consumption.[11–13] The improved gate control can be achieved in the FinFET structure due to the unique three-dimensional architecture. Chatterjee *et al.* investigated the thermal effect of vertical FinFET by conducting the infrared radiation imaging and simulation.[14] However, the high-temperature electrical performance of β-Ga_2O_3 FinFETs remains relatively unexplored. In particular, the hysteresis effect, typically ranging from 0.2 to 2 V at room temperature (RT) in β-Ga_2O_3 FinFETs fabricated using conventional reactive ion etching (RIE), has not been sufficiently characterized under high-temperature operations.[11,13] Metal-assisted chemical etching (MacEtch) is a plasma-free anisotropic etching method that avoids high-energy ion induced damage in semiconductor device fabrication.[15,16] We have recently demonstrated the achievement of near-zero hysteresis β-Ga_2O_3 FinFETs by substituting the conventional dry etch with MacEtch in the fin fabrication process.[17] Remarkably, the hysteresis of the MacEtch-fabricated β-Ga_2O_3 FinFETs was suppressed to a mere 9.7 mV under room temperature operation, which is in stark contrast to that of the β-Ga_2O_3 transistors fabricated using the RIE process. In this work, we present the high temperature (up to ~300 °C) performance of the MacEtch-formed β-Ga_2O_3 FinFETs with Al_2O_3 gate oxide and Ti/Au gate metal. We examine the thermal modulation of several critical parameters, such as the V_{th}, hysteresis, $R_{on,sp}$, and *SS* at high temperatures for the β-Ga_2O_3 FinFETs.

Figures 1(a) and 1(b) show the SEM image of a representative β-Ga_2O_3 single-Fin MOSFET and the cross section schematic view, respectively. The detailed fabrication process was reported previously.[17] Briefly, a 2 μm-thick (Si: 4×10^{17} cm^{-3}) β-Ga_2O_3 film was grown on a (010) Fe-doped semi-insulating substrate by metalorganic chemical vapor deposition (MOCVD).[18] Fin-shaped channel and source/drain regions were then defined by MacEtching using a Pt catalyst film with a mixture of HF and $K_2S_2O_8$ under illumination.[19–21] The active Si-doped (4×10^{17} cm^{-3}) n-channel fin is ~200/600 nm in top/bottom width, with a tapered sidewall, while the fin height is ~1.5 μm.[17] These geometry parameters were chosen to achieve high aspect ratio fin structure and effective channel depletion simultaneously. During the channel formation, photo-stimulated local electrochemical MacEtch (anisotropic) and wet chemical etch (isotropic or crystal orientation dependent) can take place simultaneously. The tapered sidewall profile is a result of parasitic wet etch, which reduces the top width more than the bottom because of the exposure time to the etchant. The relatively smaller fin-height and the tapered sidewalls in the β-Ga_2O_3 FinFET by MacEtch are due to the lateral etching, as indicated previously. The lateral etching could be suppressed by utilizing a UV light source with higher intensity in the MacEtch process. 20 nm ALD-grown Al_2O_3 and 25 nm/20 nm Ti/Au metal stacks were then deposited to form the gate (1 μm gate length). The distance

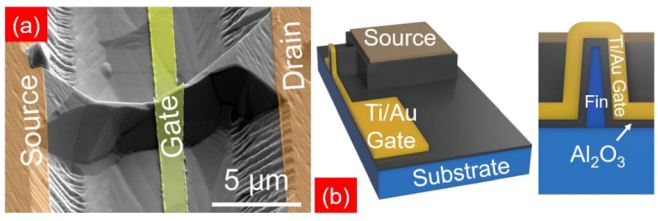

FIG. 1. (a) SEM image of the MacEtched FinFET structure. (b) The cross section schematics of the channel region of the as-fabricated FinFET device.

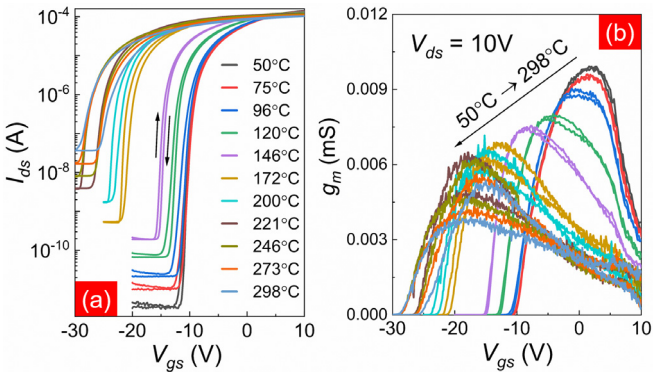

FIG. 2. (a) Log-scale transfer characteristics and (b) g_m of β-Ga_2O3 FinFETs under a variety of temperature ranging from 50 to 298 °C by upward and downward scans.

between source and drain is 5 μm. The electrical characteristics of the β-Ga_2O_3 FinFETs were measured in vacuum using a test station (MicroXact, Inc.) incorporated with a B1500A semiconductor device parameter analyzer (Keysight Technologies, Inc.). The measuring temperatures range from 50 to 298 °C with an approximate step of 25 °C. The temperature-stabilizing time for each measurement was approximately 20 min.

Figures 2(a) and 2(b) show the measured transfer, I_d–V_g, on log scale; and the corresponding transconductance (g_m) curves (linear scale) of a representative β-Ga_2O_3 FinFET device under a 10 V drain bias, as a function of temperature, with V_{gs} swept upward (negative to positive voltage) and downward sweep (positive to negative), as indicated by the arrows. The off-state current increases gradually with the rising temperatures from 4.3×10^{-12} (50 °C) to 3.7×10^{-8} (298 °C) A, which can be attributed to the thermionic emission of carriers from the source to drain. Note that the room temperature performance of the MacEtched β-Ga_2O_3 FinFET can be found in our previous report.[17] The g_m peak decreases by ~63% from 0.01 to 0.0037 mS over the entire temperature range studied, indicating the mobility degradation under high temperatures due to the phonon scattering. In addition, the corresponding voltages for the g_m peaks at different

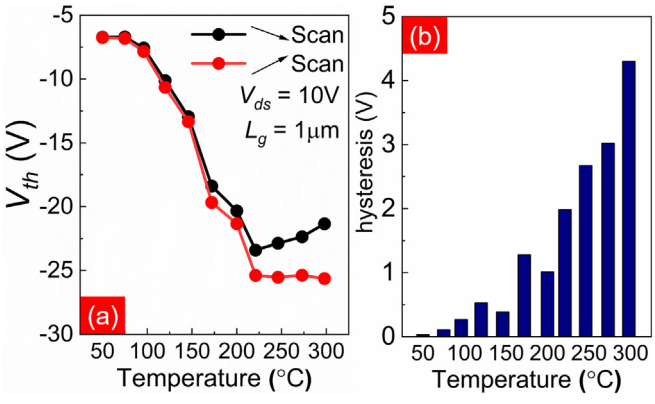

FIG. 3. The (a) extracted V_{th} (upward and downward scans) and (b) corresponding hysteresis of β-Ga_2O_3 FinFETs at the temperature range from 50 to 298 °C.

TABLE I. Material and geometry parameters of the planar β-Ga_2O_3 MOSFETs in Refs. 3–5 and the lateral β-Ga_2O_3 FinFETs in this work.

	T_{ch} (μm)	N_{ch}	S-D region	V_{ds} (V)	L_g (μm)	L_{SD} (μm)	W_g (μm)
FET 1 (Ref. 3)	0.3	Sn: 7×10^{17} cm^{-3}	Si-implant	25	2	25	500
FET 2 (Ref. 4)	0.3	Si: 3×10^{17} cm^{-3}	Si-implant	30	2	15	200
FET 3 (Ref. 5)	0.065	Si: 2×10^{12} cm^{-2}	Junction-less	5	0.7	7.5	150
This work	~1.5	Si: 4×10^{17} cm^{-3}	Junction-less	10	1	5	3.2 (Fin)

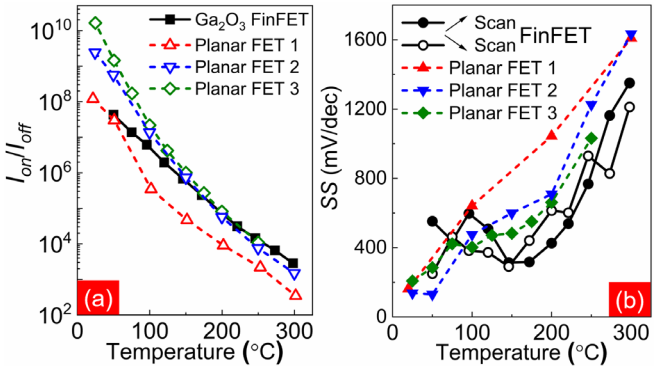

FIG. 4. The (a) I_{on}/I_{off} ratio and (b) *SS* of the β-Ga_2O_3 FinFETs in this work in comparison with the planar β-Ga_2O_3 MOSFETs reported in Ref. 3 (Planar FET 1), Ref. 4 (Planar FET 2), and Ref. 5 (Planar FET 3).

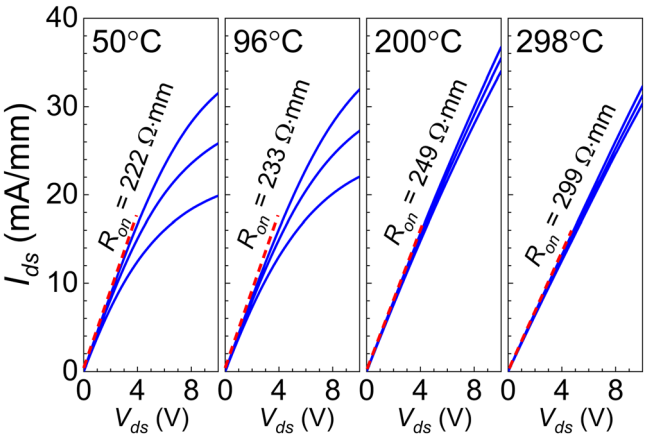

FIG. 5. The output curves of the β-Ga_2O_3 FinFETs (V_{gs} = 0, 2, 4 V) at 50, 96, 200, and 298 °C.

temperatures change dramatically with increasing temperatures, suggesting the shift of the V_{th}.

As shown in Fig. 3(a), the extracted V_{th} from the transfer curves shows a total shift of ~20 V in this temperature range. The shift is relatively small up to ~100 °C, but, slopes down dramatically before leveling off starting at ~220 °C. The negative shift of V_{th} can be attributed to the trapping/de-trapping of Al_2O_3/β-Ga_2O_3 and gate/Al_2O_3 interfaces,[22] which have been observed in the planar devices as well. It should be noted that the V_{th} thermal modulation is more pronounced in the fin-shaped junctionless structure studied here compared to planar β-Ga_2O_3 MOSFETs.[3,5] This can likely be attributed to the increased thermal effect in the fin channels, which result from higher local current densities.[14] A significant shift V_{th} can be observed from 146 to 172 °C, which can be attributed to the activation of deep traps within this specific temperature range.[23,24] This activation leads to an increase in channel conductivity and consequently raises the threshold voltage required. Note that the energy level and density of the deep traps are related to the growth method and conditions and can change as a function of thickness. It is well known that the thicker the epitaxial film is, the rougher the surface becomes, because of the accumulation of defects. In this work, a much thicker epilayer (~2 μm) was employed as the channel material compared to that (65 ~300 nm) in typical planar β-Ga_2O_3 MOSFETs.[3–5] Therefore, it is important to continue optimizing the growth conditions to achieve low defect density thick β-Ga_2O_3 for high aspect-ratio FinFET operation under high temperatures.

Concurrently, the hysteresis of the I–V measurements of β-Ga_2O_3 FinFETs [Fig. 3(b)], which was suppressed to as low as 9.7 mV at room temperature[17] as a result of the damage-free MacEtch fin formation process, clearly shows deteriorated performance at high temperature. At 50 °C, the hysteresis reaches 0.03 V, which is much lower compared to the RIE fabricated β-Ga_2O_3 transistors. However, the hysteresis increased significantly to 4.29 V at 298 °C. It was reported that deep traps in β-Ga_2O_3 associated with oxygen vacancies (V_O) and V_{Ga}-H complexes could be activated, in the temperature range (50–298 °C, or 313–571 K) examined in this study.[23–26] Those two types of deep level traps have been detected by current deep level transient spectroscopy (CLDTS) for exfoliated Ga_2O_3 thin-film transistors at similar temperature range.[27] These traps, which can be activated as temperature increases, could be captured/released during upward/downward scans, causing the hysteresis degradation when the device is heated.[22,28] Additionally, the body traps in the dielectric layer as well as the possible gate metal (Ti/Au) diffusion could be activated at high temperatures, contributing to the hysteresis degradation.[29]

I_{on}/I_{off} and *SS* temperature dependence are compared with three planar β-Ga_2O_3 MOSFETs reported in Refs. 3–5, all of which used Al_2O_3 gate dielectric. Table I summarizes the material and geometry parameters of these three devices. As shown in Fig. 4(a), the I_{on}/I_{off} ratio of the β-Ga_2O_3 FinFET degrades from ~5×10^8 to ~10^3 with increasing temperature in this range, which can be attributed to the enhanced thermionic emission of carriers across the potential barrier at the off-state.[6] The high temperature I_{on}/I_{off} ratio of the FinFET in this work exhibits a similar trend with other reported planar ones, and a slightly weaker degradation is found in the 50–150 °C regimes. As

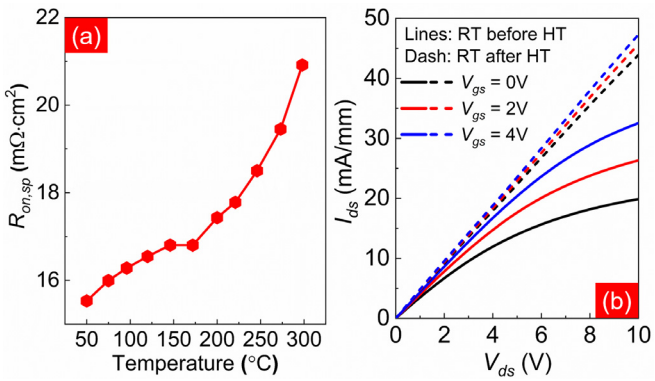

FIG. 6. (a) $R_{on,sp}$ of β-Ga_2O_3 FinFETs measured under different temperatures (50–298 °C), extracted from $V_{gs} = 4$ V in the output curves. (b) I_d–V_d characteristics of β-Ga_2O_3 FinFETs with V_{gs} from 0 to 4 V measured under room temperature before heating up to high temperature, and after a 12-h cooldown process.

illustrated in Fig. 4(b), the *SS* characteristics are increased considerably from ~120 mV/dec at room temperature to 1212 and 1351 mV/dec at ~298 °C for the upward and downward scans, respectively. The *SS* degradation suggests a severe thermal impact on the interfacial trap density, which was maintained at a low level under room temperature according to the C–V analysis.[21] Even with the large differences in device geometry, the general temperature dependence trend and magnitude of the FinFET studied here is comparable to the planar counterparts for this temperature range.

Figure 5 depicts the output curves of the β-Ga_2O_3 FinFETs with V_{gs} ranging from 0 to 4 V at temperatures of 50, 96, 200, and 298 °C. The extracted R_{on} values at V_{gs} of 4 V, which increase from 222 to 299 Ω·mm as the temperature increases from 50 to 298 °C, are labeled. The significant changes in the gate override (V_{gs}–V_{th}) observed in the output curves at different temperatures are a result of the V_{th} vs temperature profiles described earlier [Fig. 3(a)].

Figure 6(a) plots the $R_{on,sp}$ for the β-Ga_2O_3 FinFETs as a function of temperature. The $R_{on,sp}$ is defined as R_{on} (extracted at $V_{gs} = 4$ V) × W_g × (L_{SD} + 2L_T), where W_g, L_{SD}, and L_T are the gate width (3.2 μm), source–drain distance (5 μm), and transfer length (1 μm), respectively. The $R_{on,sp}$ remained relatively stable from 15.5 to 16.8 mΩ·cm² for 50 to 146 °C, similar to the room temperature $R_{on,sp}$. In contrast, the $R_{on,sp}$ increases relatively faster in the above ~150 °C regime. The nonlinear degradation $R_{on,sp}$ as temperature rises is mainly associated with the mobility reduction as a result of increased phonon scattering.[30,31] Future efforts with samples consisting of different doping levels and defect densities, as well as fin geometries, are required to understand the detailed mechanism and identify the degradation channels accurately.

To characterize the extent of permanent thermal damage, the electrical characteristics of the MacEtched β-Ga_2O_3 FinFETs were re-measured under room temperature after cooling down. We employed a cooling period of approximately 12 h, which is consistent with reported temperature-dependent studies on transistors.[6,32,33] As shown in Fig. 6(b), a noticeable difference can be seen in I_d–V_d curves obtained before and after subjecting the device to high temperature measurement and subsequent cooling. After cooling, the FinFET exhibited a significantly higher drain current, which can be attributed to a more pronounced gate override compared to that observed prior to the high temperature measurement, suggesting an irreversible impact on the performance of the β-Ga_2O_3 FinFET. Remarkably, the drain current following cooling exceeded that of 298 °C under positive gate override (Fig. 5, right). This can be attributed to the suppression of phonon scattering upon returning to room temperature conditions. Accordingly, a relatively larger drain current at $V_{gs} = 4$ V post-cooling results in a slightly decrease in $R_{on,sp}$ in comparison with that measured prior to high temperature exposure. Moreover, the hysteresis post-cooling decreased from 4.29 V at 298 °C to 1.26 V back at room temperature, although it remains significantly larger than the initial near-zero hysteresis (~0.01–0.09 V). In addition, the *SS* shifted from 1212(up)/1351(down) at 298 °C to 180.3(up)/210.8(down) mV/dec post-cooling. However, the V_{th} did not recover the following cooling process [−27.5 (up)/−26.3(down) V], indicating some of the high temperature activated traps at the oxide/β-Ga_2O_3 interface in the fin-shape channels persisted. These more severe irreversible effects observed in the FinFETs as compared to planar devices might be attributed to the higher thermal impact in narrower fins as previously modeled.[14] Table II provides a summary of the $R_{on,sp}$, hysteresis, *SS*, and V_{th} of the β-Ga_2O_3 FinFET before and after high temperature measurements.

In conclusion, we have conducted an investigation on the high temperature behavior of the lateral β-Ga_2O_3 FinFETs fabricated by the damage-free MacEtch process, for a temperature range up to ~300 °C. Below 150 °C, the FinFET performance remains relatively stable. However, at higher temperature, the off-state performance and hysteresis of the FinFETs experience significant degradation, while the on-state characteristics are less affected. The observed temperature dependence and the order of magnitude change in the I–V characteristics are similar to those reported for the planar β-Ga_2O_3 MOSFETs in the literature, despite our use of a much thicker (~2 μm epi-layer) β-Ga_2O_3 film as the channel in the FinFET. Further characterizations are needed to understand the detailed mechanism of the degradation as a function of geometry design, including the sidewall tapering. Note that the effect of sidewall tapering in FinFET structures has been studied for Si FinFETs in sub-22 nm node, by numerical simulations.[34–36] Interestingly, one study found that slightly improved *SS* and DIBL were observed in the tapered FinFETs in comparison with the vertical

TABLE II. The $R_{on,sp}$, hysteresis, *SS*, and V_{th} characteristics of the β-Ga_2O_3 FinFET measured under room temperature before and after the high temperature measurement.

			SS (mV/dec)		V_{th} (V)	
	$R_{on,sp}$ (mΩ·cm²)	hysteresis (V)	Up	Down	Up	Down
RT before HT	16.10	0.09	124.9	130.2	−6.8	
RT after HT	14.94	1.26	180.3	210.8	−27.5	−26.3

sidewall FinFETs due to the different potential distribution in two device structures.[34] With a tapered sidewall, it is possible that there exist multiple threshold values to turn on/off different part of the fin channels. However, the influence of the fin geometry on the current distribution at a function of temperature and, hence, the device performance metrics will need to be systematically studied both theoretically and experimentally.

We believe that the thermal stability of β-Ga_2O_3 FinFETs can be improved in several ways, including the improvement of the epitaxial material, especially thicker films,[37] the reduction of the body and interface trap density between the dielectric and β-Ga_2O_3; the employment of refractive metal gate contact; and passivation with higher thermal conductivity material, such as AlN. The potential advantage of the FinFET geometry over the planar counterpart for external heat removal also remains an important area for further exploration.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Zhongjie Ren and Hsien-Chih Huang contributed equally to this work.

Zhongjie Ren: Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – original draft (equal); Writing – review & editing (equal). **Wenjuan Zhu:** Data curation (supporting); Supervision (equal). **Xiuling Li:** Conceptualization (equal); Funding acquisition (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal). **hsien-chih huang:** Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Hanwool Lee:** Data curation (supporting). **Clarence Y. Chan:** Data curation (supporting); Writing – review & editing (supporting). **Henry C. Roberts:** Data curation (supporting); Writing – review & editing (supporting). **Xihang Wu:** Investigation (supporting). **Aadil Waseem:** Investigation (supporting); Writing – review & editing (supporting). **A. F. M. Anhar Uddin Bhuiyan:** Data curation (supporting). **Hongping Zhao:** Funding acquisition (equal); Supervision (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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