

Energy Efficient Neuro-Inspired Phase-Change Memory Based on $\text{Ge}_4\text{Sb}_6\text{Te}_7$ as a Novel Epitaxial Nanocomposite

Asir Intisar Khan, Heshan Yu, Huairuo Zhang, John R. Goggin, Heungdong Kwon, Xiangjin Wu, Christopher Perez, Kathryn M. Neilson, Mehdi Asheghi, Kenneth E Goodson, Patrick M. Vora, Albert Davydov, Ichiro Takeuchi, and Eric Pop*

Phase-change memory (PCM) is a promising candidate for neuro-inspired, data-intensive artificial intelligence applications, which relies on the physical attributes of PCM materials including gradual change of resistance states and multilevel operation with low resistance drift. However, achieving these attributes simultaneously remains a fundamental challenge for PCM materials such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$, the most commonly used material. Here bi-directional gradual resistance changes with $\approx 10\times$ resistance window using low energy pulses are demonstrated in nanoscale PCM devices based on $\text{Ge}_4\text{Sb}_6\text{Te}_7$, a new phase-change nanocomposite material. These devices show 13 resistance levels with low resistance drift for the first 8 levels, a resistance on/off ratio of ≈ 1000 , and low variability. These attributes are enabled by the unique microstructural and electro-thermal properties of $\text{Ge}_4\text{Sb}_6\text{Te}_7$, a nanocomposite consisting of epitaxial SbTe nanoclusters within the Ge-Sb-Te matrix, and a higher crystallization but lower melting temperature than $\text{Ge}_2\text{Sb}_2\text{Te}_5$. These results advance the pathway toward energy-efficient analog computing using PCM.

is further aggravated by the physically separated logic and memory units in the traditional von Neumann architecture, incurring significant energy dissipation during the back-and-forth shuttling of large data sets.^[2] To overcome this bottleneck, neuro-inspired computing approaches such as in-memory computing are being actively explored to unify the processing and storage within the memory cells.^[3,4] These efforts rely on exploiting the physical attributes of the nanoscale memory devices to perform computational tasks within the memory units,^[2,5-7] thus blurring the boundary between the processing and memory units. Memory technology such as phase-change memory (PCM) and resistive random-access memory (RRAM) are promising as computational memory units.^[2,8,9] PCM is already a mature storage-class memory bridging the performance gap between existing memory technologies such as flash (nonvolatile, but relatively slow) and dynamic random-access memory (fast, but volatile).^[10,11] The thermally induced phase transition in PCM is achieved using electrical pulses for crystallization (set) and melt-quenched

1. Introduction

Numerous emerging data-centric applications are reaching their scalability limits in terms of latency and energy.^[1] The challenge

and dynamic random-access memory (fast, but volatile).^[10,11] The thermally induced phase transition in PCM is achieved using electrical pulses for crystallization (set) and melt-quenched

A. I. Khan, X. Wu, K. M. Neilson, E. Pop

Department of Electrical Engineering
Stanford University
Stanford, CA 94305, USA
E-mail: epop@stanford.edu

H. Yu, I. Takeuchi
Department of Materials Science and Engineering
University of Maryland
College Park, MD 20742, USA

H. Zhang, A. Davydov
Materials Science and Engineering Division
National Institute of Standards and Technology
Gaithersburg, MD 20899, USA

H. Zhang
Theiss Research, Inc.
La Jolla, CA 92037, USA

J. R. Goggin, P. M. Vora

Department of Physics and Astronomy
George Mason University
Fairfax, VA 22030, USA

J. R. Goggin, P. M. Vora, A. Davydov
Quantum Science and Engineering Center
George Mason University
Fairfax, VA 22030, USA

H. Kwon, C. Perez, M. Asheghi, K. E Goodson
Department of Mechanical Engineering
Stanford University
Stanford, CA 94305, USA

E. Pop
Department of Materials Science & Engineering
Stanford University
Stanford, CA 94305, USA

E. Pop
Precourt Institute for Energy
Stanford University
Stanford, CA 94305, USA

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/adma.202300107>

DOI: 10.1002/adma.202300107

amorphization (reset). PCM offers lower cycle-to-cycle variability than RRAM, substantially faster switching speed than electrochemical RAM,^[12] a larger memory operation window, and longer write endurance than flash.^[10] These advantages and its potential for multilevel memory make PCM also attractive for neuromorphic applications.^[4,5,13,14]

However, abrupt resistance change during amorphization in PCM is a limiting factor for artificial neural networks^[2,5,13,15] where bi-directional and gradual resistance change is desired between the lowest resistance state (LRS) and highest resistance state (HRS). In addition, cycle-to-cycle variation, large fluctuations in LRS and HRS, and resistance drift during multilevel state operation remain challenges for efficient neuro-inspired applications using PCM. System-level solutions such as multi-PCM schemes^[15,16] using partial crystallization (set only) and mixed-precision in-memory computing have been explored,^[1,2] albeit at the expense of increased complexity. Recently, phase-change superlattices have also been employed to address part of these challenges as an intrinsic materials-based solution.^[5,14,17] The use of non-identical pulses with varying amplitude and/or pulse width has also been introduced, but such schemes necessarily increase the programming and hardware complexity in systems.^[8,13]

Here, we overcome these challenges in nanoscale PCM devices using our recently-discovered phase-change nanocomposite $\text{Ge}_4\text{Sb}_6\text{Te}_7$, which we had earlier identified as having a larger optical bandgap and contrast between the crystalline and amorphous states compared to $\text{Ge}_2\text{Sb}_2\text{Te}_5$.^[18] In the present work, we show that $\text{Ge}_4\text{Sb}_6\text{Te}_7$ can be used for robust electrical-switching nanoscale PCM, aimed at neuro-inspired computing applications. We demonstrate bi-directional gradual resistance change over a $\approx 10\times$ window in $\text{Ge}_4\text{Sb}_6\text{Te}_7$ PCM using low energy, constant amplitude pulse schemes. The devices display more than 10 resistance states with low resistance drift. The unique microstructural and electro-thermal properties of $\text{Ge}_4\text{Sb}_6\text{Te}_7$ enable faster-switching speed, lower variability, and higher stability of the resistance states compared to $\text{Ge}_2\text{Sb}_2\text{Te}_5$, thus taking the PCM technology a step further for energy-efficient neuromorphic applications.

2. Results and Discussion

We first address the microstructural properties of $\text{Ge}_4\text{Sb}_6\text{Te}_7$, which give rise to its superior PCM performance described below. We used high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) to image a ≈ 200 nm-thick cross-sectional $\text{Ge}_4\text{Sb}_6\text{Te}_7$ polycrystalline film (Figure 1a; Figure S1, Supporting Information; also see Experimental Section). The atomic-resolution HAADF-STEM images show the presence of the SbTe nanophase (average size ≈ 10 nm) grown coherently with the cubic Ge–Sb–Tb (GST) matrix along all $\{111\}_{\text{cubic}}$ crystallographic planes. Analysis of the electron diffraction rings confirms the nanophase composition to be Sb_1Te_1 .^[18] While the films here were deposited from a stoichiometric target (see Experimental Section), we note that identical results were obtained in our previous work^[18] with co-sputtering from separate Sb, Te, and Ge targets.

A recent trend in designing high-performance PCM materials has led to multilayered structures and superlattices including $\text{Sb}_2\text{Te}_3/\text{GeTe}$,^[14,17,19] $\text{Sb}_2\text{Te}_3/\text{Ge}_2\text{Sb}_2\text{Te}_5$,^[20] and

$\text{Sb}_2\text{Te}_3/\text{TiTe}_2$.^[5,21] In such materials, alternating layers serve both as diffusion barriers (e.g., TiTe_2) and nucleation sites (e.g., Sb_2Te_3) facilitating fast switching speed.^[5] We believe the naturally occurring nanocomposite structure seen in $\text{Ge}_4\text{Sb}_6\text{Te}_7$ may be playing a similar role, where ≈ 10 nm SbTe nanoclusters can act as nucleation sites enabling its fastswitching speed (as discussed below).

We performed Raman measurements to understand the local bonding environment of $\text{Ge}_4\text{Sb}_6\text{Te}_7$ in its amorphous (Figure 1b) and crystalline (Figure 1c) phases. In the amorphous phase of $\text{Ge}_4\text{Sb}_6\text{Te}_7$, two modes^[22,23] centered at ≈ 119 cm^{-1} and ≈ 150 cm^{-1} (A_1 mode) are observed related to the vibrations of defective octahedra,^[24,25] which are also associated with the octahedral coordination in the crystalline phase of $\text{Ge}_4\text{Sb}_6\text{Te}_7$ (Figure 1c). This indicates the similarity in the local structure between the amorphous and thecrystalline phases of $\text{Ge}_4\text{Sb}_6\text{Te}_7$ in contrast to $\text{Ge}_2\text{Sb}_2\text{Te}_5$,^[24,26] where such similarity has not been detected. The close resemblance in bonding environments between the amorphous and crystalline states may be an indication of the presence of a possible structure in the amorphous state which serves as a precursor for crystallizing $\text{Ge}_4\text{Sb}_6\text{Te}_7$. Such a property can further help facilitate fast switching in $\text{Ge}_4\text{Sb}_6\text{Te}_7$ PCM as will be discussed later below.

Our temperature-dependent X-ray diffraction (XRD) data in Figure 1d reveal the structural evolution of as-deposited amorphous $\text{Ge}_4\text{Sb}_6\text{Te}_7$ with increasing temperature. The measured XRD patterns at room temperature for as-deposited amorphous $\text{Ge}_4\text{Sb}_6\text{Te}_7$ show no GST peaks. Diffraction peaks emerge at ≈ 220 $^{\circ}\text{C}$, indicating the amorphous to the crystalline phase transition. Upon further increasing the temperature, the diffraction peaks disappear at the temperature range of 500 $^{\circ}\text{C}$ to 540 $^{\circ}\text{C}$, marking the melting temperature of $\text{Ge}_4\text{Sb}_6\text{Te}_7$. We note that the measured melting temperature for $\text{Ge}_4\text{Sb}_6\text{Te}_7$ (<540 $^{\circ}\text{C}$) is at least 60 $^{\circ}\text{C}$ lower than that of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (≈ 600 $^{\circ}\text{C}$).^[27] We attribute the lowered melting temperature in $\text{Ge}_4\text{Sb}_6\text{Te}_7$ vs $\text{Ge}_2\text{Sb}_2\text{Te}_5$ to the bond distortions at the interface between the coherent SbTe nanophase and the GST matrix. In addition, the SbTe nanophase in the GST matrix has a lower melting temperature, ≈ 420 $^{\circ}\text{C}$,^[28] which could also play a role in promoting the gradual resistance change (as we show below) during the operation of $\text{Ge}_4\text{Sb}_6\text{Te}_7$ PCM.

Measurements of temperature-dependent sheet resistance (Figure 1e) of $\text{Ge}_4\text{Sb}_6\text{Te}_7$ and $\text{Ge}_2\text{Sb}_2\text{Te}_5$ show a drop in resistance at ≈ 200 $^{\circ}\text{C}$ and ≈ 150 $^{\circ}\text{C}$, respectively, corresponding to their crystallization temperature. This agrees with the structural change of $\text{Ge}_4\text{Sb}_6\text{Te}_7$ from an amorphous to a cubic phase revealed in our XRD data (Figure 1b), underscoring a higher crystallization temperature in $\text{Ge}_4\text{Sb}_6\text{Te}_7$ compared to $\text{Ge}_2\text{Sb}_2\text{Te}_5$.^[10,27] Thus, as evident from Figure 1e, $\text{Ge}_4\text{Sb}_6\text{Te}_7$ shows a gradual change in resistance over a larger temperature range compared to $\text{Ge}_2\text{Sb}_2\text{Te}_5$. We also used time domain thermoreflectance with a setup previously described^[17] to measure the effective thermal conductivity of $\text{Ge}_4\text{Sb}_6\text{Te}_7$ and $\text{Ge}_2\text{Sb}_2\text{Te}_5$ stacks (Figure 1f). Figure 1f shows that the effective thermal conductivity in the crystalline phase is higher in $\text{Ge}_4\text{Sb}_6\text{Te}_7$ compared to $\text{Ge}_2\text{Sb}_2\text{Te}_5$. This could be attributed to a larger electronic contribution to the thermal conductivity of $\text{Ge}_4\text{Sb}_6\text{Te}_7$, originating from the $\approx 10\times$ smaller electrical resistivity of the crystalline phase (Figure 1e). On the other hand, despite the smaller electrical resistivity and higher thermal

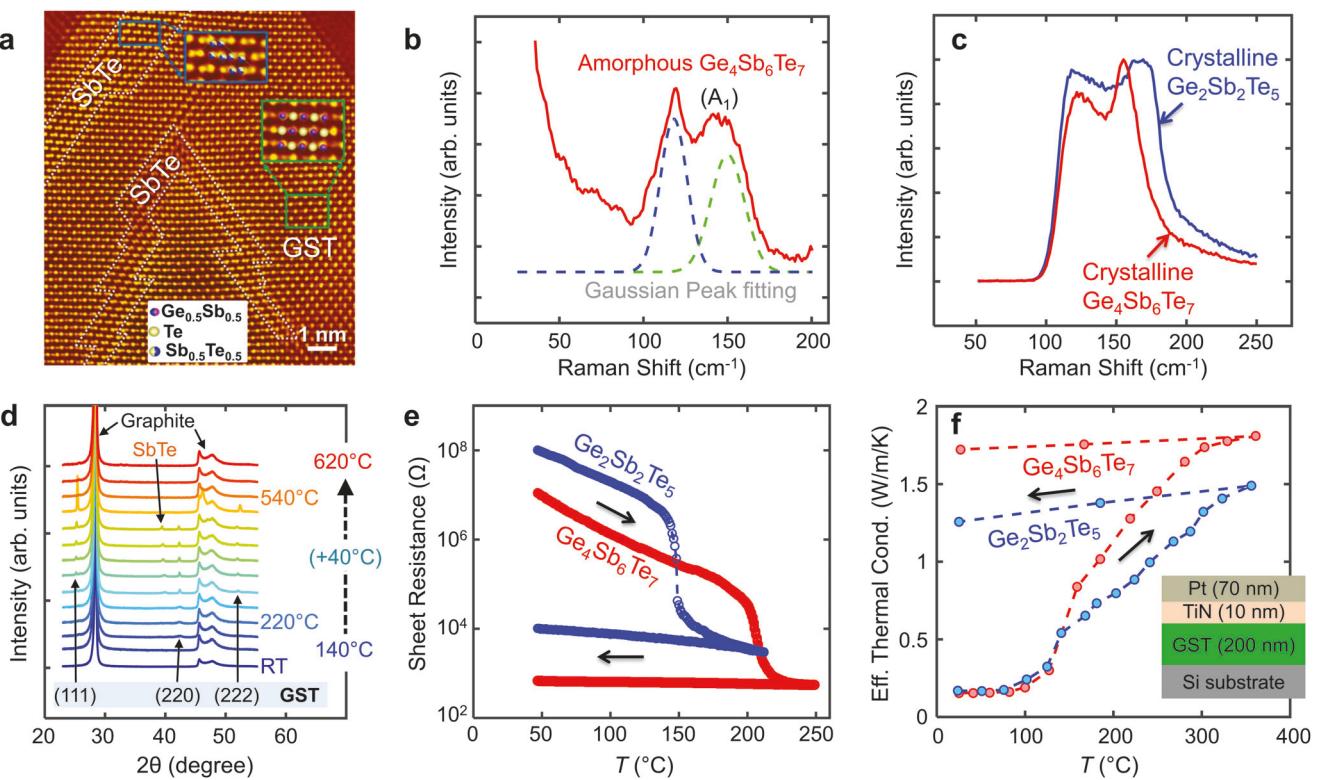


Figure 1. Microstructural and electro-thermal properties of Ge₄Sb₆Te₇. a) Atomic resolution HAADF-STEM image taken along the (110)_{cubic} zone axis showing the SbTe nanophase coherently grown inside the GST matrix. STEM image shows a representative region of a polycrystalline Ge₄Sb₆Te₇ film (\approx 200 nm thick) deposited at room temperature on a Si substrate, followed by in situ annealing at \approx 200 °C. The atomically sharp interfaces between SbTe and the GST matrix are clearly visible. b) Raman spectrum of amorphous Ge₄Sb₆Te₇. The dashed lines are fitting curves of two modes centered at 119 cm⁻¹ (blue) and 150 cm⁻¹ (green). The A₁ mode is centered at \approx 150 cm⁻¹. c) Raman spectra of polycrystalline Ge₄Sb₆Te₇ (red) and Ge₂Sb₂Te₅ (blue). d) Evolution of the XRD pattern of a Ge₄Sb₆Te₇ film from room temperature (where it was deposited in the amorphous state) to 620 °C. The emergence of the GST diffraction peaks at \approx 220 °C reveals the crystallization temperature. Thereafter, the disappearance of diffraction peaks at \approx 540 °C indicates the melting temperature for Ge₄Sb₆Te₇. Some peaks are from the graphite dome covering the heating stage of the XRD setup at high temperatures. e) Measured sheet resistance as a function of temperature for 200 nm-thick Ge₄Sb₆Te₇ (red) and Ge₂Sb₂Te₅ (blue) films. The sudden drop in Ge₄Sb₆Te₇ resistance is consistent with the crystallization temperature observed in the XRD data. f) Measured effective thermal conductivity of 200 nm-thick Ge₄Sb₆Te₇ and Ge₂Sb₂Te₅ films (including TiN/Pt capping; stack shown in the inset) from room temperature to \approx 360 °C and back. For (d–f), the films were deposited at room temperature.

conductivity in the crystalline phase of Ge₄Sb₆Te₇, the significantly lower melting temperature of Ge₄Sb₆Te₇ (over 60 °C lower than that of Ge₂Sb₂Te₅) and its SbTe nanophase (\approx 200 °C lower than that of Ge₂Sb₂Te₅) further ensure the lower reset energy operation in Ge₄Sb₆Te₇ PCM devices compared to Ge₂Sb₂Te₅, as will be explored below.

Figure 2a shows the schematic of our fabricated mushroom-cell PCM device with \approx 60 nm-thick Ge₄Sb₆Te₇ on a \approx 110 nm diameter TiN bottom electrode (BE) (see Experimental Section for the fabrication details and Figure S2 (Supporting Information) for a scanning electron microscopy image of the fabricated device). The setup for the electrical measurement of our PCM devices is described in detail elsewhere.^[14] We read the resistance of all devices with a 50 mV DC bias.

Figure 2b shows the multi-level resistance states of such a Ge₄Sb₆Te₇ PCM device. We achieve 13 distinct resistance states using single-shot pulses, each one starting in the LRS with increasing amplitude (from 1.35 to 2.1 V; see Figure S3 (Supporting Information) for the complete list of voltages) and the same pulse shape (1/20/1 ns rise/width/fall time). We note that even

more intermediate resistance states could be achieved in this material composite, by further fine-tuning the amplitude of the voltage pulses and/or using more complex read-verify programming algorithms.^[13] Figure 2b also demonstrates low resistance drift for the first 8 levels, with a drift coefficient $\nu \approx 0.01$ for level 8 (measured for 1 h), which is promising for analog PCM applications as well as for high-density memory.^[2] However, beyond level 8 a larger resistance drift is observed, with an estimated $\nu \approx 0.1$ for level 13, which is comparable to conventional Ge₂Sb₂Te₅ PCM.^[11]

Figure 2c shows the gradual and nearly linear change in resistance (\approx 10 \times resistance window) during the depression from high to low conductance (here shown from low to high resistance) in well-cycled Ge₄Sb₆Te₇ PCM, averaged over 25 different cycles. For depression, we applied consecutive reset pulses of the same magnitude and shape (1.45 V; 1/45/1 ns rise/width/fall time). Figure 2d demonstrates the gradual resistance change (\approx 10 \times resistance window) during potentiation from low to high conductance (i.e., high to low resistance) in the same device, achieved by applying consecutive set pulses of the same magnitude and

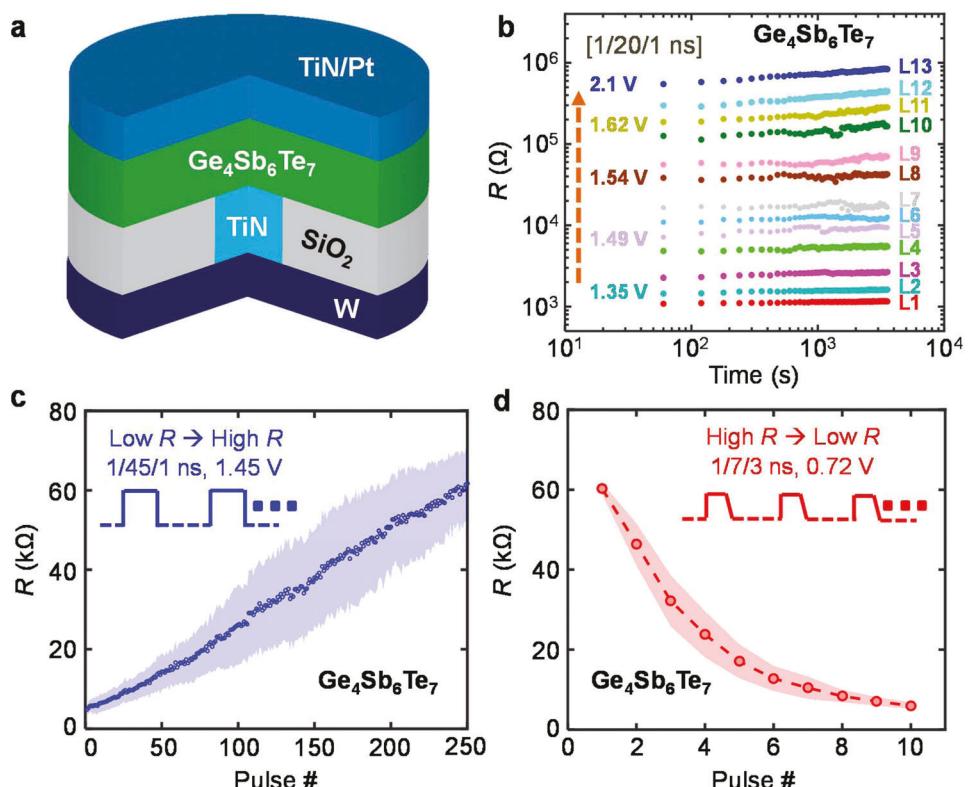


Figure 2. Multilevel operation and gradual resistance change in Ge₄Sb₆Te₇ PCM. a) Schematic of the “mushroom cell” PCM device with \approx 60 nm Ge₄Sb₆Te₇. b) 13 resistance levels (L1 to L13) are achieved in a device with \approx 110 nm BE diameter, reflecting robust multilevel capability with low resistance drift for the first eight levels. Increasing voltage reset pulses (1/20/1 ns rise/width/fall time) were used, each starting in the LRS (see Figure S3 (Supporting Information) for all voltage levels used). c) Gradual resistance change in Ge₄Sb₆Te₇ PCM (\approx 110 nm BE diameter) from low to high resistance states, averaged over 25 cycles with identical voltage pulses (1.45 V; 1/45/1 ns). d) Gradual resistance change from high to low resistance states for the same device as in (c) averaged over 25 cycles with identical voltage pulses (0.72 V; 1/7/3 ns). The standard deviation is represented in the shaded blue and red regions in (c) and (d), respectively. Figure S4 (Supporting Information) shows the corresponding changes in average conductance.

shape (0.72 V; 1/7/3 ns). Figure S4a,b (Supporting Information) shows the corresponding gradual change in the average conductance (\approx 10 \times window) from high to low and low to high states, respectively. Gradual resistance changes for 10 different cycles for both depression and potentiation transition with $>10\times$ resistance window are shown in Figure S5a,b (Supporting Information) respectively. As discussed earlier, the SbTe nanophase in the GST matrix has a lower melting temperature (\approx 420 °C)^[28] compared to the overall Ge₄Sb₆Te₇ melting temperature (\approx 540 °C), which could help promote the observed gradual resistance change during the operation of Ge₄Sb₆Te₇ PCM. We also note that the asymmetry between the potentiation and depression arises from the significantly faster switching speed from a partially amorphized state (the high resistance state \approx 60 kΩ) to a crystalline state (lower resistance state \approx 6 kΩ). However, such asymmetry can be improved by tuning the pulse amplitude, pulse duration, as well as degree of amorphization or crystallization, that is, the resistance window for potentiation and depression. To this end, we have further confirmed that the linearity, symmetricity, and resistance (conductance) window can be tuned with even smaller voltages or shorter pulses, as shown in Figure S6a-c (Supporting Information).

From Figure 2c,d, we estimate the pulse energies (E) for potentiation and depression as $E = t_p V_p^2 / R$, where t_p is the pulse du-

ration, V_p is the pulse voltage amplitude, and R is the measured resistance. Thus, for depression with a \approx 10 \times resistance window (from low $R \approx$ 6 kΩ to high $R \approx$ 60 kΩ), using constant amplitude 1.45 V pulses with 47 ns pulse duration (the sum of the rise time, pulse width, and fall time), the maximum (minimum) pulse energies for our Ge₄Sb₆Te₇ PCM devices are estimated to be 16.5 pJ (1.65 pJ). Similarly, the maximum (minimum) pulse energies during potentiation (from 60 to 6 kΩ), using 0.72 V pulses with 11 ns total pulse duration are estimated to be 0.95 pJ (\approx 95 fJ), these figures being lower than pulse energies in all previous reports of PCM devices for neuromorphic applications.^[5,29–31]

To confirm the reproducibility, depression, and potentiation with \approx 10 \times resistance window for five different devices are displayed in Figure S7a,b (Supporting Information), respectively. Moreover, the symmetricity between the potentiation and depression could be further improved using iterative programming techniques.^[2,13] However, we note that the gradual resistance change (\approx 10 \times resistance window) achieved here during both potentiation and depression relies only on the materials-based solution (here Ge₄Sb₆Te₇) without increasing the programming and hardware complexity. Our Ge₄Sb₆Te₇ PCM devices thus display bi-directional, gradual tunability of resistance with identical low-energy pulses, in contrast to previous PCM demonstrations^[32–34] which required increasing amplitude pulses to achieve gradual

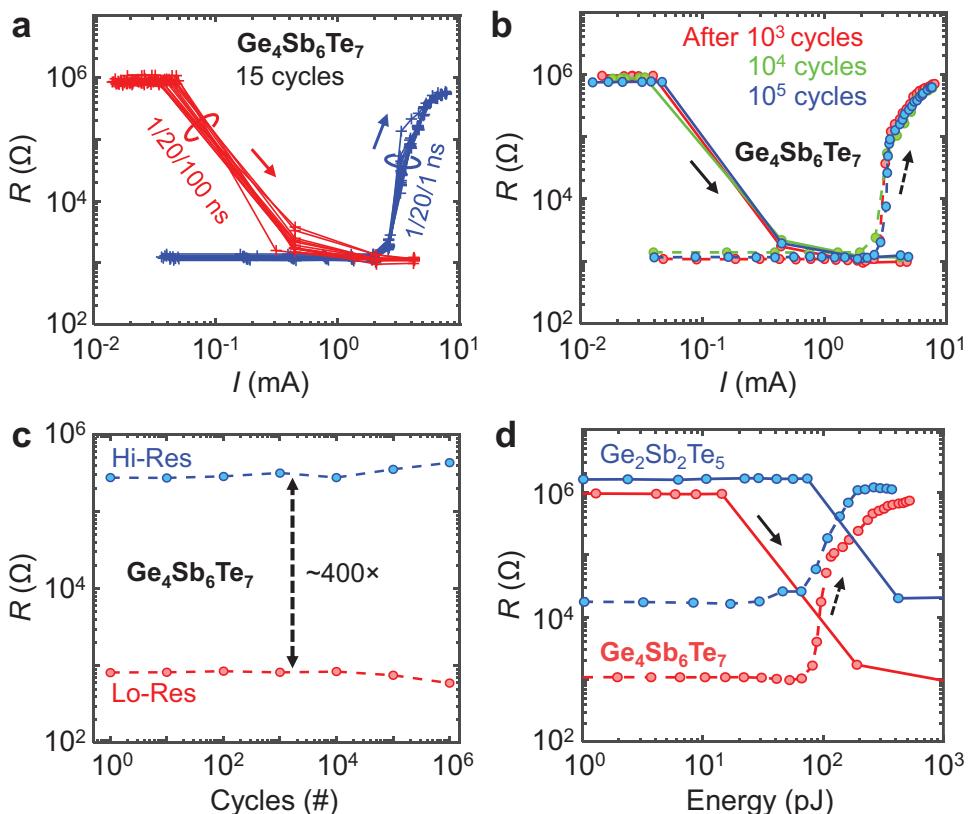


Figure 3. Variation, endurance, and energy of Ge₄Sb₆Te₇ PCM. a) Measured resistance (R) vs current (I) for 15 consecutive cycles of Ge₄Sb₆Te₇ PCM, for a well-cycled device (>5000 cycles). The curves in red show the transition from HRS to LRS and the ones in blue represent the LRS to HRS transition. The programming pulse rise/width/fall times are listed in the figure. b) Measured R vs I for a Ge₄Sb₆Te₇ PCM after 1000, 10 000, and 100 000 cycles, showing the stability and repeatability of the device even after extensive cycling. c) Resistance on/off ratio ≈ 400 is maintained for $>10^6$ switching cycles programmed using a single shot set (1/20/100 ns, 1.5 V) and reset (1/20/1 ns, 2.4 V) pulses, with resistance states read every 10x cycles. d) R vs energy comparing Ge₄Sb₆Te₇ PCM (in red) with Ge₂Sb₂Te₅ PCM (in blue). The solid lines are from HRS to LRS (pulse shape 1/20/100 ns for Ge₄Sb₆Te₇ and 1/20/400 ns for Ge₂Sb₂Te₅), dashed lines are from LRS to HRS (1/20/1 ns reset pulse shape for both). All PCM devices shown in this figure have a bottom electrode diameter of ≈ 110 nm.

low to a high resistance state transition. The simpler, constant-pulse approach of our Ge₄Sb₆Te₇ PCM can be advantageous for large-scale neuromorphic systems of crossbar arrays, compared to increasing-amplitude schemes which can lead to capacitive line-charging and high-power dissipation.^[13,29]

Next, we explore the stability and cycle-to-cycle variation of our Ge₄Sb₆Te₇ PCM, in Figure 3a,b. Resistance (R) vs current (I) curves for 15 consecutive switching cycles of a well-cycled (over 5000 times) Ge₄Sb₆Te₇ PCM device are shown in Figure 3a, demonstrating low cycle-to-cycle variation; the corresponding R vs voltage (V) is shown in Figure S8 (Supporting Information). Data for five other devices are shown in Figure S9a,b (Supporting Information), confirming low variability between the devices. We have a resistance on/off ratio of ≈ 1000 in our Ge₄Sb₆Te₇ PCM devices which is desirable for multilevel and high-density memory operation. The low cycle-to-cycle variation and the stability of LRS and HRS are further demonstrated for $\approx 10^4$ cycles (Figure S10a,b, Supporting Information). From Figure S10a (Supporting Information), the fluctuations in the LRS (12%) and HRS (4%) of our extensively-cycled Ge₄Sb₆Te₇ PCM devices are substantially lower than those of previously-reported Ge₂Sb₂Te₅ PCM,^[5,35] and are comparable to those achieved

using phase-change heterostructures.^[5] The low cycle-to-cycle variation and good stability of Ge₄Sb₆Te₇ PCM can be attributed to the higher crystallization temperature^[10] in Ge₄Sb₆Te₇ (≈ 200 °C) vs Ge₂Sb₂Te₅ (≈ 150 °C).^[10,27] The higher crystallization temperature also enables good data retention in Ge₄Sb₆Te₇-based PCM. As shown in Figure S11 (Supporting Information), the highest resistance state of Ge₄Sb₆Te₇ PCM devices can retain its state for >11 days at a measurement temperature of 105 °C and for ≈ 3 h at 145 °C.

Furthermore, our Ge₄Sb₆Te₇ PCM devices can maintain $\approx 400\times$ resistance on/off ratio for $>10^6$ switching cycles (read-verified every 10x switching cycles), indicating good endurance (Figure 3c). We note that this is achieved using single-shot programming pulses (set and reset), and thus in the event of gradual switching (e.g., in neuromorphic applications) where there will be less programming stress on the cell,^[32] we expect a significantly larger endurance for our Ge₄Sb₆Te₇ PCM devices compared to Ge₂Sb₂Te₅-based devices. We further show the robustness of the endurance of our Ge₄Sb₆Te₇ PCM devices maintaining $\approx 100\times$ resistance on/off ratio upon reading the DC resistance every switching cycle for $\approx 10^5$ switching cycles (Figure S12, Supporting Information).

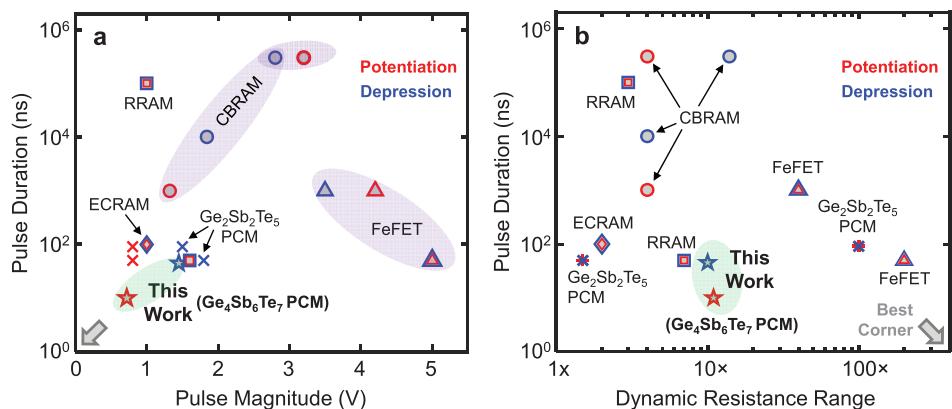


Figure 4. Comparison of memory technologies for neuromorphic device applications. a) Pulse duration vs pulse magnitude. b) Pulse duration vs dynamic resistance (gradual resistance change) range for different nonvolatile memories^[9,30,31,39–44] including our Ge₄Sb₆Te₇ PCM (shown in stars within the green-shaded regions). The data points shown in blue represent depression, that is, gradual change in resistance from a low to high resistance state. The data points shown in red represent potentiation, that is, gradual change in resistance from the high to a low resistance state of the memory device. The best corners indicated by silver arrows represent the limits where the potentiation and depression are achieved using the smallest pulse duration and the smallest pulsing magnitude in (a), and the largest dynamic resistance range achieved using the smallest pulse duration in (b). Our Ge₄Sb₆Te₇ PCM displays some of the best characteristics, placing it close to the best corners in both figures. (PCM: Phase-change memory; RRAM: Resistive random-access memory; ECRAM: Electrochemical random-access memory; CBRAM: Conductive bridge random-access memory | FeFET: Ferroelectric field-effect transistor).

For devices with the same BE diameter (all \approx 110 nm here), our Ge₄Sb₆Te₇ PCM devices have \approx 3 and 4 \times lower set energy (E_{set}) and slightly lower reset energy (E_{reset}) compared to those of the control Ge₂Sb₂Te₅ PCM device (Figure 3d). We estimate the R vs energy by multiplying the peak power [obtained from R vs I in Figure S13a (Supporting Information) and R vs V in Figure S13b (Supporting Information)] with the set and reset pulse durations. For reset programming of both Ge₄Sb₆Te₇ and Ge₂Sb₂Te₅ PCM devices, we use 1/20/1 ns rise/width/fall pulses, respectively, with a setup previously described.^[14] The set programming of the Ge₄Sb₆Te₇ PCM was possible with a shorter pulse duration (1/20/100 ns rise/width/fall) compared to that needed for Ge₂Sb₂Te₅ PCM (1/20/400 ns rise/width/fall).

E_{set} and E_{reset} are defined here as the energy required for the HRS to LRS and LRS to HRS transitions (with \approx 10 \times resistance window), respectively. The significantly lower E_{set} for Ge₄Sb₆Te₇ compared to Ge₂Sb₂Te₅ originates from the faster set switching speed in Ge₄Sb₆Te₇ (120 ns) vs Ge₂Sb₂Te₅ (420 ns). As discussed above, the similarity in the local bonding environment of Ge₄Sb₆Te₇ between the amorphous and crystalline states (Figure 1b,c) and the presence of SbTe nanophase within the GST matrix (Figure 1a; Figure S1, Supporting Information) help facilitate the faster switching speed in Ge₄Sb₆Te₇ PCM compared to Ge₂Sb₂Te₅, leading to lower E_{set} . E_{reset} for Ge₄Sb₆Te₇ is also slightly smaller compared to control Ge₂Sb₂Te₅ which can be attributed to the lower melting temperature of Ge₄Sb₆Te₇, as discussed earlier.

Thus, our Ge₄Sb₆Te₇ PCM devices concurrently exhibit unique gradual and nearly linear change of resistance states with constant amplitude pulses of ultralow energy, as well as lower power and faster switching, good endurance, stability, and retention at a higher temperature than control Ge₂Sb₂Te₅ PCM. These electronic properties originate from the unique microstructural and electro-thermal properties of Ge₄Sb₆Te₇: i) a nanocomposite consisting of epitaxial SbTe nanoclusters within the Ge–Sb–Te ma-

trix; ii) the similarity in the local bonding environment between the amorphous and crystalline phases; iii) high crystallization temperature; and iv) a low melting temperature including the presence of a nanocomposite with a separate (but lower) melting temperature. From a materials standpoint, our PCM devices using the novel epitaxial nanocomposite Ge₄Sb₆Te₇ should further encourage high-throughput materials screening of other phase-change nanocomposites (e.g., Ti–Sb–Te)^[36–38] and relevant optimization techniques such as doping to promote gradual, low-power and faster switching in PCM with high thermal stability and retention for future neuro-inspired applications. At the same time, a future study involving more detailed microstructural characterization could provide further insight into the correlation between the nanostructure and the PCM device performance. In particular, while challenging to perform, *in situ* TEM during the switching operation of a nanoscale Ge₄Sb₆Te₇ PCM device may shed light on the role of the material's defect density.

Finally, we compare our Ge₄Sb₆Te₇ PCM devices with other emerging non-volatile memories for neuromorphic applications across various parameters (Figure 4a,b, Table S1, Supporting Information). A simultaneous presence of a large dynamic resistance on/off ratio, fast-switching speed (e.g., small pulse duration), and small pulsing amplitude for both potentiation and depression are desirable for neuromorphic applications. Our nanoscale Ge₄Sb₆Te₇ PCM devices are promising with their fast gradual programming speed (<50 ns, as low as 10 ns, see Figure 2), small pulsing voltage (<1.5 V, as low as 0.65 V, Figure S6, Supporting Information) while maintaining a large dynamic resistance window (>10 \times) both for potentiation and depression. These promising characteristics for neuromorphic applications have otherwise not been achieved using other phase-change material candidates such as Ge₂Sb₂Te₅. The pulse width and amplitude needed for potentiation and depression in our Ge₄Sb₆Te₇ can be reduced in smaller BE diameter devices for more energy-efficient operation, further helping to position PCM as a

promising candidate among other emerging technologies for neuromorphic applications.

3. Conclusion

We have demonstrated a nanoscale PCM with robust multilevel resistance states as well as bi-directional and gradual tuning over $\approx 10\times$ resistance window, which can be achieved with energy-efficient electrical pulses of low amplitude and nanosecond-pulse duration. This is enabled by the unique microstructural and electro-thermal properties of the new $\text{Ge}_4\text{Sb}_6\text{Te}_7$ phase-change material composite within the PCM cell. These PCM devices further show fast switching speed, low cycle-to-cycle variation, and good endurance. We have thus demonstrated $\text{Ge}_4\text{Sb}_6\text{Te}_7$ as a novel material for PCM, which can facilitate energy-efficient analog computing as well as fast, high-density data storage. Future work should focus on further increasing the number of resistance states, improving the resistance drift of the higher resistance states, and lowering the switching current in $\text{Ge}_4\text{Sb}_6\text{Te}_7$ PCM, which could be achieved by incorporating this new material into a superlattice structure.^[5,14,45]

4. Experimental Section

For the fabrication of the $\text{Ge}_4\text{Sb}_6\text{Te}_7$ and $\text{Ge}_2\text{Sb}_2\text{Te}_5$ mushroom cell PCM devices, we started with the planarized TiN BE. Prior to the deposition of $\text{Ge}_4\text{Sb}_6\text{Te}_7$ ($\text{Ge}_2\text{Sb}_2\text{Te}_5$), the bottom TiN surface was in situ cleaned by Ar ion etching (30 standard cubic centimeters per minute (sccm) Ar flow, 50 W radio-frequency (rf) bias for 2 min) to remove any native oxide. Then the phase-change material (20 sccm Ar flow, 12 W DC power, 2 mTorr pressure) was sputtered from a stoichiometric $\text{Ge}_4\text{Sb}_6\text{Te}_7$ ($\text{Ge}_2\text{Sb}_2\text{Te}_5$) sputtering target at room temperature followed by in situ annealing at 200 °C. (It was noted that identical results were obtained in the previous work^[18] with co-sputtering from separate Sb, Te, and Ge targets.) Next, after letting the chamber cool down to room temperature, 10 nm TiN was deposited as the capping layer before breaking the vacuum. The phase-change stack was patterned by reactive ion etching using 30 sccm Cl_2 / 5 sccm BCl_3 , 10 sccm Ar, 60 W rf power at a pressure of 10 mTorr. Next, after doing another in situ Ar cleaning for 2 min, 10 nm TiN was sputtered followed by 50 nm Pt and lift-off as the top electrode. The setup for the electrical measurement of the PCM devices is described in detail elsewhere.^[14] For the time-domain thermoreflectance measurement in Figure 1f, the samples consist of (bottom to top): silicon substrate, 200 nm $\text{Ge}_4\text{Sb}_6\text{Te}_7$ ($\text{Ge}_2\text{Sb}_2\text{Te}_5$), 10 nm TiN capping layer, and 70 nm-thick platinum transducer layer, all sputtered at room temperature without breaking the vacuum.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

A.I.K. is thankful to James McVittie for the lab support and to Chris Neumann for the electrical measurement setup. This work was performed at the Stanford Nanofabrication Facility (SNF) and Stanford Nano Shared Facilities (SNSF) and was supported in part by member companies of the Stanford Non-Volatile Memory Technology Research Initiative (NMTRI) and in part by nCORE, a Semiconductor Research Corporation program,

sponsored by National Institute of Standards and Technology (NIST). A.I.K and K.M.N. acknowledge support from the Stanford Graduate Fellowship. H.K. acknowledges support from the Kwanjeong Educational Foundation Fellowship. C.P. acknowledges support from DARE fellowship. The work at the University of Maryland was partly supported by ONR MURI N00014-17-1-2661. H.Z. acknowledges support from the U.S. Department of Commerce, NIST under financial assistance award 70NANB19H138. A.V.D. acknowledges support from the Material Genome Initiative funding allocated to NIST. NIST disclaimer: Certain commercial equipment, instruments, or materials were identified in this manuscript to specify the experimental procedure adequately. Such identification was not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor was it intended to imply that the materials or equipment identified were necessarily the best available for the purpose. P.M.V. and J.G.G acknowledge support from the National Science Foundation (NSF) under Grant No. DMR-1847782 and the George Mason University Quantum Science and Engineering Center.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

A.I.K and E.P. conceived the idea together with H.Y. and I.T. A.I.K designed the experiments. A.I.K fabricated the devices, carried out the measurements, and analyzed the data. A.I.K performed material deposition and H.Y., H.Z., J.G.G, H.K., C.P., X.W. and K.M.N performed material and electro-thermal characterization. A.I.K. and E.P. wrote the manuscript with help from H.Y. and I.T. All authors discussed the results and commented on the manuscript. E.P. supervised the work.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

analog memory, low-energy memory, nanocomposites, neuro-inspired phase-change memory

Received: January 4, 2023

Published online: June 15, 2023

- [1] A. Sebastian, M. L. Gallo, R. Khaddam-Aljameh, E. Eleftheriou, *Nat. Nanotechnol.* **2020**, *15*, 529.
- [2] A. Sebastian, M. L. Gallo, G. W. Burr, S. Kim, M. BrightSky, E. Eleftheriou, *J. Appl. Phys.* **2018**, *124*, 111101.
- [3] J. Feldmann, N. Youngblood, C. D. Wright, H. Bhaskaran, W. H. P. Pernice, *Nature* **2019**, *569*, 208.
- [4] W. Zhang, R. Mazzarello, M. Wuttig, E. Ma, *Nat. Rev. Mater.* **2019**, *4*, 150.
- [5] K. Ding, J. Wang, Y. Zhou, H. Tian, L. Lu, R. Mazzarello, C. Jia, W. Zhang, F. Rao, E. Ma, *Science* **2019**, *366*, 210.
- [6] Q. Xia, J. J. Yang, *Nat. Mater.* **2019**, *18*, 309.
- [7] S. Yu, *Proc. IEEE* **2018**, *106*, 260.
- [8] M. Suri, O. Bichler, D. Querlioz, B. Traoré, O. Cueto, L. Perniola, V. Sousa, D. Vuillaume, C. Gamrat, B. DeSalvo, *J. Appl. Phys.* **2012**, *112*, 054904.

[9] W. Wu, H. Wu, B. Gao, N. Deng, S. Yu, H. Qian, *IEEE Electron Device Lett.* **2017**, *38*, 1019.

[10] S. Raoux, F. Xiong, M. Wuttig, E. Pop, *MRS Bull.* **2014**, *39*, 703.

[11] A. I. Khan, H. Kwon, R. Islam, C. Perez, M. E. Chen, M. Asheghi, K. E. Goodson, H.-S. P. Wong, E. Pop, *IEEE Electron Device Lett.* **2020**, *41*, 1657.

[12] J. Tang, D. Bishop, S. Kim, M. Copel, T. Gokmen, T. Todorov, S. Shin, K.-T. Lee, P. Solomon, K. Chan, W. Haensch, J. Rozen, in *2018 IEEE Int. Electron Devices Meeting (IEDM)*, IEEE, Piscataway, NJ, USA **2018**, <https://doi.org/10.1109/IEDM.2018.8614551>.

[13] D. Kuzum, R. G. D. Jeyasingh, B. Lee, H.-S. P. Wong, *Nano Lett.* **2012**, *12*, 2179.

[14] A. I. Khan, A. Daus, R. Islam, K. M. Neilson, H. R. Lee, H.-S. P. Wong, E. Pop, *Science* **2021**, *373*, 1243.

[15] C. Li, J. An, J. Y. Kweon, Y.-H. Song, *Jpn. J. Appl. Phys.* **2020**, *59*, SGGB07.

[16] I. Boybat, M. L. Gallo, S. R. Nandakumar, T. Moraitis, T. Parnell, T. Tuma, B. Rajendran, Y. Leblebici, A. Sebastian, E. Eleftheriou, *Nat. Commun.* **2018**, *9*, 2514.

[17] H. Kwon, A. I. Khan, C. Perez, M. Asheghi, E. Pop, K. E. Goodson, *Nano Lett.* **2021**, *21*, 5984.

[18] A. G. Kusne, H. Yu, C. Wu, H. Zhang, J. Hattrick-Simpers, B. DeCost, S. Sarker, C. Oses, C. Toher, S. Curtarolo, A. V. Davydov, R. Agarwal, L. A. Bendersky, M. Li, A. Mehta, I. Takeuchi, *Nat. Commun.* **2020**, *11*, 5966.

[19] A. I. Khan, H. Kwon, M. E. Chen, M. Asheghi, H.-S. P. Wong, K. E. Goodson, E. Pop, *IEEE Electron Device Lett.* **2022**, *43*, 204.

[20] A. I. Khan, X. Wu, C. Perez, B. Won, K. Kim, P. Ramesh, H. Kwon, M. C. Tung, Z. Lee, I.-K. Oh, K. Saraswat, M. Asheghi, K. E. Goodson, H.-S. P. Wong, E. Pop, *Nano Lett.* **2022**, *22*, 6285.

[21] J. Shen, S. Lv, X. Chen, T. Li, S. Zhang, Z. Song, M. Zhu, *ACS Appl. Mater. Interfaces* **2019**, *11*, 5336.

[22] G. C. Sosso, S. Caravati, R. Mazzarello, M. Bernasconi, *Phys. Rev. B* **2011**, *83*, 134201.

[23] R. De Bastian, E. Carria, S. Gibilisco, A. Mio, C. Bongiorno, F. Piccinelli, M. Bettinelli, A. R. Pennisi, M. G. Grimaldi, E. Rimini, *J. Appl. Phys.* **2010**, *107*, 113521.

[24] V. Bragaglia, K. Holldack, J. E. Boschker, F. Arciprete, E. Zallo, T. Flissikowski, R. Calarco, *Sci. Rep.* **2016**, *6*, 28560.

[25] F. Rao, Z. Song, Y. Cheng, X. Liu, M. Xia, W. Li, K. Ding, X. Feng, M. Zhu, S. Feng, *Nat. Commun.* **2015**, *6*, 10040.

[26] E. Yalon, S. Deshmukh, M. M. Rojo, F. Lian, C. M. Neumann, F. Xiong, E. Pop, *Sci. Rep.* **2017**, *7*, 15360.

[27] N. Yamada, E. Ohno, K. Nishiuchi, N. Akahira, M. Takao, *J. Appl. Phys.* **1991**, *69*, 2849.

[28] G. Ghosh, *J. Phase Equilib.* **1994**, *15*, 349.

[29] M. Suri, O. Bichler, D. Querlioz, O. Cueto, L. Perniola, V. Sousa, D. Vuillaume, C. Gamrat, B. DeSalvo, in *2011 Int. Electron Devices Meeting*, IEEE, New York City **2011**, pp. 4.4.1–4.4.4.

[30] Y. Li, Y. Zhong, L. Xu, J. Zhang, X. Xu, H. Sun, X. Miao, *Sci. Rep.* **2013**, *3*, 1619.

[31] S. X. Go, T. H. Lee, S. R. Elliott, N. Bajalovic, D. K. Loke, *APL Mater.* **2021**, *9*, 91103.

[32] D. Kuzum, R. G. D. Jeyasingh, H. -P. Wong, in *2011 Int. Electron Devices Meeting*, IEEE, Piscataway, NJ, USA **2011**, <https://doi.org/10.1109/IEDM.2011.6131643>.

[33] S. Braga, A. Sanasi, A. Cabrini, G. Torelli, *IEEE Trans. Electron Devices* **2010**, *57*, 2556.

[34] M. L. Gallo, A. Sebastian, *J. Phys. D: Appl. Phys.* **2020**, *53*, 213002.

[35] C. M. Neumann, K. L. Okabe, E. Yalon, R. W. Grady, H.-S. P. Wong, E. Pop, *Appl. Phys. Lett.* **2019**, *114*, 082103.

[36] W. Czubatyj, S. J. Hudgens, C. Dennison, C. Schell, T. Lowrey, *IEEE Electron Device Lett.* **2010**, *31*, 869.

[37] Q. Zheng, T. Guo, L. Chen, S. Song, X. Zhang, W. Yu, X. Zhu, H. Shao, W. Zheng, J. Zhang, *Mater. Lett.* **2019**, *241*, 148.

[38] Y. Xue, S. Song, S. Yan, T. Guo, L. Shen, L. Wu, Z. Song, S. Feng, *J. Alloys Compd.* **2017**, *727*, 1288.

[39] S. Kim, T. Todorov, M. Onen, T. Gokmen, D. Bishop, P. Solomon, K.-T. Lee, M. Copel, D. B. Farmer, J. A. Ott, T. Ando, H. Miyazoe, V. Narayanan, J. Rozen, in *2019 IEEE Int. Electron Devices Meeting (IEDM)*, IEEE, c **2019**, <https://doi.org/10.1109/IEDM19573.2019.8993463>.

[40] W. Chung, M. Si, P. D. Ye, in *2018 IEEE Int. Electron Devices Meeting (IEDM)*, IEEE, Piscataway, NJ, USA **2018**, <https://doi.org/10.1109/IEDM.2018.8614516>.

[41] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, W. Lu, *Nano Lett.* **2010**, *10*, 1297.

[42] S. Dutta, C. Schafer, J. Gomez, K. Ni, S. Joshi, S. Datta, *Front. Neurosci.* **2020**, *14*, 634.

[43] Y. Shi, L. Nguyen, S. Oh, X. Liu, F. Koushan, J. R. Jameson, D. Kuzum, *Nat. Commun.* **2018**, *9*, 5312.

[44] J. Woo, K. Moon, J. Song, S. Lee, M. Kwak, J. Park, H. Hwang, *IEEE Electron Device Lett.* **2016**, *37*, 994.

[45] X. Wu, A. I. Khan, P. Ramesh, C. Perez, K. Kim, Z. Lee, K. Saraswat, K. E. Goodson, H.-S. P. Wong, E. Pop, *IEEE Electron Device Lett.* **2022**, *43*, 1669.