A Fully-Integrated Direct-Conversion Resonant Switched Capacitor Converter with Modular Multi-Winding Current Ballasting

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Increasing needs for smaller form factor electronic systems motivate higher integration of power management circuits. This has led to growing interest in high-frequency DC-DC converters with smaller passive components [1-6]. Even though hybrid or resonant switched capacitor (ReSC) converters show promise, full integration of inductors remains challenging. At frequencies above 10 MHz, magnetic cores are typically impractical, and even with air-core magnetics, current crowding (skin and proximity) effects lead to high AC resistance. Past work has leveraged capacitive current ballasting with multi-trace 'merged LC resonators' to counteract AC current crowding and reduce high frequency loss [4]. However, the same concept has not been previously demonstrated with direct-conversion ReSC topologies which use lumped rather than distributed LC structures.

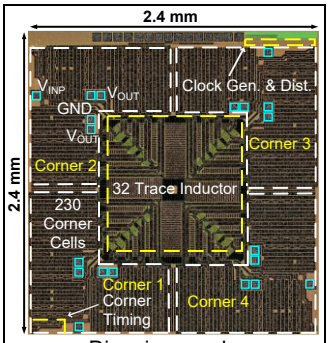
Shown in Fig. 1, this work uses direct-conversion ballasting where a nominally 2:1 SC stage is split into multiple (modular) units with each switching node V_{Xi} connected to a single trace of a multi-winding on-chip spiral inductor. Each SC stage presents a unique flying capacitance C_{Fi} to the given inductor trace. With each trace width smaller than the skin depth, the value for capacitance C_{Fi} can be set or tuned to force a desired current density profile which optimally goes inversely with trace resistance (or radius in spiral structures) [7]. Conceptually, capacitive ballasting manifests through voltage feedback in the LC structure: if current is too high, capacitor voltage increases to reduce current and vice versa. The difference between this work and the 'merged LC' approach in [4] is that here C_{Fi} is lumped and presented to the winding structure in discrete/modular direct-SC unit cells, thus it can be tuned or adjusted during operation. Direct conversion architectures have other advantages such as overall lower AC losses in magnetic components, improving inductor utilization.

Fig. 2 illustrates a portion of the spiral inductor and circuit interface. The inductor is 1mm^2 and uses 32 parallel traces with 11.5µm width and 2.5µm spacing. The 32 traces are split into 4 groups of 8 traces, each group being identical but rotated with taps at four corners of the structure. Each of the 8 traces (per group/corner) connects to a 2:1 SC stage with a unique flying capacitance C_{Fi}. The SC stages are constructed from identical 'unit cells.' Importantly, each unit cell has fixed flying capacitance C_F = 9.6pF and bypass capacitance C_{IO} and C_{OG} each 4.2pF, providing a local path for AC current flow.

To present a unique (optimal) capacitance C_{Fi} to each trace, different numbers n_i of unit cells are configured in parallel. Fig 2 tabulates the number n_i of unit cells per trace (out of 230 total/group) used for ballasting the current density profile. However, for LC resonant structures, capability for tuning is important to enable close-to-resonant operation, despite variations or deviation from simulation models. Fig. 3 further details the SC unit cell, showing modifications which allow for tunability. Notably, the design uses two categories of unit cells, fixed and tunable. Overall 80% of the cells are fixed, i.e., connected to only a single trace. The remaining 20% are tunable which enables the cell to be multiplexed between any two traces.

Overall, each unit cell is a self-sufficient converter with its own gate drivers (GD), boot-strapping (BS), level-shifting (LS), local flying and bypass capacitance and 1.2V-rated power devices. The GD input is generated from 2.5V digital logic, which is converted to 1.2V for the powertrain buffers. Bootstrapping uses a 2.5V NMOS switch to charge the 1.2V MOS bootstrap capacitor, C_{BS}. The GD and BS of the bottom power FETs M_1/M_2 are powered/bootstrapped from 1.2V system supply, V_{GG}. Devices M_3/M_4 are powered/bootstrapped from V_{IN}. LS control for M_3/M_4 uses an additional capacitive level shift with C_{CP} charge pump above V_{GG} and/or V_{IN}. While M_3 can, in principle, be driven directly from V_{IN}, a BS circuit is used as S&H to shield the gate from V_X voltage swing. Local anti-cross conduction precedes the GD/BS input circuit guarantee (local) non-overlapped clock phases to the power train from the main clock distribution network.

Timing circuitry uses a cascade of a ring voltage-controlled oscillator (VCO), frequency divider by factor of 4, and tunable dead-time generation as shown in Fig. 4. The 5-stage ring VCO uses current source degeneration for the second and third stage since these stages have the same but complementary sinking currents. Dead-time control is achieved by variable rise and fall times of differentially-paired current-starved inverters. This allows generation of both overlapping and non-overlapping clock phases in order to adjust for subsequent mismatches along the *extensive* clock distribution network to the unit cells.



Die micrograph.

Another benefit of the modular unit cell approach is in the layout and routing of the power train signals. Fig. 4 shows the floorplan of a unit cells which has both horizontal and vertical mirror symmetry. This helps in sharing power train signals by placing the cells in the matrix form as depicted and to reduce routing overheads.

The design is fabricated in 130nm RF SOI CMOS process with active area 5.5 mm^2. The die micrograph is shown above. Flying and bypass capacitors are realized using MOS capacitors with instantiated density ~9.1nF/mm^2. Fig. 5 shows measurement results. Peak efficiency is 84.7%, operating at 24MHz resonant frequency for V_{IN} from 2.25-2.75V. Note that direct-ReSC architectures can operate above resonance; here the design achieves peak current density of ~100mA/mm^2 at 44MHz with ~75% efficiency. Measured output resistance, R_{EFF} is ~ 550mΩ for load current from 50 – 925mA. With only on-chip bypass capacitance output ripple can be significant; however with modest (~100nF) off-chip or load-embedded C_{OUT}, output ripple is significantly reduced due to high-frequency operation.

Fig. 6 compares this work with current state-of-the-art designs. Important differences include that this work achieves 2X-3X lower R_{EFF} due to improved current ballasting (achieves lower ESR in magnetics). While efficiency and power density are comparable to [3], [4], this work uses only MOS capacitors, smaller die area, and higher peak current. Thus favorable benefits of this approach include improved utilization of on-chip magnetics leading to lower conduction loss and higher output current density. The other main contribution is a modular design/layout approach (standard switching cells + tunability) that is scalable for different application specs with the potential for partial synthesis and design automation. Thus this design provides a roadmap and suitable implementation strategy for future designs in advanced process nodes.

Acknowledgment:

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References:

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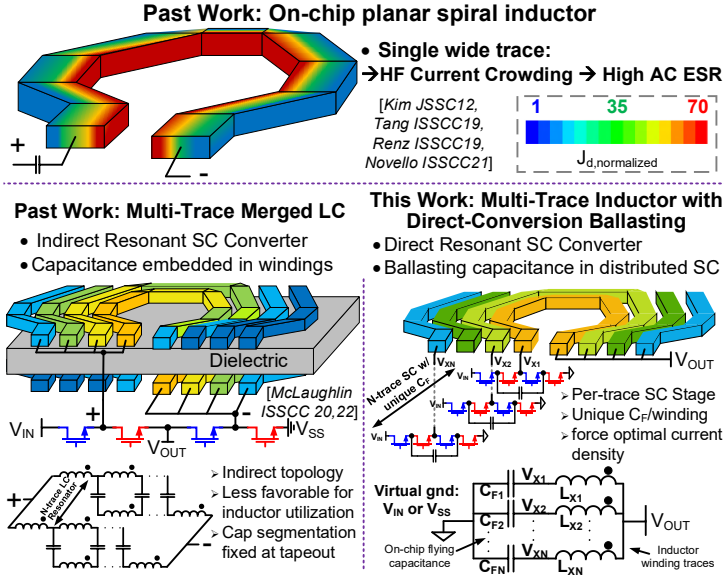
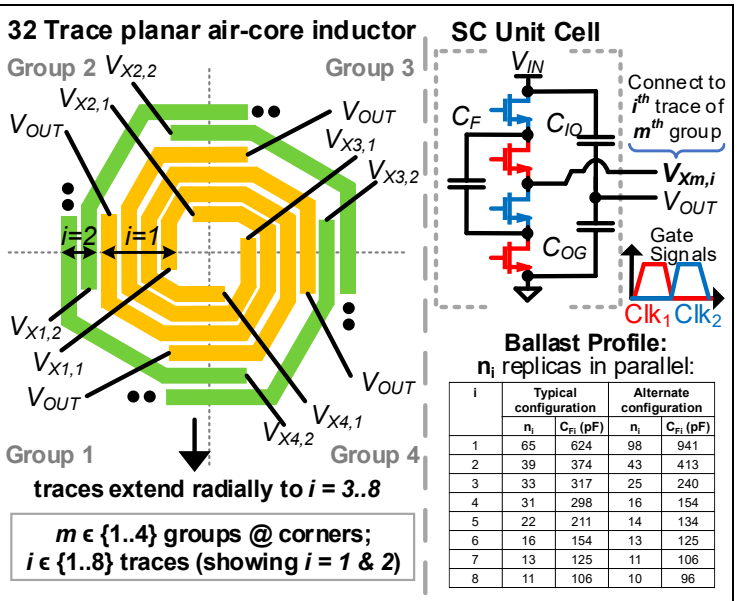


Fig. 1. Topology overview and comparison to past work.



i	Typical configuration		Alternate configuration	
	n_i	C_{Fi} (pF)	n_i	C_{Fi} (pF)
1	65	624	98	941
2	39	374	43	413
3	33	317	25	240
4	31	298	16	154
5	22	211	14	134
6	16	154	13	125
7	13	125	11	106
8	11	106	10	96

Fig. 2. Architecture implementation and multi-trace winding layout.

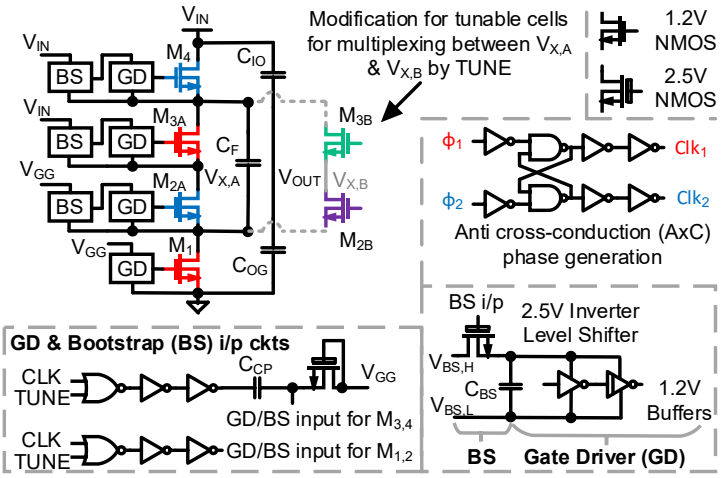


Fig. 3. Schematic design of individual switched capacitor unit cell.

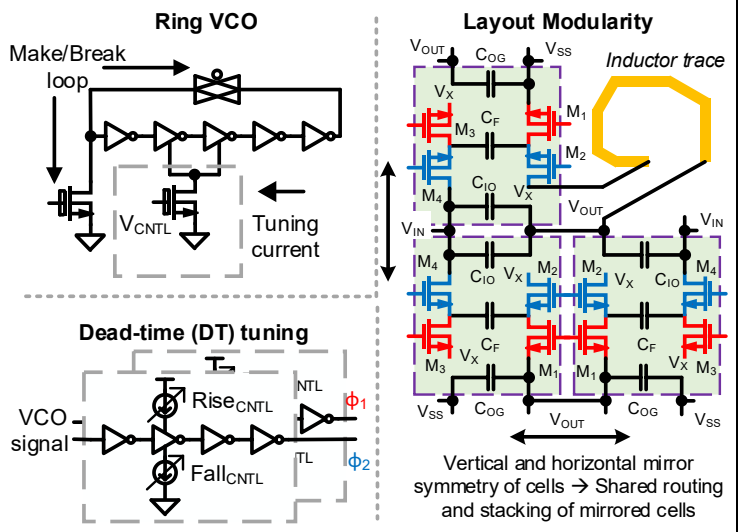


Fig. 4. Timing generation details and layout strategy.

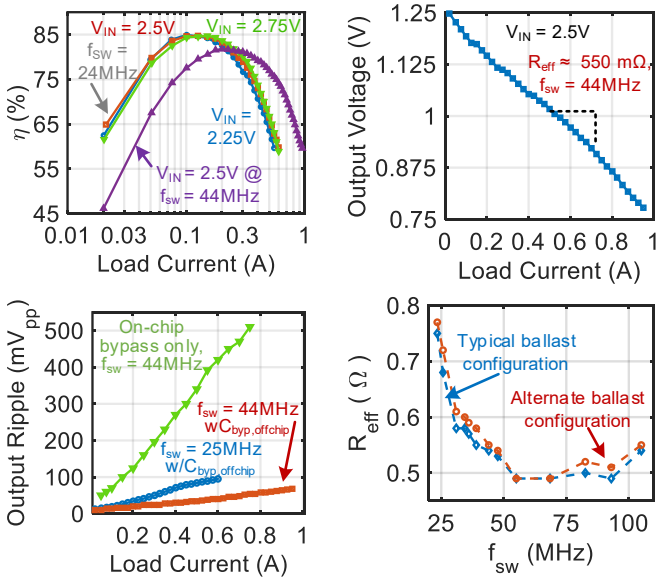


Fig. 5. Measurement results.

	Kim JSSC12	Tang ISSCC19	Renz ISSCC19	McLaughlin ISSCC20	Novello ISSCC21	McLaughlin ISSCC22	This Work
Topology	3-Level	SIC	ReSC	ReSC	Class-D LC	ReSC	ReSC
V_{in} (V)	2.4	1.2	3.0 – 4.5	2.4 – 4.4	1 – 3.6	3.3 – 6.6	2.25 – 2.75
V_{out} (V)	0.4 – 1.4	0.6 – 0.9	1.5 – 1.8	1.0 – 2.2	0.4 – 1.6	0.8 – 2.2	0.7 – 1.39
Technology	130nm CMOS	65nm CMOS	130nm BCD	180nm CMOS	180nm CMOS	180nm CMOS	130nm RF SOI
f_{sw} (MHz)	50 – 240	450	35.5	47.5	1250	30	24 – 45
C_{fly} (nF)	18	1.72	2	3.4	0.46	5.4	9
C_{in} (nF)	NR	NR	0.18 + off chip	7	0	4.2	4.2
C_{out} (nF)	10	3.1	10	7	0	5.8	4.2
η_{pk} (%) @ I_{den} (A/mm²)	77 @ 0.06	64 @ 0.369†	85 @ 0.015	85.5 @ 0.025	67 @ NR	78.3 @ 0.013	84.7 @ 0.028
$I_{den,pk}$ (A/mm²) @ η (%) @ P_{out} (W)	0.16 @ 63 @ 1	0.708 @ 52 @ 0.276†	0.015 @ 85 @ 0.22	0.058 @ 74.5 @ 0.868	NR	0.056 @ 61 @ 0.67	0.105 @ 75.0 @ 0.542
I_{PK} (A)	0.8	0.533	0.12	0.52	NR	0.49	0.925
R_{eff} (Ω)**	NR	NR	0.833*	1.24	> 1.3*	1.5	0.550
Area (mm²)	5	0.65	7.83	8.93	1.61	8.7	5.5

*Estimated, **Reported where I_{PK} is achieved, †Here reporting at 2:1 conversion to match other works in comparison

Fig. 6. Comparison table with state-of-the-art works.