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State-Space Modeling and Control of Flying-Capacitor Multilevel DC-DC Converters

Ziyu Xia*, *Graduate Student Member, IEEE,* Kishalay Datta*, *Graduate Student Member, IEEE,* and Jason T. Stauth, *Member, IEEE*

***Abstract*—Hybrid and resonant switched capacitor converters show promise in a number of power management applications, but are subject to a range of challenges in control and implementation. In particular, hybrid topologies use a network of switched flying capacitors to reduce voltage stress on switching devices and energy storage requirements of inductor(s). However the increased order of system dynamics can lead to problems with voltage balance and regulation of the unique flying capacitor voltage states, leading to higher voltage stress and other undesirable effects. This work presents a simple yet comprehensive state-space analysis of hybrid topologies which can be used to predict and control system dynamics including voltage imbalance phenomena. The model affords new perspectives on modern-control metrics through a condition-number-based treatment, providing relative quantification of observability and controllability. Expanded opportunities such as a state observer and discrete time eigenvalues which govern natural balance are presented. The model is exemplified and validated using flying-capacitor multilevel converter (FCML) hardware prototypes.[1]**

***Index Terms*—hybrid switched-capacitor, capacitor voltage balance, flying capacitor multilevel converter, DC-DC converter.**

I. Introduction

POWER management and delivery is an increasing bottleneck in a variety of applications spanning performance and mobile computing, renewable energy, electrified transportation, low-power embedded systems, and many others [3]. In pursuit of high efficiency, small volume, and flexible regulation, hybrid switched-capacitor (SC) converters have emerged as promising candidates for such applications [4]–[8]. By incorporating capacitors and inductors as energy storage elements, hybrid converters combine advantages of both magnetic-based and pure SC topologies: the inductor(s) achieve soft charging of flying capacitors and enable efficient regulation characteristics [9]–[12]; the capacitors boost average energy density of passive components thus reducing the overall physical volume [13]–[15].

While many hybrid SC converter topologies are explored in the literature [6]–[8], [16]–[24], they can generally be segmented into base classes spanning series-parallel, Dickson, ladder, Fibonacci, and flying capacitor multilevel (FCML) [14], the latter illustrated for a 4-cell ($N = 4$) converter in Fig. 1. The direct-conversion architectures have a defining characteristic that an inductor is connected between a switching node and the output terminal [11] and can be operated in resonant or pulse-width modulated (inductive) modes [12].

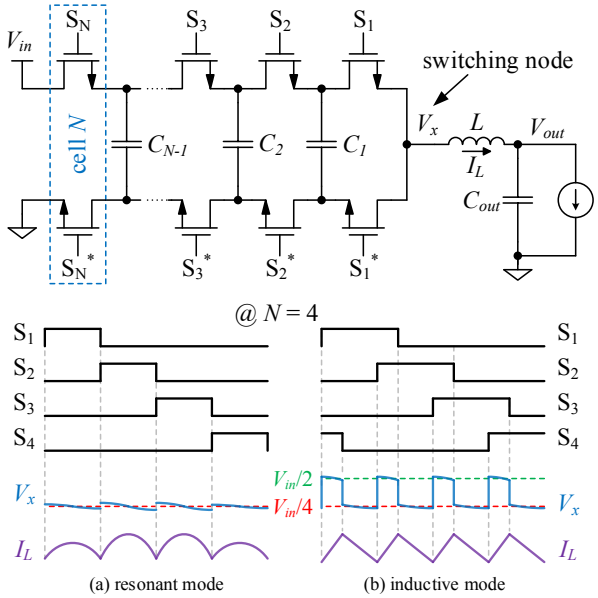

Fig. 1. The general schematic of an N-cell FCML converter; $4-$cell FCML converter timing diagrams under (a) resonant and (b) inductive modes.

Compared to a conventional buck converter with a 2nd-order LC filter, hybrid converters can have much higher order dynamics due to the additional *independent energy storage* of flying capacitors. This results in a practical challenge of maintaining flying capacitor voltages at a desired or nominal 'balanced' level [24]–[28]. Many topologies can achieve *natural balance*, leveraging intrinsic passive feedback to drive flying capacitor voltages to their balanced values [24]–[30]. However, its strength and effectiveness depends on circuit parameters, converter operating conditions, and non-idealities [29]–[32]. In the presence of external disturbances, flying capacitor voltages may drift away from nominal values, resulting in imbalance, causing increased ripple and switch voltage stress [33]. Therefore, it is important to understand flying capacitor voltage dynamics and identify scenarios where natural balance is weak or even fails.

In scenarios where transient response is important or natural balance is too weak, active control is often required to regulate

[1]This work is an extension of conference papers [1] "State space analysis of flying capacitor multilevel dc-dc converters for capacitor voltage estimation," IEEE Applied Power Electronics Conference (APEC) 2019, and [2] "Natural balancing of flying capacitor multilevel converters at nominal conversion ratios" IEEE Workshop on Control and Modeling for Power Electronics (COMPEL) 2019. This work was funded in part by the National Science Foundation under grant numbers ECCS 1554265 (CAREER) and IIP 1822140 through the NSF Power Management Integration Center (PMIC) Industry/University Cooperative Research Center (I/UCRC). *The two first authors contributed equally to this work.

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flying capacitor voltages. Current-mode control achieves balance by aligning the inductor valley or peak current [34], [35], with its variations further improving stability and transient response [36]–[39]. However, high-bandwidth current sensing is often difficult or impractical. Voltage-mode algorithms, which don't require current sensing, have also been explored. These include time-domain feedback based on switching node sampling [40], phase-shift or linear compensation control [41]–[43], nonlinear control methods based on ripple-injection hysteretic controllers [19], [44], threshold-based voltage-mode controllers [6], [45], and sensorless methods [46].

This paper extends previous work in [1], [2], generalizing the state-space (SS) model for hybrid SC converters. Compared to [1], [2] which primarily treated operation at resonant or nominal conversion ratio levels, here we expand to better capture dynamics in pulse-width modulated (inductive) operation. The state-space model is modified to capture the admixture of dynamics when a converter is duty cycled between adjacent levels. This allows a broader perspective on the modern control metrics of observability and controlability by using the linear algebraic concept of *'condition number'* to provide a relative quantification of these metrics across conversion ratios. We also refine and generalize the passive feedback model in [2] to illustrate the relationship between controllability and natural balance.

While the model can be applied to other topologies, here we provide examples based on flying capacitor multilevel (FCML) converters, which have more complex balancing dynamics than other topologies. Various aspects of the analysis are verified in FCML hardare prototypes. A state observer for FCML flying capacitor voltages is presented which achieves similar resolution but over 2× faster settling than the example in [1]. Measurement results are compared to model predictions to illustrate the limitations of natural balance.

II. Discrete-Time State Space Model

In this section, a discrete-time state space model is developed to analyze direct-conversion hybrid SC converters and explore fundamental principles that govern flying capacitor voltage dynamics. As illustrated in Fig. 2, the general form of a step-down, direct-conversion hybrid SC converter comprises a switched-capacitor stage, where semiconductor switches are used to reconfigure a network of flying capacitors, and a single inductor, which connects the SC stage to the output terminal. This architecture can be intuitively treated as two subsystems: the SC stage and the output filter stage. The switching node voltage, V_x, is modeled as the output signal of SC stage and the input signal of output filter stage; the charge transferred through the inductor, q, is modeled as the output signal of output filter stage and the input signal of SC stage.

A. Flying Capacitor Multilevel Converters

The general schematic of a FCML converter, shown in Fig. 1, will be used as an example to derive and apply the model. FCML converters comprise N commutation cells, each of which includes two complementary switches. While many naming systems exist in the literature, an N-cell FCML converter is equivalent to an (N+1)-level converter, and has N-1 flying capacitors between adjacent cells. In each phase, the states of switching cells configure flying capacitors to be charged, discharged, or remain idle, leading to one of the N+1 possible voltage levels at the switching node: $n/N \times V_{in}$ ($n = 0, 1, 2, \cdots, N$). The switching node voltage, V_x, is averaged by the output filter to give output voltage V_{out}.

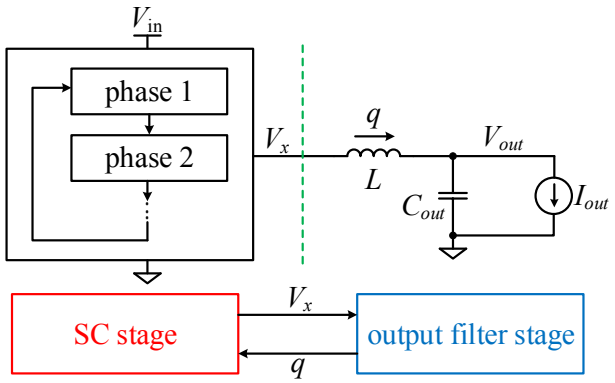

Fig. 2. A direct hybrid SC converter treated as two subsystems.

A common way to operate FCML converters is phase-shifted pulse width modulation (PSPWM) [25], [47], where all cells share the same duty cycle, D, but cell j ($j = 1, 2, \cdots, N$) is phase shifted by (j -1)/N×360°. The output voltage is given by the product of the duty cycle and the input voltage, DV_{in}. While the duty cycle may be any value between 0 and 1, it can be normalized to the following form:

$$D = \frac{m}{N}, \tag{1}$$

where the denominator equals the number of cells, N; the numerator obtained from this normalization is denoted as m. If m is not an integer, V_x alternates between two neighboring voltage levels, resembling a square wave; this scenario is hereby called *inductive-mode* operation. In the special cases where m is an integer, V_x remains at one voltage level through the whole period, leading to sinusoidal characteristics of the inductor current; this scenario is hereby referred to as *resonant-mode* operation [12]. The two operating modes are illustrated in Fig. 1 using a 4-cell example.

However, the above operation puts specific requirements on flying capacitors: for capacitor C_i ($i = 1, 2, \cdots, N$-1), its *'average'* voltage should be $i/N \times V_{in}$, here defined as the balanced voltage. The term *'average'* may have more than one possible interpretation, but for the switches to have minimum voltage stress, it should be *the algebraic average of the initial and final voltage during a switching phase that the capacitor is either being charged or discharged.* If flying capacitors become imbalanced, ripple quantities and switch voltage stress will increase, degrading efficiency and reliability [29]–[32].

B. Switched-Capacitor Stage State-Space Model

In the SC stage, flying capacitor voltages (and their configuration in a given state) determine the switching node voltage V_x, however these voltages are influenced by charge transfer

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due to current flow in the inductor. Derivation of the state-space (SS) model involves defining and quantifying these relationships in matrix form. Past work provides examples for constructing the state equation for in resonant mode at nominal conversion ratios: a 5-cell converter at $D = 2/5$ in [1] and a 4-cell converter at $D = 2/4$ in [2]. However, here we generalize the model to consider non-integer fraction duty cycles across the full range of resonant and inductive modes of operation.

The following assumptions are made for the derivation of discrete-time (DT) SS model of the FCML converter:

1) The circuit is linear in each phase.
2) Capacitor voltages (and inductor current) are continuous *i.e.,* the final condition in a given phase is the same as the initial condition of the next phase.
3) For simplicity, here we assume all flying capacitors have the same capacitance C_f.[2]

In nominal resonant-mode operation, there are N distinct phases and each flying capacitor is charged and discharged once in a switching period. In the more generic inductive-mode case, the FCML converter may multiplex between two neighbouring nominal conversion ratio levels [25], thus the converter has $2N$ distinct switching phases ($j = 1 \dots 2N$) in each converter period [2], [10]. To treat the general inductive mode operation where V_x is duty cycled between levels, we decompose m from (1) as,

$$m = m_{nom} + m_{frac}, \tag{2}$$

where, $m_{nom} < m$ is an integer corresponding to nearest nominal conversion ratio level and $0 \leq m_{frac} \leq 1$ corresponds to the extra fractional contribution to the duty-cycle. For example, if $m = 1.3$, then $m_{nom} = 1$ and $m_{frac} = 0.3$. The converter operates in the m_{nom}/N and $(m_{nom}+1)/N$ mode for $(1-m_{frac})$ and m_{frac} fractions of a single switching period respectively. Further discussion and and example of this concept are provided in Appendix A.

1) State Equation Model: To generalize the state-space model for inductive-mode duty cycles given (2), we modify the matrix construction in [1] to consider (up to) $2N$ charge quantities in a given converter period k. Similar to [1], each charge quantity $q_j(k)$ represents the integral of inductor current across the j^{th} switching phase.[3] For the i^{th} capacitor C_i, its initial voltage in period k is defined as $V_{Ci}(k)$; its final value, or initial value in period $k+1$, is $V_{Ci}(k+1) = V_{Ci}(k)+q(k)/C_f$ where $q(k)$ is total charge flow in the capacitor in period k. With these definitions, the initial value of final flying capacitor voltages in period $k+1$ can be packed in matrix form:

$$\begin{bmatrix} V_{C1}(k+1) \\ \vdots \\ V_{CN-1}(k+1) \end{bmatrix} = \begin{bmatrix} V_{C1}(k) \\ \vdots \\ V_{CN-1}(k) \end{bmatrix} + (\frac{1}{C_f})\boldsymbol{B_{con}}\boldsymbol{M_{con}} \begin{bmatrix} q_1(k) \\ \vdots \\ q_{2N}(k) \end{bmatrix}, \tag{3}$$

where,

$$\boldsymbol{M_{con}} = \begin{bmatrix} (1-m_{frac})\boldsymbol{I_N} & \boldsymbol{0_{N\times N}} \\ \boldsymbol{0_{N\times N}} & m_{frac}\boldsymbol{I_N} \end{bmatrix}. \tag{4}$$

In (4), $\boldsymbol{I_N}$ is the N^{th} order identity matrix; $\boldsymbol{B_{con}}$ and $\boldsymbol{M_{con}}$ are respectively termed the *state connection matrix* and *fractional duty cycle matrix*. Matrix $\boldsymbol{B_{con}}$ is used to define which capacitors are connected (and the polarity of charge flow) in each switching phase j for converter period k. Matrix $\boldsymbol{M_{con}}$ formalizes (2), and splits charge flow based on the fractional duty cycle. Thus (3) represents the state equation for the switched capacitor stage, which can be more compactly and formally expressed as:

$$\boldsymbol{V_C}(k+1) = \boldsymbol{A}\cdot\boldsymbol{V_C}(k) + \boldsymbol{B}\cdot\boldsymbol{q}(k), \tag{5}$$

where $\boldsymbol{A} = \boldsymbol{I_{N-1}}$ is the identity matrix. However, different from the pure resonant treatment in [1] and [2], the expanded formulation $\boldsymbol{B} = (1/C_f)\boldsymbol{B_{con}}\boldsymbol{M_{con}}$ captures the impact of charge flow vector $\boldsymbol{q}(k)$ on flying capacitor voltages for each of the up to $2N$ switching states for non-integer fractional duty cycles. An example for the construction of $\boldsymbol{B}$ based on $\boldsymbol{B_{con}}$ and $\boldsymbol{M_{con}}$ for an inductive-mode $4-$cell converter with $D = 1.3/4$ is provided in Appendix B for reference.

2) Output Equation Model: Illustrated in Fig. (2) it is also important to characterize the switching node V_x, which is here treated as the output of the SC stage. Based on Kirchhoff's voltage law (KVL), V_x is calculated by linear combinations of flying capacitor voltages and input voltage V_{in}. However, charge flow through the flying capacitor network is also considered as this impacts capacitor voltages in converter period k. This is formulated as the SC-stage output equation:

$$\boldsymbol{V_x}(k) = \boldsymbol{C}\cdot\boldsymbol{V_C}(k) + \boldsymbol{D}\cdot\boldsymbol{q}(k) + \boldsymbol{W_1}\cdot V_{in}. \tag{6}$$

Due to symmetry with (3), it can be shown that $\boldsymbol{C} = -\boldsymbol{B_{con}^T}$, where $\boldsymbol{C}$ is here termed the *output connection matrix*, following similar terminology in [10], [48]. A further modification from [1], [2] is that here we solve for the final value of switching node voltages $\boldsymbol{V_x}(k)$ rather than initial voltages. Even though $\boldsymbol{V_x}(k)$ may be treated as sampled at any point during the phase, this leads to a simpler construction of $\boldsymbol{D}$ and does not otherwise change the analysis or conclusions. Vector $\boldsymbol{W_1}$ captures which of the switching phases $j \in (1 \dots 2N)$ input voltage V_{in} is needed to determine V_x. More details on the output equation and matrix construction are shown in Appendix B; for the convenience of the interested reader, the MATLAB function to generate the required matrices for the SS model of a generic m/N FCML converter is also provided.

[2]Note that while is not always practical or achievable to have the same C_f for all capacitors (due to voltage derating and other factors), this and other non-idealities can be captured in the SS model (see [1] and [48]); we do not include them here to minimize complexity of notation.

[3]For now, exact details of the inductor current waveform (and its integral, q_j) are not needed; however we will return to treat q_j in the discussion of passive feedback and natural balance.

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III. Observability and Controllability of Flying Capacitor Voltages

Here we explore the key modern control metrics of observability and controllability. As defined here, observability describes whether the switching node voltage V_x contains enough information to uniquely determine (or estimate) flying capacitor voltages. Controllability describes whether charge transferred through the inductor can arbitrarily adjust flying capacitor voltages. The state space model of the SC stage is reproduced below from (5) and (6) for convenience:

$$\begin{aligned}\boldsymbol{V_C}(k+1) &= \boldsymbol{A}\cdot\boldsymbol{V_C}(k) + \boldsymbol{B}\cdot\boldsymbol{q}(k),\\ \boldsymbol{V_x}(k) &= \boldsymbol{C}\cdot\boldsymbol{V_C}(k) + \boldsymbol{D}\cdot\boldsymbol{q}(k) + \boldsymbol{W_1}\cdot V_{in}.\end{aligned}$$

A. The Criteria

Following modern control conventions [49], the observability matrix for the SC stage can be constructed as:

$$\boldsymbol{\mathcal{O}} = \begin{bmatrix}\boldsymbol{C} & \boldsymbol{CA} & \dots & \boldsymbol{CA}^{N-2}\end{bmatrix}^T. \tag{7}$$

Noting that $\boldsymbol{A}$ is the identity matrix, it can be simplified to

$$\boldsymbol{\mathcal{O}} = \begin{bmatrix}\boldsymbol{C} & \boldsymbol{C} & \dots & \boldsymbol{C}\end{bmatrix}^T, \tag{8}$$

showing that $\boldsymbol{\mathcal{O}}$ is the vertical expansion of $\boldsymbol{C}$. Since $\boldsymbol{C}$ has more rows than columns, this expansion does not affect the rank. The observability criteria for the SC stage is rank($\boldsymbol{C}$) equal to the number of flying capacitors, or

$$\text{rank}(\boldsymbol{C}) = N-1. \tag{9}$$

Similarly, the controllability matrix is expressed as:

$$\boldsymbol{\mathcal{C}} = \begin{bmatrix}\boldsymbol{B} & \boldsymbol{AB} & \cdots & \boldsymbol{A}^{N-2}\boldsymbol{B}\end{bmatrix}, \tag{10}$$

where, since $\boldsymbol{A}$ is the identity matrix, it reduces to

$$\boldsymbol{\mathcal{C}} = \begin{bmatrix}\boldsymbol{B} & \boldsymbol{B} & \cdots & \boldsymbol{B}\end{bmatrix}. \tag{11}$$

This expansion does not affect the rank either, as $\boldsymbol{B}$ has more columns than rows. The controllability criteria is given by rank($\boldsymbol{B}$) is equal to the number of flying capacitors, or,

$$\text{rank}(\boldsymbol{B}) = N-1. \tag{12}$$

Here we note that $\boldsymbol{B}$ and $\boldsymbol{C}$ must have the same rank. This is because they have a scaled transpose relationship, i.e. $\boldsymbol{B} = -(1/C_f)\cdot\boldsymbol{C^T}\cdot\boldsymbol{M_{con}}$. Essentially, in inductive-mode cases $\boldsymbol{M_{con}}$ is a full rank diagonal matrix. In resonant-mode cases, $m_{frac} = 0$. The construction in (3) can still be used but due to the reduced order of $\boldsymbol{B}$, the model becomes equivalent to the construction in [1]. In either case, it is true that rank($\boldsymbol{B}$) = rank($\boldsymbol{C}$). Thus is can be summarized that *the SC stage is observable and controllable if and only if $\boldsymbol{C}$ (or $\boldsymbol{B}$) has rank equal to the number $(N-1)$ of flying capacitors*.

Simplifying this determination, matrix $\boldsymbol{C}$ can be conveniently obtained without using KVL by noting the following patterns for the j^{th} row and i^{th} column element, c_{ji}:

$$c_{ji} = \begin{cases} -1 & \text{capacitor } C_i \text{ is charged in phase } j,\\ 0 & \text{capacitor } C_i \text{ is idling in phase } j,\\ 1 & \text{capacitor } C_i \text{ is discharged in phase } j.\end{cases} \tag{13}$$

This allows writing the connection matrix directly from the equivalent circuits of a hybrid SC converter. Observability and controllability of its SC stage can then be determined.

Specifically for an N-cell FCML converter with $D = m/N$, Appendix C proves that the SC stage is observable and controllable except the case where m and N are integers whose greatest common factor is larger than one (i.e., m and N are not coprime). While this is a relatively simple proof, it aligns with previous literature on natural balance in FCML converters [29]–[32] and is summarized in Table I.

TABLE I
Controllability and observability of the SC stage for an N-cell FCML converter with $D = m/N$.

	resonant mode (integer m)		inductive mode (non-integer m)
	m, N coprime	not coprime	
observable	✓	×	✓
controllable	✓	×	✓

B. Relative Controllability based on Condition Number

While useful in principle, the binary nature ($true$ or $false$) of the controllability metric does not offer much insight into the degree of controllability of a converter. Specifically, while operating in an inductive mode which is in the neighborhood of an uncontrollable conversion ratio level, intuitively we should expect the converter to be difficult to control. This raises the need for an analog or quantitative measure of controllability. For a general switching mode converter, [50] suggests an interesting sensitivity function-based approach to analyze open-loop converters near uncontrollable scenarios. However, as of now, it has been shown for certain case-by-case transient responses.

Here we provide a more quantifiable measure based on a robust and well-established concept developed for numerical computation used in linear algebra known as the *condition number* [49], [51], [52]. Condition number, $\kappa(\boldsymbol{\alpha})$, gives *a numerical measure of how full-rank is a matrix,* $\boldsymbol{\alpha}$, such that,

$$1 \le \kappa(\boldsymbol{\alpha}) = \frac{\sigma_{max}}{\sigma_{min}} < \infty. \tag{14}$$

In (14), σ_{min} and σ_{max} are the minimum and maximum singular values of $\boldsymbol{\alpha}$ obtained from its *Singular Value Decomposition* (SVD) [51], [52]. The closer $\kappa(\boldsymbol{\alpha})$ is to unity, the more *well-conditioned* or full-rank is $\boldsymbol{\alpha}$.

To provide an intuitive understanding of $\kappa(\boldsymbol{\alpha})$, we use it in the example of solving a linear equation of two variables. Suppose we wish to solve the equation,

$$\boldsymbol{\alpha}\cdot\mathbf{x} = \begin{bmatrix}\alpha_{11} & \alpha_{12}\\ \alpha_{21} & \alpha_{22}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} = \begin{bmatrix}b_1\\ b_2\end{bmatrix}.$$

Consider two different scenarios:

- $\alpha_{11} = \alpha_{22} = 1$, $\alpha_{12} = \alpha_{21} = 0$ and $b_1 = 1$, $b_2 = 2$. Then we get, $x_1 = 1$, $x_2 = 2$ and $\kappa(\boldsymbol{\alpha}) = 1$.
- For $\alpha_{11} = 1, \alpha_{12} = 0.99, \alpha_{21} = 1.01$, and $\alpha_{22} = 1$ with $b_1 = 1$, $b_2 = 2$, we get, $x_1 = -9.8\times10^3$, $x_2 = 9.9\times10^3$ and $\kappa(\boldsymbol{\alpha}) = 4\times10^4$.

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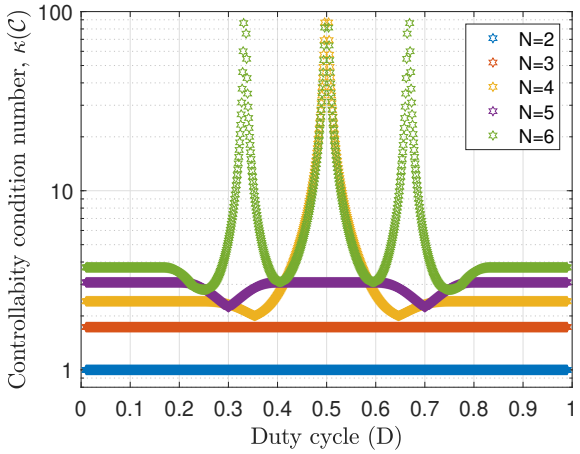

Fig. 3. Condition number of the controllability matrix $\mathcal{C}$ versus duty cycle for FCML converters with PSPWM (lower is more controllable).

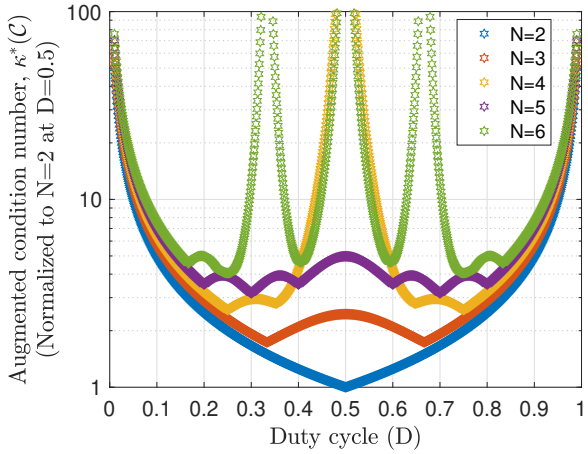

Fig. 4. Augmented condition number of the controllabilty matrix $\mathcal{C}$ versus duty cycle for FCML converters with PSPWM (lower is more controllable).

The above cases show how relative solution magnitudes diverge and the sensitivity to slight parameter differences (or systematic errors) grow with increasing condition number. So, even though both versions of $\boldsymbol{\alpha}$ are full-rank, the appropriate value of $\boldsymbol{x}$ starts to become unbounded with a $\kappa(\boldsymbol{\alpha})$ much greater than unity. Thus increasing magnitude of $\kappa(\boldsymbol{\alpha})$ indicates how unsolvable the system is. As $\kappa(\boldsymbol{\alpha}) \to \infty$, the system is unsolvable since $\boldsymbol{\alpha}$ is no longer full-rank.

This concept can be applied to hybrid SC converters to quantify the relative difficulty of achieving flying capacitor balance, especially in regimes near known uncontrollable conversion ratio levels. For example, Fig. 3 plots the condition number of the controllability matrix $\kappa(\mathcal{C})$ for FCML converter examples with $N = 2, 3, 4, 5, 6$ across different duty cycles.[4] Duty cycles where $\kappa(\mathcal{C})$ is closer to unity (lower magnitude) are correspondingly *'more controllable'* (easier to balance). However, where $\kappa(\mathcal{C})$ starts becoming unbounded, we can conclude the converter is becoming increasingly uncontrollable.

As seen in Fig. 3, $\kappa(\mathcal{C})$ starts to becomes unbounded near duty-cycles where m and N are not co-prime. For example, for $N = 4$ (5-level) and $N = 6$ (7-level) converters, the condition number becomes unbounded at duty cycles of $D = 2/4$ and $D = 2/6, 3/6$, and $4/6$ respectively. More importantly, $\kappa(\mathcal{C})$ helps to quantify which converters and ranges of duty-cycles are fundamentally difficult to control. For example, an interesting observation seen in Fig. 3 is that higher order (increasing N) FCML converters have generally higher values of $\kappa(\mathcal{C})$. This aligns with intuition: *as the number of flying capacitors increases, it is more difficult to achieve balance*. Such can be compared to the $N = 2$ (3-level) case which has $\kappa(\mathcal{C}) = 1$ for all D, i.e. the 3-level converter has the highest degree of controllability as it has only a single flying capacitor.

An important point to note is that at the extreme duty cycles of $D = 0$ and $D = 1$, $\kappa(\mathcal{C})$ is, in fact, unbounded. This is because at these extreme duty cycles, flying capacitors are not connected to the switching node and can't be controlled. However, in the neighborhood of $D = 0$ and $D = 1$, $\kappa(\mathcal{C})$ is still finite. The reason behind this is that the controllability matrices approach null matrices at $D \to 0$ and $D \to 1$. Hence, both the maximum singular value (σ_{max}) and minimum singular value (σ_{min}) are very small but their ratio, *i.e.,* $\kappa(\mathcal{C})$ is still finite. This indicates the limitation of condition number near these extreme duty cycles and does not correlate with closed-loop performance and practical data.

To circumvent this, we use another metric whose construction is similar to the condition number but conveys better controllabilty information across the full duty cycle range. We term this the augmented condition number:[5]

$$\kappa^*(\mathcal{C}) = \frac{\kappa(\mathcal{C})}{\sigma_{min}}. \tag{15}$$

The intuition behind defining this is as follows. Fundamentally a matrix would become ill-conditioned once its σ_{min} starts to diminish or $1/\sigma_{min}$ tends to be unbounded. Hence, the product of $\kappa(\mathcal{C})$ and $1/\sigma_{min}$ at non-extreme duty cycles would be similar to just $\kappa(\mathcal{C})$ while the extreme cases would be represented by the $1/\sigma_{min}$ term. Fig. 4 (a) shows the plot of $\kappa^*(\mathcal{C})$ with the same conditions as Fig. 3, where the curves become unbounded near all the duty-cycle ranges where the practical data show the converter to be uncontrollable. The correlation of this metric with closed-loop performance will become more clear in Section IV.

Another point to clarify is that augmented condition number $\kappa^*(\mathcal{C})$ is only a *proxy for the degree of controllability,* i.e. it describes the *relative control effort* needed in an ideal state-feedback control system. However, the actual closed loop system performance will depend also on the nature and dynamics of the associated controller. For example, it is known in the literature that even- and odd-level FCML converters

[4]Specific details of computing $\kappa(\mathcal{C})$ are not provided here as this is based on a well-known mathematical framework [49]; however an interested reader can replicate Fig. 3 using the *svd* command in *MATLAB* for relevant $\boldsymbol{B}$ matrix and computing $\kappa(\mathcal{C})$ using (14).

[5]Note from (3) that $\mathcal{C}$ is scaled by $1/C_{\mathrm{f}}$ in (11); thus (15) is more appropriately expressed as $\kappa^*(\mathcal{C}) = \kappa(\mathcal{C})/(\sigma_{min} \cdot C_f)$; we drop the C_f scaling in (11) to have a simpler expression and because the augmented condition number is only appropriate when used as a relative metric, i.e. the normalized perspective in Fig. 4.

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have different natural balance performance – even-level (odd-N) converters being better in terms of settling time, rejection of disturbances, etc [2], [31]. This results from the unique dynamics of the closed-loop passive feedback established in natural balance scenarios and can not be inferred directly from $\kappa^*(\boldsymbol{\mathcal{C}})$. This concept is explored in Section IV.

Expanding on the concept, a key contribution of [2] was that for FCML converters with uncontrollable (or unobservable) duty cycles, it is possible to modify the switching sequence in order to make the SC network controllable (and observable). The concept, called *modified PSPWM* adds switching states between the traditional PSPWM phases, in order to gain unique access to otherwise hidden or uncontrollable flying capacitor voltages. Effectively this makes the controllability matrix $\boldsymbol{\mathcal{C}}$ become full rank where it otherwise would not.

An example of the modified PSPWM sequence for an $N = 4-$cell converter at $D = 2/4$ is provided in [2] and is not further replicated here. However, to illustrate the augmented condition number concept applied to this case, we plot $\kappa^*(\boldsymbol{\mathcal{C}})$ for PSPWM and modified PSPWM in Fig. 5. Here it is seen that in the proximity of $D = 2/4$ the $\kappa^*(\boldsymbol{\mathcal{C}})$ for modified PSPWM is bounded, indicating $\boldsymbol{\mathcal{C}}$ is well conditioned and aligning with the better controllability of the modified PSPWM sequence. This is also later verified in experimental work.

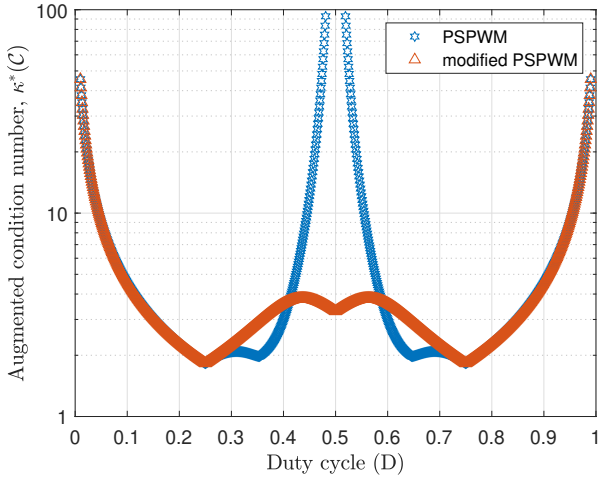

Fig. 5. Condition number of the controllability matrix for 4-cell FCML converters with PSPWM and modified PSPWM.

C. Relative Observability using Condition Number

Similar to the previous discussion, while observability is a useful concept, it does not provide intuition on the practical implementation of a state estimator. Specifically, as in [1] and [10], state observers are envisioned to use sampled (measured) values of switching node V_x to estimate (observe) actual flying capacitor voltages V_{Ci}. Here we apply straightforward considerations associated with any *practical instrumentation scheme* to highlight challenges in state estimation in the proximity of unobservable conversion ratios.

1) Estimation Algorithms: We first note the general state estimation concepts developed in past work. A key insight from [1] is that we desire to estimate the (algebraic) average $\overline{V}_C$ of flying capacitor voltages, i.e. the average of initial and final values of V_C. The algebraic average of the output equation (6) is

$$\overline{\boldsymbol{V}}_{\boldsymbol{x}} = \boldsymbol{C} \cdot \overline{\boldsymbol{V}}_{\boldsymbol{C}} + \boldsymbol{W_1} \cdot V_{in}, \tag{16}$$

where dependency on charge vector $\boldsymbol{q}$ disappears, greatly simplifying the estimation process. When the SC stage is observable, matrix $\boldsymbol{C}$ is full-rank and flying capacitor voltages can be solved:

$$\overline{\boldsymbol{V}}_{\boldsymbol{C}} = \boldsymbol{C}^{\dagger}(\overline{\boldsymbol{V}}_{\boldsymbol{x}} - \boldsymbol{W_1} \cdot V_{in}), \tag{17}$$

where $\boldsymbol{C}^{\dagger}$ is the pseudoinverse of $\boldsymbol{C}$, since it is not a square matrix and simple inverse cannot be applied. In addition, an alternative estimation algorithm can be formulated:

$$\begin{bmatrix} \overline{\boldsymbol{V}}_{\boldsymbol{C}} \\ V_{in} \end{bmatrix} = \begin{bmatrix} \boldsymbol{C} & \boldsymbol{W_1} \end{bmatrix}^{-1} \cdot \overline{\boldsymbol{V}}_{\boldsymbol{x}}, \tag{18}$$

showing that V_{in} can be estimated as well, because the system has enough information to do so. Here simple inverse can be used, as the coefficient matrix is square.

However, while (17), (18) imply straightforward (single cycle) estimation using a matrix (pseudo)inverse, the computational cost of matrix inversion is high. Thus, iterative algorithms have been proposed in [1] and [10]. For example, during phase j of period k, the switching node voltage can be expressed as a linear combination of flying capacitor voltages and the input voltage:

$$\overline{V}_{xj}(k) = bV_{in} + \sum_{i=1}^{N-1} a_i \overline{V}_{Ci}(k), \tag{19}$$

where a_i ($i = 1, 2, \cdots, N$-1), b are coefficients determined by switch states. If capacitor C_i is being charged or discharged ($a_i \neq 0$), its new estimation can be solved:

$$\overline{V}_{Ci,est}(k) = \frac{1}{a_i}(\overline{V}_{xj}(k) - bV_{in} - \sum_{n \neq i}^{N-1} a_n \overline{V}_{Cn,est}(k)), \tag{20}$$

where $\overline{V}_{Cn,est}(k)$ is the estimate of any flying capacitor voltage(s) needed to determine $\overline{V}_{Ci,est}(k)$ in period k. Thus, an iterative algorithm uses a priori knowledge of the output connection matrix $\boldsymbol{C}$ to estimate flying capacitor voltages sequentially as new information is gained from samples of the switching node V_x. For multilevel (inverter) examples, a more extensive algorithm is presented in [10]. Compared to the single-ratio (DC-DC) algorithm in [1], (20) can be appreciated as a more direct (single-cycle) estimator which can in principle converge in a single cycle as it doesn't require knowledge of previous cycle estimated values.

2) Practical Limitations and Quantification Relevant to State Observers: In order to estimate flying capacitor voltages, switching node $\boldsymbol{V}_x$ must be measured, i.e. sampled, instrumented and processed by analog (and/or) digital circuitry. Such

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circuitry will have instrumentation limitations due to settling time and memory effects [2], [10], [28].

A realistic way to incorporate first-order non-idealities is to include a representative time-constant (τ_{sh}) of the instrumentation circuit to account for finite settling time (relative to the converter switching frequency f_{sw} or phase duration) and/or memory affects, assuming a sample and hold *(S&H)* structure is used for successive V_x node sampling.

In the following analysis we assume an instrumentation scheme with settling time quantified by τ_{sh}. Hence, under inductive-mode operation, when the converter is operating at the $(m_{nom}+1)/N$ level, the acquired sample is,

$$V_{x,s,j}(k) = w_{frac} V_{x,j}(k), \tag{21}$$

where, $V_{x,s,j}(k)$ denotes the sample acquired in the j^{th} phase, $V_{x,j}(k)$ is the actual voltage of the V_x node during that phase,

$$w_{frac} = 1 - e^{-\left(\frac{m_{frac}}{N f_{sw} \tau_{sh}}\right)}, \tag{22}$$

quantify the settling dynamics of the current sample. We recall that m_{frac} is extra fractional contribution to the duty cycle of the inductive mode FCML converter. Similarly, during a phase corresponding to the m_{nom}/N level, settling dynamics follow:

$$w_{nom} = 1 - e^{\left(-\frac{(1-m_{frac})}{N f_{sw} \tau_{sh}}\right)}. \tag{23}$$

Here we may realize that (22) and (23) simply scale output equation (6) with the appropriate (first-order) settling behavior. Hence, very similar to the construction of the state equation (5), the output equation for the samples may written as,

$$\mathbf{V_{x,s}}(k) = \boldsymbol{W_{sh}} \cdot \boldsymbol{V_x}(k), \tag{24}$$

where, the weighting matrix, W_{sh} is given by,

$$\boldsymbol{W_{sh}} = \begin{bmatrix} w_{nom}\boldsymbol{I_N} & \mathbf{0_{N\times N}} \\ \mathbf{0_{N\times N}} & w_{frac}\boldsymbol{I_N} \end{bmatrix}. \tag{25}$$

Hence, the sampled output equation will be of the form,

$$\mathbf{V_{x,s}}(k) = \boldsymbol{C_s} \cdot \boldsymbol{V_C}(k) + \boldsymbol{D_s} \cdot \boldsymbol{q}(k) + \boldsymbol{W_{1s}} V_{in}, \tag{26}$$

where, from (6) and (24) we get,

$$\boldsymbol{C_s} = \boldsymbol{W_{sh}} \cdot \boldsymbol{C} \tag{27}$$

$$\boldsymbol{D_s} = \boldsymbol{W_{sh}} \cdot \boldsymbol{D} \tag{28}$$

$$\boldsymbol{W_{1s}} = \boldsymbol{W_{sh}} \cdot \boldsymbol{W_1} \tag{29}$$

As previously discussed, in resonant-mode cases the converter is not observable if m and N are not co-prime. Also, similar to the controllability example, at extreme duty cycles $D = 0$ and $D = 1$, the system is unobservable as there is no information of flying capacitor voltages. However, in the proximity of these duty cycles, finite settling time also limits the practicality of a state estimator. Therefore, for inductive-mode cases, the augmented condition number $\kappa^*(\boldsymbol{\mathcal{O}}) = \kappa(\boldsymbol{\mathcal{O}})/\sigma_{min}$ provides a simple and directly calculated metric to show the range of duty-cycles for which instrumentation challenges make it difficult to estimate the flying capacitor voltages.

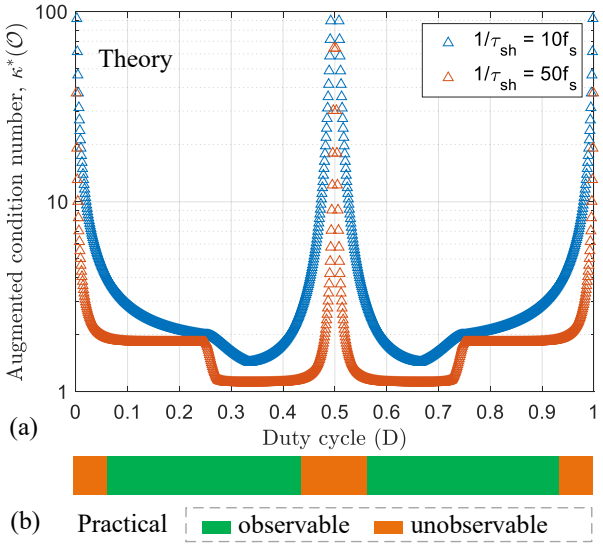

Fig. 6. Comparison of (a) Theoretically calculated augmented condition number and (b) Practical observability data from a $4-cell$ FCML converter.

Fig. 6 shows an example of $\kappa^*(\boldsymbol{\mathcal{O}})$ versus duty-cycle for a $4-$cell FCML converter for different τ_{sh} to compare the effects of instrumentation non-idealities. We observe for smaller τ_{sh}, the range of duty-cycles with high-values of $\kappa^*(\boldsymbol{\mathcal{O}})$ is narrower. This is because, with small values of τ_{sh}, the samples settle faster; *i.e.* in proximity of $D = 0.5$ in Fig. 6, there is a short time interval to acquire information from the adjacent observable conversion ratio level. Faster settling (smaller τ_{sh}) provides more information from this level, improving estimation of flying capacitor voltages. While the trend also matches with practical data reported in [2], [10], [28], the augmented condition number also quantifies the difficulty in estimating flying capacitor voltages near the extreme duty-cycle scenarios of $D = 0$ and $D = 1$.

IV. Controllability and Natural Balance

As described in the introduction, natural balance is a well-known phenomenon where passive feedback alone can drive flying capacitors towards balance [26], [27]. However, natural balance does not work at some duty cycles even if the powertrain is ideal [28], [30], and interestingly, these duty cycles match the uncontrollable scenarios identified in the previous section, implying a fundamental relationship between natural balance and controllability of the SC stage.

To understand the link between these concepts, the following analysis develops the closed-loop passive-feedback model for direct-conversion hybrid SC converters of the general form in Fig. 2. With the two subsystems, the SC stage and the output filter stage both modeled in state space, the complete model can be obtained by combining them. As shown in Fig. 7, with the two subsystems combined, their input and output signals become internal signals; the complete model only interfaces with external excitation, which is V_{in} and I_{out}.

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A. Output Filter State-Space Model

For the output filter stage, the inductor current and output voltage are affected by the switching node voltage; they also determine the charge transferred through the inductor. To quantify this relationship, the equivalent circuit of a direct-conversion hybrid SC converter in a given switching phase j is constructed in Fig. 8. As in [11], the SC stage is represented by its per-phase Thevenin equivalent capacitance, $C_{x,j}$. All series resistance, including switch and inductor resistance, is lumped into R. The differential equation model follows as:

$$\begin{bmatrix} \frac{dI_{L,j}}{dt} \\ \frac{dV_{out,j}}{dt} \\ \frac{dV_{x,j}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} & \frac{1}{L} \\ \frac{1}{C_{out}} & 0 & 0 \\ -\frac{1}{C_{x,j}} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{L,j} \\ V_{out,j} \\ V_{x,j} \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{1}{C_{out}} \\ 0 \end{bmatrix} I_{out},$$

which can be compactly denoted as:

$$\frac{d\boldsymbol{z_j}}{dt} = \boldsymbol{M_{1,j}} \cdot \boldsymbol{z_j} + \boldsymbol{M_2} \cdot I_{out}. \tag{30}$$

Solving (30) yields:

$$\boldsymbol{z_j}(t) = e^{\boldsymbol{M_{1,j}}t}\boldsymbol{z_j}(t_0) + \int_{t_0}^{t} e^{\boldsymbol{M_{1,j}}\cdot\tau}\boldsymbol{M_2}\, d\tau \cdot I_{out}, \tag{31}$$

or simply denoted as:

$$\boldsymbol{z_j}(t) = \boldsymbol{U_j}(t) \cdot \boldsymbol{z_j}(t_0) + \boldsymbol{V_j}(t) \cdot I_{out}, \tag{32}$$

where $\boldsymbol{z_j}(t)$ is the time-domain inductor current, output voltage, and switching node voltage based on their initial values $\boldsymbol{z_j}(t_0)$ at time t_0 in phase j. Thus $\boldsymbol{U_j}$ is the state transition matrix of the output filter stage; the expression in (32) can be used to determine the values $I_{L,j}$ and $V_{out,j}$ across switching phase j. It is important to note that if $C_{x,j}$ is different in certain phases, matrices $\boldsymbol{U_j}$ and $\boldsymbol{V_j}$ also need to be recalculated.

The state transition model can be used to compute the state variables of the output filter stage as they progress in a given converter phase k. This is done by iterating the state transition for each converter phase j, using the final values as the initial values for the next cycle. Ultimately, this results in the state equation for the output filter stage:

$$\boldsymbol{x}(k+1) = \boldsymbol{P} \cdot \boldsymbol{x}(k) + \boldsymbol{Q} \cdot \boldsymbol{V_x}(k) + \boldsymbol{W_2} \cdot I_{out}, \tag{33}$$

where $\boldsymbol{x} = [I_{L,0}, V_{out,0}]^T$ includes initial values of inductor current and output voltage in a given converter phase k. This is the state equation of the output filter stage, because it describes how the input signal, $\boldsymbol{V_x}$, affects the state variable, $\boldsymbol{x}$.

The output signal, charge transferred through the inductor, is equal to the charge lost on C_x in each switching phase. By tracking the voltage transition on V_x in state j,

$$\boldsymbol{q_j}(k) = C_x(V_{x,j} - V_{x,j-1}).$$

Following an iterative state transition process, similar to (33), the output equation for the filter stage can be constructed as:

$$\boldsymbol{q}(k) = \boldsymbol{R} \cdot \boldsymbol{x}(k) + \boldsymbol{S} \cdot \boldsymbol{V_x}(k) + \boldsymbol{W_3} I_{out}. \tag{34}$$

This is the output equation of the output filter stage, because it describes how the state variable, $\boldsymbol{x}$, determines the output signal of the system, $\boldsymbol{q}$. A detailed example of computing matrices $\boldsymbol{P}$, $\boldsymbol{Q}$, $\boldsymbol{R}$, $\boldsymbol{S}$, $\boldsymbol{W_2}$, and $\boldsymbol{W_3}$ for a 4-cell FCML converter can be found in [48]; these matrices and are not further developed here for the sake of brevity.

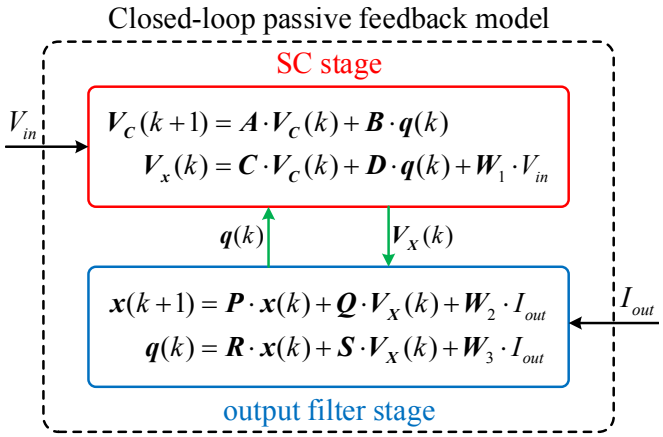

Fig. 7. Passive feedback model for a general hybrid SC converter.

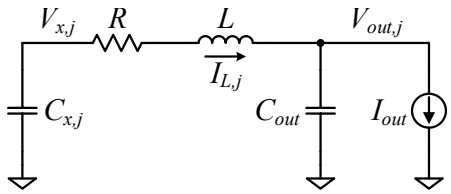

Fig. 8. Equivalent circuit of a direct hybrid SC converter in each phase [11].

B. The Complete Closed-Loop Passive-Feedback Model

The complete passive-feedback model can be obtained by combining the state space models for the SC stage and output filter stage. As shown in Fig. 7, when the two subsystems are seen as an entity, their input and output signals become internal signals and are not externally visible; the only external (exogenous) signals are input voltage V_{in} and output current I_{out}. Solving the two subsystems, (5), (6), (33), (34), gives:

$$\begin{bmatrix} \boldsymbol{V_C}(k+1) \\ \boldsymbol{x}(k+1) \end{bmatrix} = \begin{bmatrix} \boldsymbol{A}+\boldsymbol{BTSC} & \boldsymbol{BTR} \\ \boldsymbol{QC}+\boldsymbol{QDTSC} & \boldsymbol{P}+\boldsymbol{QDTR} \end{bmatrix} \begin{bmatrix} \boldsymbol{V_C}(k) \\ \boldsymbol{x}(k) \end{bmatrix} + \begin{bmatrix} \boldsymbol{BTSW_1} & \boldsymbol{BTW_3} \\ \boldsymbol{QW_1}+\boldsymbol{QDTSW_1} & \boldsymbol{W_2}+\boldsymbol{QDTW_3} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_{out} \end{bmatrix}, \tag{35}$$

where $\boldsymbol{T} = (\boldsymbol{I} - \boldsymbol{SD})^{-1}$; $\boldsymbol{I}$ is the identity matrix.

Thus, the closed-loop passive feedback model can be simply expressed as

$$\boldsymbol{x_{cl}}(k+1) = \boldsymbol{A_{cl}} \cdot \boldsymbol{x_{cl}}(k) + \boldsymbol{E} \cdot \boldsymbol{e}, \tag{36}$$

where $\boldsymbol{x_{cl}} = [\boldsymbol{V_C}, I_{L,0}, V_{out,0}]^T$ stands for the discrete-time state variables of both subsystems: the initial values in a given

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converter period k of flying capacitor voltages, the inductor current, and output voltage; $\boldsymbol{A_{cl}}$ is the state matrix of the closed loop passive feedback system; $\boldsymbol{e}$ represents the external excitation via input voltage or output current and $\boldsymbol{E}$ is its coefficient matrix. Equation (36) describes the behavior of the whole converter: the dynamics are determined by its own characteristics (circuit parameters and phase duration) and external excitation (input voltage and load current).

C. Natural Balance Analysis

For a linear circuit, the time-domain response, y, can be decomposed as the sum of the zero-state response, y_{zs}, and the zero-input response, y_{zi}:

$$y = y_{zs} + y_{zi}. \tag{37}$$

The zero-state response is excited merely by active sources; the zero-input response is excited merely by initial condition of the energy-storage components. In open-loop operation, a naturally balanced hybrid SC converter should arrive at the balanced state regardless of the initial condition. Alternatively speaking, it should satisfy:

1. The steady state of zero-state response is balanced.
2. The steady state of zero-input response is zero.

Either of the two statements alone is a necessary condition for natural balance. The following analysis will focus on the second statement as it leads to a more intuitive explanation. Since the zero-input response is investigated, active sources, $\boldsymbol{e}$, in the complete model, (36), can be set to zero, leading to the reduced model:

$$\boldsymbol{x_{zi}}(k+1) = \boldsymbol{A_{cl}} \cdot \boldsymbol{x_{zi}}(k), \tag{38}$$

where $\boldsymbol{x_{zi}}$ is the zero-input portion of state variables. Its must decay to zero in steady state for natural balance to hold:

$$\lim_{k\to\infty} \boldsymbol{x_{zi}}(k) = \boldsymbol{0}. \tag{39}$$

In discrete-time state space, this is equivalent to the condition that all eigenvalues of $\boldsymbol{A_{cl}}$ are within the unit circle.

However, when the SC stage is not controllable ($\boldsymbol{C}$ is not full-rank), there is always an eigenvalue on the unit circle. To prove it, matrix $(\boldsymbol{A_{cl}} - \boldsymbol{I})$ is decomposed as below:

$$\begin{aligned}\boldsymbol{A_{cl}} - \boldsymbol{I} &= \begin{bmatrix} \boldsymbol{BTSC} & \boldsymbol{BTR} \\ \boldsymbol{QC} + \boldsymbol{QDTSC} & \boldsymbol{P} + \boldsymbol{QDTR} - \boldsymbol{I} \end{bmatrix} \\ &= \begin{bmatrix} \boldsymbol{B} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{I} \end{bmatrix} \begin{bmatrix} \boldsymbol{TS} & \boldsymbol{TR} \\ \boldsymbol{Q} + \boldsymbol{QDTS} & \boldsymbol{P} + \boldsymbol{QDTR} - \boldsymbol{I} \end{bmatrix} \begin{bmatrix} \boldsymbol{C} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{I} \end{bmatrix},\end{aligned}$$

or abbreviated as

$$\boldsymbol{A_{cl}} - \boldsymbol{I} = \boldsymbol{B'} \cdot \boldsymbol{T'} \cdot \boldsymbol{C'}. \tag{40}$$

Due to the property of matrix multiplication, the rank of the product matrix is no greater than any of its factor matrices:

$$\text{rank}(\boldsymbol{A_{cl}} - \boldsymbol{I}) \leq \text{rank}(\boldsymbol{C'}). \tag{41}$$

When $\boldsymbol{C}$ is not full-rank, neither is $\boldsymbol{C'}$, therefore, according to (41), matrix $\boldsymbol{A_{cl}} - \boldsymbol{I}$ is not full-rank, indicating:

$$|\boldsymbol{A_{cl}} - \boldsymbol{I}| = 0, \tag{42}$$

meaning an eigenvalue of $\boldsymbol{A_{cl}}$ is one, which is on the unit circle. In this case, steady state of the zero-input response is finite but non-zero, thus natural balance fails. To summarize, *the SC stage being controllable is a necessary condition for natural balance*.

This conclusion can be intuitively understood by recognizing the relationship between the two subsystems in Fig. 2. The harmonic feedback of the inductor, described in [30], can be regarded as an intrinsic control effort of the output filter stage on the SC stage. However, for this mechanism to take effect, the SC stage has to be controllable; otherwise natural balance cannot function. The above analysis is similar to the recent work [50] on determining the indeterminacy of general switched-mode power converters.

1) Natural Balance Scenarios: Closed-Loop Eigenvalues: An additional use of the closed loop model in (36) is to explore the *'strength'* of natural balance given realistic converter scenarios. For example, the balancing speed is indicated by location of $\boldsymbol{A_{cl}}$ eigenvalues, which depends on converter parameters (resistance, inductance, capacitance, switching frequency, etc.). It is slower when the dominant eigenvalue (the one with largest amplitude) is closer to the unit circle.

Intuitively this is because the discrete-time eigenvalues govern asymptotic stability (settling to the balanced level) of flying capacitor voltages. With eigenvalue magnitudes less than unity, after each switching period, any residual imbalance will decrease in magnitude, asymptotically converging to zero. Thus, with lower eigenvalue magnitude(s), imbalance decays faster and natural balance is *'stronger.'* With an eigenvalue on the unit circle, the system is *marginally stable:* the steady state is finite but non-zero – any initial imbalance in the system never decays. As natural balance relies on passive feedback, eigenvalue magnitudes can never be greater than unity, but this does not ensure immunity to disturbances: duty cycle mismatch [30], finite bypass capacitance [31], etc.

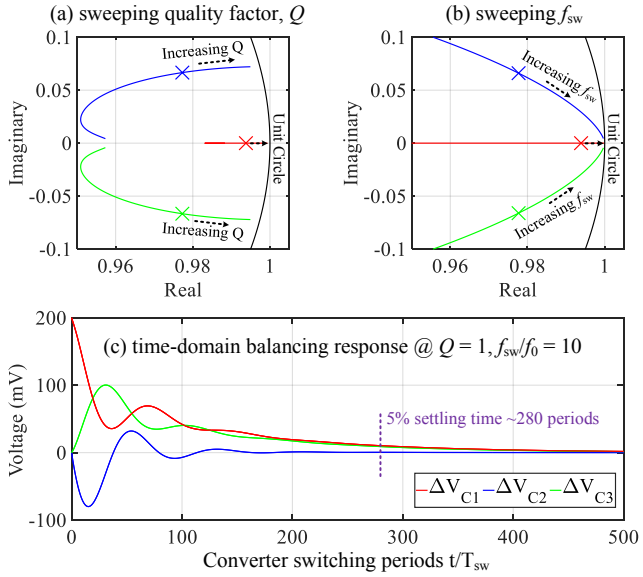

Fig. 9. Discrete-time eigenvalue trajectories and time-domain response from closed loop passive feedback model for a 4-cell (5-level) FCML converter.

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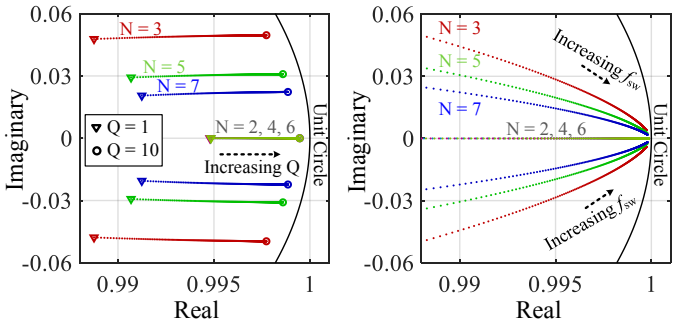
Fig. 9 shows an example trajectory for closed loop eigenvalues when sweeping resistance (ESR) and switching frequency for a 4-cell (5-level) FCML converter with $D = 1/4$. In Fig. 9(a), resistance is scaled such that quality factor Q of the equivalent circuit ranges from 0.1 to 10 with switching frequency f_{sw} of the FCML converter held such that $f_{sw}/f_0 = 10$ where f_0 is the effective resonant frequency of the equivalent circuit(s). In Fig. 9(b) f_{sw} is scaled between $5\times$ to $35 \times f_0$, while holding $Q = 1$. The markers indicate where $Q = 1$ and $f_{sw}/f_0 = 10$; showing that for both higher Q and higher f_{sw}, eigenvalues move towards the unit circle, corresponding to slower natural balance dynamics relative to the converter switching period.

This is further explored in Fig. 9(c) which provides a time-domain perspective on balance dynamics for $Q = 1$ and $f_{sw}/f_0 = 10$. Here, an initial (unbalanced) voltage is given to V_{C1} such that $\Delta V_{C1} = 200mV$, which is allowed to decay via natural balance. This scenario requires ∼280 full switching periods of the 4-cell FCML converter to reach 5% of steady state. Thus even with low Q, the amplitude of the dominant eigenvalue is still close to 1 (>0.98 in this example), indicating that natural balance is a 'weak' process and is generally slow.



(a) sweeping quality factor, Q (b) sweeping f_{sw}

Fig. 10. Trajectory of *dominant* discrete-time eigenvalues at the nominal $1/N$ conversion ratio level for $N = 2 \ldots 7$ FCML converters.

Expanding on this perspective, Fig. 10 shows the dominant eigenvalues for FCML converters at the nominal $D = 1/N$ conversion ratio level for $N = 2 \ldots 7$.[6] Interestingly, for $Q > 1$, the dominant eigenvalues for even-N follow an identical trajectory and lie on the real axis. The dominant eigenvalues for odd-N are complex conjugate pairs, but are always lower in magnitude than the next adjacent even-N FCML converter. The lower magnitude eigenvalues for odd-N (even-level) FCML converters indicates faster settling or 'stronger' natural balance than for even-N (odd-level), aligning with previous literature on natural balance [2], [31], [47], which shows even-level converters to have better balance characteristics.

Fig. 11 shows a more comprehensive and design-focused perspective on the relative settling time of natural balancing versus duty cycle [2], [53]. The settling time of each of the $N = 2 \ldots 6$ FCML converters is estimated based on the dominant eigenvalue magnitude with $Q = 1$ and $f_{sw}/f_0 = 10$ and is normalized to the $N = 2$ (3-level) converter with $D = 50\%$. The *star* annotation indicates the nominal $1/N$ (resonant or nominal) conversion ratio level.

[6]Note that Fig. 10 shows only dominant eigenvalues and in fact, the examples for $N = 4$ and above each have additional (non-dominant) eigenvalues (one per each flying capacitor). Similar to Fig. 9, in each case, eigenvalues move towards the unit circuit for higher Q and switching frequency, although non-dominant eigenvalues have less impact on natural balance 'strength.'

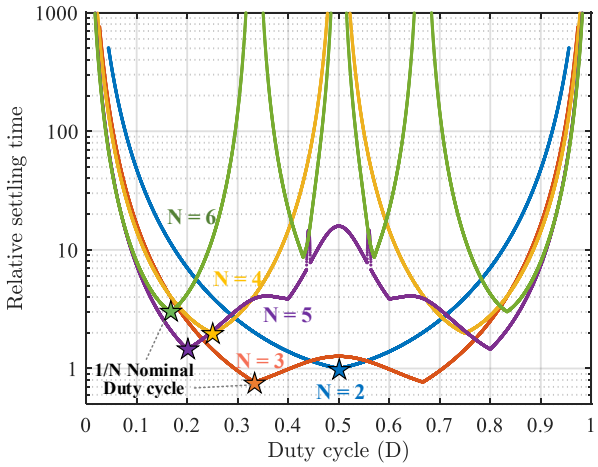


Fig. 11. Relative settling time of natural balanced FCML converters with $Q = 1$ and $f_{sw}/f_0 = 10$. Stars indicate nominal $1/N$ conversion ratio.

Several important observations can be made from Fig. 11. First, the differences in settling time for odd- vs even-N converters are more apparent: at the nominal $1/N$ ratios, the relative settling times match those provided in [2]. Note that while even-N converters have the same dominant eigenvalues for $Q > 1$, higher-N converters are slower at the same normalized frequency (f_{sw}/f_0) because they have more switching phases and therefore a longer switching period. Thus $N = 4$ and $N = 6$ have respectively $\sim 2\times$ and $\sim 3\times$ longer settling than for $N = 2$. Odd-N converters have shorter settling time than adjacent even-N but this increases faster vs N: higher-level odd-N converters have both a longer normalized switching period and eigenvalues moving closer to the unit circle.

The second important observation is a qualitative comparison of Fig. 11 to Fig. 4. It is seen that the general trend of settling time based on passive feedback (natural balance) aligns with predictions of the augmented condition number, $\kappa^*(\mathcal{C})$. Specifically, the closed-loop eigenvalues of the passive feedback model predict the same extrema at non-coprime conversion ratio levels as well as near the $D = 0$ and $D = 1$ levels. The model also confirms the trend of generally 'weaker' controllability as the number of levels increases.

However, while Fig. 11 and Fig. 4 match qualitatively, there are noticeable differences. Specifically, $\kappa^*(\mathcal{C})$ does not predict the observed differences in even- vs odd-N settling time or closed-loop eigenvalue position. Importantly, this is because $\kappa^*(\mathcal{C})$ only provides information on the SC-stage and has no knowledge of the controller or its associated dynamics. With natural balance, the output filter stage has particular dynamics that interact with the SC stage forming unique closed loop properties. An example of these dynamics is the 'harmonic feedback' concept, described in [30] which can lead to periodic asymmetries in even- vs odd-level converters and can not be captured in $\kappa^*(\mathcal{C})$ alone. Also, slight modifications, (*i.e.* different Q or f_{sw}/f_0) will move the closed loop eigenvalues,

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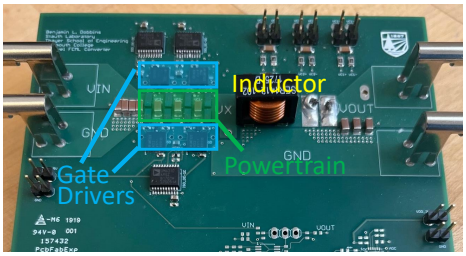

Spec	Value
V_{in}	24 V
C_{fly}	3.3 µF*
L	1 µH
C_{out}	9.9 µF*
C_{in}	13.2µF*
f_{sw}	250kHz
FETs	EPC GaN

*derated @ nom. voltage

Fig. 12. Annotated photo of the 4-cell FCML converter PCB.

changing the shape of the curves in Fig. 11, even if their overall trends are the same.

Finally, for an active controller, the closed loop dynamics may be entirely different than with natural balance, but such controller will still have difficulty near the extreme duty cycles predicted in Fig. 4. Thus the benefit of the $\kappa^*(\boldsymbol{\mathcal{C}})$ metric is that it is very easy to calculate based on the output connection matrix and provides insight into potential control challenges, as well as ways to alleviate these through techniques like modified PSPWM [2].

2) Hardware Verification of Natural Balance Model: A hardware prototype was used to verify both natural balance dynamics and controllability concepts. The 4-cell FCML converter and component details are shown in Fig. 12. The prototype uses modest $C_{fly} \approx 3.3\,\mu F$ and runs at $f_{sw} \approx 250\,kHz$. In steady state, the flying capacitor voltages are measured at $0.4 < D < 0.6$, where imbalance is most severe under conventional PSPWM.

The imbalance quantities, ΔV_{Ci}, which represent the difference between the measured values to the balanced values, as well as the output voltage are plotted in Fig. 13. The results show that modified PSPWM significantly reduces imbalance quantities (strengthens natural balance) in the vicinity of uncontrollable duty cycles.

The results in Fig. 13 can be compared to the augmented condition number $\kappa^*(\boldsymbol{\mathcal{C}})$ for the same converter in Fig. 5. While natural balance cannot be achieved at $D = 0.5$, it is also poor in the vicinity of this uncontrollable conversion ratio. However, the use of modified PSPWM is able to correct for the uncontrollable switching network by adding states in the switching sequence. This improves controllability and allows natural balance to succeed in the previously unbalanced regions. However, as discussed in [2] modified PSPWM can increase conduction loss because the added switching states have more flying capacitors in the conduction path. This is more of an impact at heavy load, where conduction loss dominates. Nevertheless, modified PSPWM allows natural balance and affords opportunities for active balance compensation schemes at otherwise uncontrollable duty cycles.

V. Flying Capacitor Voltage Estimator

An additional point of verification to the model in Section III is the development of a hardware platform for the flying capacitor voltage state estimation. Here we present an improved (faster settling) estimator leveraging the platform developed

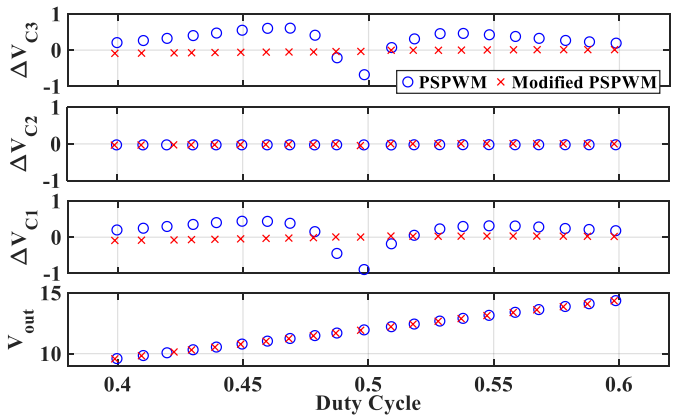

Fig. 13. Measured flying capacitor voltages with PSPWM and mod. PSPWM.

Phase, j	1	2	3	4	5
$V_x =$	V_{C1}	V_{C2}	$V_{C2} - V_{C1}$	$V_{C3} - V_{C1}$	$V_{C3} - V_{C2}$
$\boldsymbol{V_{est}} =$	$\boldsymbol{V_{C1} = V_x}$	$\boldsymbol{V_{C2} = V_x}$	$\boldsymbol{V_{C1} = V_{C2} - V_x}$	$\boldsymbol{V_{C3} = V_x + V_{C1}}$	$\boldsymbol{V_{C2} = V_{C3} - V_x}$

Phase, j	6	7	8	9	10
$V_x =$	$V_{C4} - V_{C2}$	$V_{C4} - V_{C3}$	$V_{in} - V_{C3}$	$V_{in} - V_{C4}$	$V_{in} - V_{C4} + V_{C1}$
$\boldsymbol{V_{est}} =$	$\boldsymbol{V_{C4} = V_x + V_{C2}}$	$\boldsymbol{V_{C3} = V_{C4} - V_x}$	$\boldsymbol{V_{in} = V_x + V_{C3}}$	$\boldsymbol{V_{C4} = V_{in} - V_x}$	$\boldsymbol{V_{in} = V_x + V_{C4} - V_{C1}}$

Fig. 14. Itertive estimation algorithm for 5-cell FCML at $D = 1.5/5$.

in [1]. Specifically, as previously discussed, iterative state estimators are more practical in hardware implementation due to the high cost of matrix inversion. The proposed estimator uses the algorithm shown in (20), applied to a 5-cell (6-level) FCML hardware prototype.

Exploring a slightly different estimation algorithm than in [1], Fig. 14 shows one of multiple possible iterative sequences to estimate flying capacitor voltages for a 5-cell FCML converter at $D = 1.5/5$. Note from Fig. 3 that this lies between two nominal conversion ratio levels, notably $D = 1/5$ and $D = 2/5$. This requires a $2N = 10$ switching state sequence, but also the possibility of two estimates of each flying capacitor voltage and the input voltage each converter period. Multiple estimates result in a slightly '*better conditioned*' observability matrix and the benefits of this are seen in experimental results.

The flying capacitor voltage estimator was designed and evaluated on a 5-cell FCML converter. The top-level block diagram is shown in Fig. 15. The switching node voltage, V_x, is divided down and processed by the pre-amplifier. The sample clock triggers the analog to digital converter (ADC) to take a measurement of V_x, which is then transferred to a field programmable gate array (FPGA) device through a serial peripheral interface (SPI). Based on the measurement of V_x and the current switch states, the FPGA calculates the estimated flying capacitor voltages and store them in the random access memory (RAM). Finally, the results are moved to MATLAB by an universal asynchronous receiver-transmitter (UART) to be visualized.

The hardware platform itself is shown in Fig. 16. The 5-cell converter is designed for input voltage $V_{in} = 36V$, and operates at $f_{sw} = 250kHz$. Instrumentation for the V_x node includes a 70 MHz GBW instrumentation amplifier and 12-bit,

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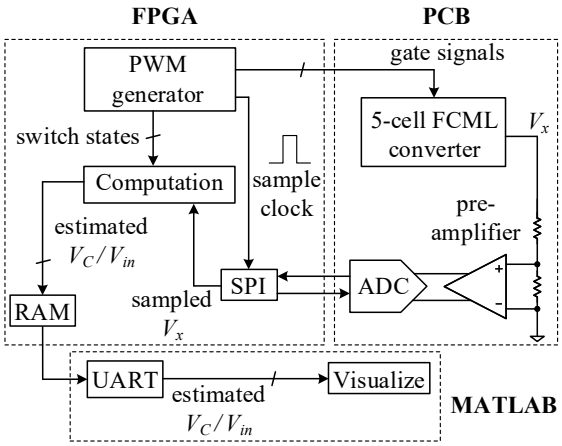
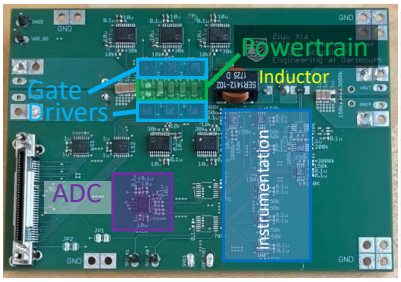


Fig. 15. Block diagram of the flying capacitor voltage estimator.



Spec	Value
V_{in}	36 V
C_{fly}	3.3 µF
L	1 µH
Pre-amp	$\omega_u = 70MHz$
ADC	5Msps, 12bits
f_{sw}	250kHz
GaN FETs	16mΩ, 40V

Fig. 16. Photo of 5-cell FCML estimation platform.

5 Msps ADC. Otherwise the converter specifications are fairly modest as this platform was designed primarily to explore state estimation at different conversion ratios.

The estimator was explored with different conversion ratios, specifically the $D = 1/5$ case explored in [1] and the $D = 1.5/5$ case outlined in Fig. 14. Transient behavior of the estimator was examined by operating the converter in balanced steady state. The estimator is activated with initial estimations set to zero. The output result of the estimator is recorded over time with results plotted in Matlab.

Fig. 17 shows estimator transient response for $D = 1/5$ using the algorithm in (20), which is slightly improved compared to [1] as it can achieve (unfiltered) estimates in a single converter switching period. While the unfiltered estimates can be gained quickly, they are subject to noise. To reduce noise a simple (running average) infinite-impulse response (IIR) filter was used in the FPGA; the filter is a simple (equal-weight) average of the running estimate and new estimate; many other digital filter schemes could be used in practice so this is mainly to illustrate the use of a basic filter. An important note is that here, the filtered estimates settle to within 5% of steady state within 5 converter periods, compared to 9 periods to settle in [1], illustrating the advantage of a slightly modified iterative estimation algorithm.

Fig. 18 shows estimator transient response for $D = 1.5/5$ using the algorithm in Fig. 14. Here, because the 2-level switching sequence permits multiple samples of each estimated quantity per converter period, the transient response is faster than the $D = 1/5$ case in Fig. 17. Specifically, the benefit comes from the fact that multiple samples per period improve the convergence speed of the IIR filter. In the $D = 1.5/5$ case, the IIR-filtered estimates settle to within 1% of steady state in under 3 converter periods. Again, this relates to the observability condition number $\kappa(\mathcal{O})$; *i.e.* the $D = 1.5/5$ observability matrix is better conditioned than pure nominal ratios as there is more information in the 2-level multiplexed FCML operation.

Another characterization of the estimator is to quantify total noise in estimated capacitor voltages. To do this, a total number of 3000 consecutive estimations were collected for each flying capacitor in steady state operation. They are compared against accurately measured DC voltages using a digital multimeter. The estimation error is normalized to the DC flying capacitor voltage and a histogram is shown in Fig. 19. The maximum steady state estimation error does not exceed 0.25% for all flying capacitors, proving accuracy of the estimation algorithm.

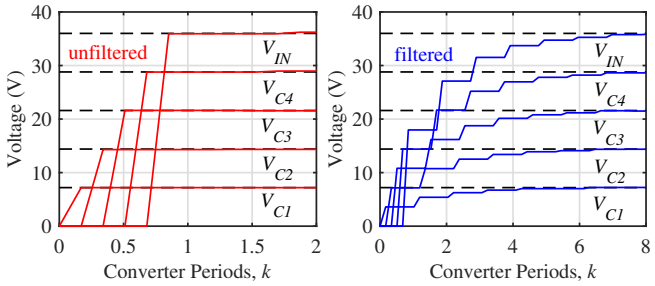


Fig. 17. Estimator transient response from zero initial conditions for $D = 1/5 = 0.2$.

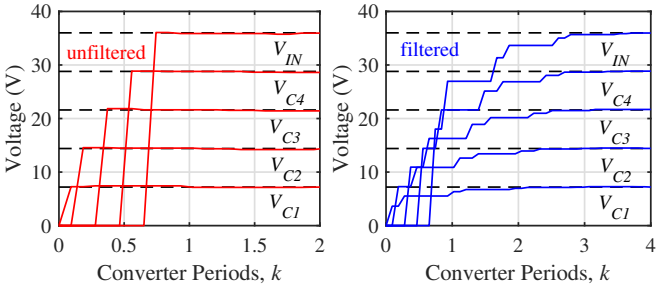


Fig. 18. Estimator transient response from zero initial conditions for $D = 1.5/5 = 0.3$.

VI. Conclusion

This work developed a comprehensive state-space model that can be used to explore the complex and high-order dynamics associated with the switched-capacitor networks in a variety of hybrid and resonant switched capacitor (SC) converters. The state space model was exemplified through application to flying-capacitor multilevel (FCML) DC-DC converters to expand on the basic concepts of flying capacitor observability and controllability. The concept of *condition number* was used to quantify relative observability and controllability, providing several new perspectives on flying capacitor state regulation

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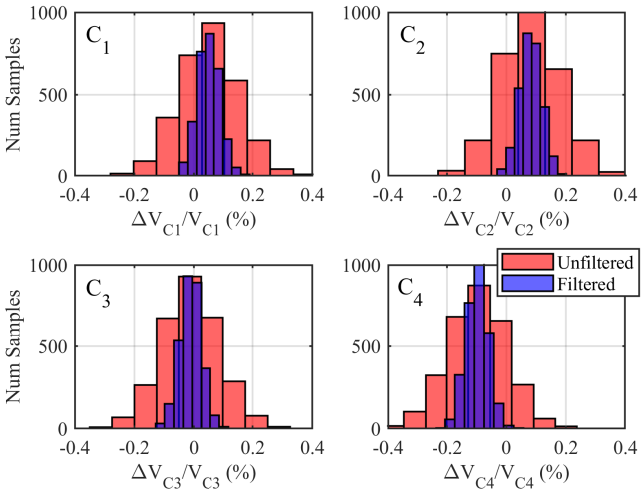

Fig. 19. Histogram of normalized steady state estimation error.

and estimation. A closed-loop passive feedback model was developed and used to illustrate the relationship between controllability and natural balance. Two hardware prototypes were used: a first to explore natural balance in the context of the condition number treatment; a second to explore opportunities for state estimation of flying capacitor voltages. Overall this works hopes to add to the body of knowledge in control and modelling of hybrid SC converters such that faster and more reliable regulation schemes can be developed in the future.

Appendix A
Proof for relative duration of operation in the two resonant modes

Under the inductive mode of operation, we denote the fraction of time for which the converter operates in the m_{nom+1}/N mode during a switching period, $1/f_{sw}$, be D_{frac}. Hence, it operates in the m_{nom}/N mode for $(1-D_{frac})$ fraction of $1/f_{sw}$. If we look at the operation for $1/N$ fraction of the total switching period, the same timing split exists between the two resonant modes of operation.

Referring to Fig. 1(a), we observe that, the on-time of each switch is the sum of m_{nom+1} and m_{nom} segments of the converter operating in the m_{nom+1}/N and m_{nom}/N modes respectively. Therefore, the converter duty cycle is given by,

$$D = \frac{m}{N} = \frac{m_{nom+1}D_{frac} + m_{nom}(1-D_{frac})}{N}. \tag{43}$$

We recall that $m_{nom+1} = m_{nom}+1$ and using (2), we simplify (43), to get,

$$D_{frac} = m_{frac}. \tag{44}$$

This shows that the converter operates in the m_{nom}/N and m_{nom+1}/N resonant modes for $(1-m_{frac})$ and m_{frac} duration of the total switching period to accomplish the desired inductive mode operation.

Appendix B
DT SS construction example for Inductive mode operation

Here we show the construction of DT SS equations for an example $D = 1.3/4$ FCML converter. Referring to (3) and (4), we get,

$$\mathbf{B} = (\frac{1}{C_f})\boldsymbol{B_{con}}\boldsymbol{M_{con}} = (\frac{1}{C_f})\mathbf{B_{con}}\begin{bmatrix}0.7\mathbf{I_4} & \mathbf{0_{4\times4}}\\ \mathbf{0_{4\times4}} & 0.3\mathbf{I_4}\end{bmatrix},$$

where,

$$\mathbf{B_{con}} = \begin{bmatrix}-1 & 1 & 0 & 0 & -1 & 0 & 1 & 0\\ 0 & -1 & 1 & 0 & 0 & -1 & 0 & 1\\ 0 & 0 & -1 & 1 & 1 & 0 & -1 & 0\end{bmatrix} = \begin{bmatrix}\mathbf{B_{con,1}}\\ \mathbf{B_{con,2}}\end{bmatrix}^T,$$

where, $\mathbf{B_{con,1}}$ and $\mathbf{B_{con,2}}$ are the individual 3×4 state connection matrices of the $1/4$ and $2/4$ resonant modes respectively. Hence, the input matrix for this example is,

$$\mathbf{B} = (\frac{1}{C_f})\begin{bmatrix}0.7\mathbf{B_{con,1}} & 0.3\mathbf{B_{con,2}}\end{bmatrix}.$$

For brevity, we state without proving that the above example may be extended for the general case to obtain,

$$\mathbf{B} = (\frac{1}{C_f})\begin{bmatrix}(1-m_{frac})\mathbf{B_{con,nom}} & m_{frac}\mathbf{B_{con,nom+1}}\end{bmatrix}. \tag{45}$$

As mentioned in Section II-B2, the output connection matrix is $\boldsymbol{C} = -\boldsymbol{B_{con}^T}$, hence for this example we get,

$$\boldsymbol{C} = \begin{bmatrix}1 & 0 & 0\\ -1 & 1 & 0\\ 0 & -1 & 1\\ 0 & 0 & -1\\ 1 & 0 & -1\\ 0 & 1 & 0\\ -1 & 0 & 1\\ 0 & -1 & 0\end{bmatrix} = \begin{bmatrix}-\boldsymbol{B_{con,1}^T}\\ -\boldsymbol{B_{con,2}^T}\end{bmatrix}.$$

The $\boldsymbol{D}$ matrix in (6) has the following construction. This matrix captures the phase by phase charge accumulation in the flying capacitors as well their connections. For easier explanation, we show the construction of the $D = 1.3/4$ example but the same can be applied for any $D = m/N$ case. The row corresponding to the first phase (operating in $2/4$ resonant mode) is formed by

$$\begin{bmatrix}D_{51}\\ \vdots\\ D_{58}\end{bmatrix}^T = (\frac{1}{C_f})\begin{bmatrix}1\\ 0\\ -1\end{bmatrix}^T\begin{bmatrix}0 & 0 & 0 & 0 & -0.3 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0.3 & 0 & 0 & 0\end{bmatrix}.$$

Therefore, we are multiplying the row of $\boldsymbol{C}$ corresponding to the first phase with a matrix of similar form as $\boldsymbol{B}$ except that the column for the first phase all other columns are null because charges from the future phases are yet to flow.

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```
function [A,B,C,D,W1,m_frac] = FCML_SS(N,m,Cfly)
% N+1 level FCML
% m/N duty cycle
% All flying capacitances are identical to Cfly


% Evaluation of A
A = eye(N-1);
%%%


% Evaluation of B
m_nom = floor(m);
m_nomP1 = ceil(m);
m_frac = m - m_nom;

base_seq_nom = zeros(1,N);
base_seq_nomP1 = zeros(1,N);


if(m_nom>0 && m_nom~=N)
base_seq_nom(1,1) = -1;
base_seq_nom(1,m_nom+1) = 1;
end


if(m_nomP1<N)
base_seq_nomP1(1,1) = -1;
base_seq_nomP1(1,m_nomP1+1) = 1;
end


for i=1:N-1
     Bcon_nom(i,:) = circshift(base_seq_nom,i-1);
     Bcon_nomP1(i,:) = circshift(base_seq_nomP1,i-1);
end


Bcon = [Bcon_nom Bcon_nomP1];
Mcon = [(1-m_frac).*eye(N) zeros(N,N);zeros(N,N) m_frac.*eye(N)];
B_norm = Bcon*Mcon;
B = B_norm./Cfly;
%%%

% Evaluation of C
C = -Bcon';
%%%

% Evaluation of D
D_temp = zeros(N-1,2*N);
for i=1:2*N
    if(mod(i,2)==1)
        duty_indx = m_frac;
        indx = N+((i+1)/2);
    else
        duty_indx = 1-m_frac;
        indx = (i/2);
    end

    D_temp(:,indx) = duty_indx.*Bcon(:,indx);
    D(indx,:) = -Bcon(:,indx)'*D_temp;
end
D = D./Cfly;
%%%

% Evaluation of W1
W1_nom = ones(N,1);
W1_nomP1 = ones(N,1);


if (m_nom == 0)
    W1_nom = zeros(N,1);
else
    W1_nom(m_nom:N-1,1) = zeros(N-m_nom,1);
end


if (m_nomP1 == 0)
    W1_nomP1 = zeros(N,1);
else
    W1_nomP1(m_nomP1:N-1,1) = zeros(N-m_nomP1,1);
end


W1 = [W1_nom;W1_nomP1];

%%%

end
```

Fig. 20. MATLAB function to generate DT SS matrices for generic m/N FCML converter.

Continuing the construction, the row for the second phase (operating in $1/4$ resonant mode) is given by,

$$\begin{bmatrix} D_{11} \\ \vdots \\ D_{18} \end{bmatrix}^T = (\frac{1}{C_f}) \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}^T \begin{bmatrix} -0.7 & 0 & 0 & 0 & -0.3 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0.3 & 0 & 0 & 0 \end{bmatrix}.$$

We can keep repeating this for every phase to obtain for the final phase (operating in $1/4$ resonant mode),

$$\begin{bmatrix} D_{41} & \dots & D_{48} \end{bmatrix} = (\frac{1}{C_f}) \begin{bmatrix} 0 & 0 & -1 \end{bmatrix} \boldsymbol{B}.$$

Finally for the current example the matrix $\boldsymbol{W_1}$ in (6) is given by,

$$\boldsymbol{W_1} = \begin{bmatrix} 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}^T.$$

For the reference of the reader, the MATLAB function generating the above matrices for generic m/N FCML converter is shown in Fig. 20.

APPENDIX C
PROOF FOR CONDITION OF CONTROLLABILITY AND OBSERVABILITY OF A FCML CONVERTER

As described in Section III-A, the rank $\boldsymbol{B}$ will be unaffected by the diagonal matrix M_{con} and depend only on $\boldsymbol{B_{con}}$. Since, the matrices from (5) and (6) are related as $\boldsymbol{C} = -\boldsymbol{B_{con}^T}$. Thus controllability and observability matrices for are also related as $\boldsymbol{\mathcal{O}} = -\boldsymbol{\mathcal{C}}^T$. Therefore the proof for condition for observability *i.e.,* $\boldsymbol{C}$ is full-rank, will also hold for controllability.

In the resonant mode (m is an integer), $\boldsymbol{C}$ always has more rows than columns, thus its rank is determined by the number of linearly dependent column vectors. The first column, $\boldsymbol{C_{*1}}$, has the form,

$$\boldsymbol{C_{*1}} = \begin{bmatrix} 1 & 0 & \dots & -1 & 0 & \dots \end{bmatrix}^T, \tag{46}$$

where there are $(m-1)$ zeros in the middle and $(N-m-1)$ zeros in the end. The p^{th} column is obtained by circular shifting $\boldsymbol{C_{*1}}$ by $(p-1)$ steps.

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If there exist an non-zero row vector $\boldsymbol{\gamma} = \begin{bmatrix}\gamma_1 & \dots & \gamma_{N-1}\end{bmatrix}$, such that,

$$\sum_{p=1}^{N-1} \gamma_p \cdot \boldsymbol{C_{*p}} = \mathbf{0}, \tag{47}$$

then, C is not full-rank and vice-versa.

Solving (47) gives,

$$\gamma_p = \begin{cases} 0 & p = m \text{ or } p = N-m, \\ \gamma_{(p+N-m)\%N} & \text{otherwise}, \end{cases} \tag{48}$$

where the symbol $\%$ represents the modulo operation.

When m and N are not co-prime, they have a greatest common divider, $g(>1)$. Using (48), we get,

$$\begin{aligned} &\gamma_1 = \gamma_{g+1} = \ldots = \gamma_{N-g+1}, \\ &\vdots \\ &\gamma_{g-1} = \gamma_{2g-1} = \ldots = \gamma_{N-1}, \\ &\gamma_g = \gamma_{2g} = \ldots = \gamma_{N-g} = 0, \end{aligned} \tag{49}$$

which leads to,

$$\begin{aligned} &\boldsymbol{C_{*1}} = \boldsymbol{C_{*(g+1)}} = \ldots = \boldsymbol{C_{*(N-g+1)}}, \\ &\vdots \\ &\boldsymbol{C_{*(g-1)}} = \boldsymbol{C_{*(2g-1)}} = \ldots = \boldsymbol{C_{*(N-1)}}. \end{aligned} \tag{50}$$

This means that there are $(g-1)$ linear dependency among the column vectors, leading to the conclusion for m and N not co-prime scenario that,

$$\text{rank}(\boldsymbol{C}) = N - g. \tag{51}$$

For the m and N coprime case, we substitute $g = 1$ in (49) to get,

$$\gamma_1 = \gamma_2 = \ldots = \gamma_{N-1} = 0, \tag{52}$$

indicating,

$$\text{rank}(\boldsymbol{C}) = N - 1, \tag{53}$$

i.e., $\boldsymbol{C}$ is full-rank.

In the inductive mode, we get,

$$\text{rank}(\boldsymbol{C}) = \text{rank}\begin{bmatrix} -\boldsymbol{B_{con,nom}^T} \\ -\boldsymbol{B_{con,nom+1}^T} \end{bmatrix}. \tag{54}$$

Following a similar derivation method as the resonant mode, it is straightforward to show that $\boldsymbol{C}$ is always full-rank in inductive mode.

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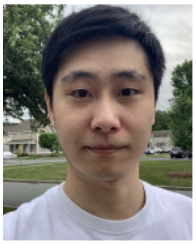

Ziyu Xia (Graduate Student Member, IEEE) received B.E. degree in Electrical Engineering from Shanghai Jiao Tong University, Shanghai, China, in 2016. He completed the Ph.D. degree at Thayer school of Engineering, Dartmouth College, Hanover, USA, in 2022. Dr. Xia is currently with Apple Inc, Cupertino, CA. His research area includes modeling, control and integrated implementation of DC-DC power converters, with an emphasis on soft-charging (hybrid, resonant) switched-capacitor converters.

Kishalay Datta (Graduate Student Member, IEEE) completed B.Tech from IIEST, Shibpur, India, in 2014 and M.S. from IIT Madras, India, in 2019. He was with Texas Instruments, Bengaluru, India, in Kilby Labs and the Isolation Group from 2015 to 2020. He received the best student paper award at the Custom Integrated Circuits Conference (CICC) 2023 and is currently working towards his PhD at Dartmouth College, USA. His interests include power management and analog mixed-signal IC design.

Jason T. Stauth (Member, IEEE) received the M.S. and Ph.D. degrees from the University of California at Berkeley, Berkeley, CA, USA, in 2006 and 2008, respectively. He is currently an Associate Professor with the Thayer School of Engineering, Dartmouth College, Hanover, NH, USA.

Dr. Stauth is Co-Director of the National Science Foundation (NSF) Power Management Integration Center (PMIC) Industry/University Cooperative Research Center. He is a member of the International Solid-State Circuits Conference (ISSCC) and Custom Integrated Circuits Conference (CICC) Technical Program Committees. He received the National Science Foundation CAREER Award in 2016 and the Excellence in Teaching Award from the Thayer School of Engineering in 2018. He served as an Associate Editor for the IEEE Transactions on Power Electronics (TPEL) and IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE) from 2016 to 2021 and is currently Associate Editor of the IEEE Solid-State Circuits Letters (SSCL).

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